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FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA

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METODOLOGIJA ZA PONAŠAJNO MODELIRANJE BLOKOVA INTEGRIRANIH SKLOPOVA ZA PRIMJENE U ELEKTROMAGNETSKOJ KOMPATIBILNOSTI

DOKTORSKI RAD

Mentor: Prof. dr. sc. Adrijan Barić

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About the Supervisor

Adrijan Barić was born in Zagreb in 1958. He received the Dipl. Ing. degree in 1982 and the M.Sc. degree in 1985 from the University of Zagreb (UniZag), Faculty of Electrical Engineering and Computing (FER), Croatia. He received the PhD degree in 1995 from the Dublin City University, Ireland. He is employed by FER since 1984. He was a visiting researcher at the Rutherford Appleton Laboratory, England, and at the Ghent University, Belgium. He was promoted to Full professor in 2013. He was a principal investigator of two projects funded by the Ministry of Science, Education and Sports of Croatia, one BICRO project, and he coordinated the FER research team in one EU FP6 project, one EU FP7 project, and several bilateral and multilateral projects with European companies and universities. He presently coordinates the project "Sensor Fusion" funded by ams-OSRAM AG, Austria, and the project "Fast switching converters based on GaN devices and resonant architectures" funded by the Croatian Science Foundation. He published over 100 papers in scientific journals and scientific conference proceedings in the area of integrated circuits and electromagnetic compatibility. He was the President of the Committee for Research, Development and Technology of the UniZag from 2008 to 2011, and the President of the Council of Technical Faculties of the UniZag from 2013 to 2017. He was a General Chair or Co-Chair of two IEEE conferences, the Finance Chair of one IEEE conference, and the Technical Programme Chair of the IEEE conference EMC Compo 2011. He is a member IEEE, HD MIPRO, KoREMA, and AMAC-FER societies. In 2015, he received the Gold Plaque "Josip Lončar" from FER.

O mentoru

Adrijan Barić rođen je u Zagrebu 1958. Diplomirao je 1982. i magistrirao 1985. na Fakultetu elektrotehnike i računarstva (FER) Sveučilišta u Zagrebu (SuZ). Doktorirao je 1995. na Dublin City University, Irska. Na FER-u radi od 1984. Bio je gostujući istraživač na Rutherford Appleton Laboratory, Engleska te na Ghent University, Belgija. U redovitog profesora u trajnom zvanju izabran je 2013. Bio je glavni istraživač na dva projekta MZOS-a, jednom BICRO projektu te je vodio je FER-ov tim u jednom EU FP6, jednom EU FP7 projektu te više bilateralnih i multilateralnih projekata s europskim tvrtkama i sveučilištima. Trenutno vodi projekt HRZZ-a „Brzi prekidački pretvornici zasnovani na GaN elementima i rezonantnim arhitekturama" te projekt „Sensor Fusion" s tvrtkom ams-OSRAM AG, Austrija. Objavio je više od 100 radova u znanstvenim časopisima i zbornicima znanstvenih konferencija iz područja integriranih sklopova i elektromagnetske kompatibilnosti. Bio je predsjednik Odbora za istraživanje, razvoj i tehnologiju SuZ-a od 2008. do 2011. te predsjednik Vijeća tehničkog područja SuZ-a od 2013. do 2017. Bio je predsjedatelj ili supredsjedatelj dviju IEEE konferencija, financijski voditelj jedne IEEE konferencije te Technical Programe Chair IEEE konferencije EMC Compo 2011. Član je udruga IEEE, HD MIPRO, KoREMA i AMAC-FER. Godine 2015. primio je FER-ovu Zlatnu plaketu „Josip Lončar".

Mojem Didu.

Abstract

The echo state network (ESN) is presented as the building block for the behavioural modelling of integrated circuits. The ESN is able to model the nonlinear relationships of time-domain signals observed in integrated circuit simulations. An adaptive algorithm for sampling the nonlinear behaviour of integrated circuits in the time-domain is proposed, that enables building ESN models that cover a wide range of operation of the modelled circuit.

A nonlinear impedance model based on the echo state network is proposed. The model enables building interchangeable behavioural models of integrated circuits in the conducted immunity simulation environment according to the IEC-62132-4 Direct RF Power Injection (DPI) standard, and it is applied to a buffered voltage reference integrated circuit that consists of three subcircuits.

An overview of nonlinear effects observed in the conducted immunity simulations of the modelled circuit is presented, and the methodology for evaluating the accuracy of the modelled time-domain waveforms is introduced. The stability of the presented behavioural models is analysed, including the DC operating point stability, the small-signal stability, and the initial transient stability.

The behavioural modelling principles are also applied to modelling applications in ESD and EMC area. A lumped-distributed model of a transmission line pulsing setup is presented, including a behavioural model of an ESD protection device that exhibits snapback. The behavioural model of an I2C pad of an industrial integrated circuit is presented that enables simulating the RF re-radiation due to RF harmonic distortion in a magnetically coupled wireless system.

Keywords: electromagnetic compatibility, behavioural modelling, echo state networks, nonlinear impedance modelling, stability analysis, direct power injection, artificial neural networks, bandgap reference, simulation speed-up, adaptive sampling, conducted immunity

Extended abstract in Croatian language: Metodologija za ponašajno modeliranje blokova integriranih sklopova za primjene u elektromagnetskoj kompatibilnosti

Obzirom na porast složenosti integriranih sklopova u poluvodičkoj industriji, elektromagnetska kompatibilnost (eng. *electromagnetic compatibility*, EMC) postala je sastavni dio procesa projektiranja i ispitivanja integriranih sklopova. Simulacije ponašanja integriranih sklopova podvrgnutih zračenim ili vođenim elektromagnetskim smetnjama visokih frekvencija i amplituda omogućuju proizvođačima integriranih sklopova smanjivanje troškova projektiranja poluvodičkih proizvoda te njihov brži plasman na tržište.

Potreba za simulacijskim modelima integriranih sklopova koji omogućuju veću brzinu simulacija uz manje memorijske zahtjeve dovela je do vrlo aktivnog istraživačkog rada na području ponašajnog modeliranja. Ponašajni modeli generiraju ponašanje integriranih sklopova koje se opaža na stezaljkama modeliranih sklopova, bez korištenja informacija o njihovom unutarnjem ustrojstvu. Na ovaj način ponašajni modeli omogućuju smanjivanje kompleksnosti simulacijskih modela te zaštitu intelektualnog vlasništva.

Integrirani sklopovi su nelinearni sustavi s memorijom jer su izlazni signali definirani kao nelinearne transformacije ulaznih signala i njihovih prethodnih vrijednosti u vremenskoj domeni. Neuronske mreže s povratnom vezom (eng. *recurrent neural networks*, RNN) su podskup umjetnih neuronskih mreža koje modeliraju nelinearne sustave s memorijom pomoću povratnih veza između neurona u jednom ili više skrivenih slojeva mreže. Glavni nedostatci RNN mreža su potencijalna nestabilnost modela te sporo vrijeme treniranja, koje se u većini metoda temelji na gradijentnom spuštanju (eng. *gradient descent*).

Predstavljeni su rezultati istraživanja iz područja izgradnje zamjenjivih ponašajnih modela (eng. *interchangeable behavioural models*) integriranih sklopova temeljenih na ESN mrežama (eng. *echo state network*) za primjene u simulacijama otpornosti sklopova na vođene smetnje. ESN mreža je podskup RNN mreža s vrlo kratkim vremenom treniranja i zajamčenom stabilnošću.

Predstavljeni ponašajni modeli ispravno modeliraju nelinearne ulazne i izlazne impedancije integriranih sklopova te zbog toga ispravno opterećuju tranzistorske sklopove s kojima su spojeni u električnoj shemi koja definira sklopovsku simulaciju (eng. *test bench*). Modeli su precizni u širokom rasponu amplituda vođenih smetnji te ispravno reproduciraju pomak statičke radne točke i pojavu harmonika višeg reda. Ovisno o modelu i primjeni, koeficijenti ubrzanja sklopovskih simulacija iznose od 2 puta do 100 puta uz zadržavanje dobre preciznosti modela.

ESN mreža uvodi se kao temeljna sastavnica za modeliranje ponašanja nelinearnih integriranih sklopova u uvjetima velikog signala. Dana je formalna matematička definicija ESN mreže s postupkom treniranja koji jamči stabilnost modela u smislu ograničenog izlaznog signala uz ograničeni ulazni signal (eng. *bounded-input bounded-output*, BIBO). Postupci za treniranje i verifikaciju ESN mreža sa slučajno odabranim povratnim vezama u skrivenom sloju koji omogućuju modeliranje općenitih vremenskih nizova prilagođeni su radi modeliranja naponskih i strujnih signala u vremenskoj domeni dobivenih simulacijama integriranih sklopova. Dana je iterativna metoda za ručno odabiranje hiper-parametara ESN mreže, uz smjernice o utjecaju pojedinog hiper-parametra na svojstva mreže.

Predstavljen je adaptivni algoritam za uzorkovanje nelinearnog ponašanja sklopova u domeni definiranoj frekvencijom i snagom smetnje koji omogućuje izgradnju skupa podataka za treniranje ESN mreže. Algoritam smješta više uzoraka u područje rada sklopa s većom nelinearnošću modeliranih valnih oblika te izbjegava nedovoljno uzorkovanje linearnog područja rada. Uvode se dva kriterija za zaustavljanje algoritma, jedan temeljen na unaprijed određenom broju uzoraka i jedan temeljen na Spearmanovoj korelaciji uzastopnih dvodimenzionalnih interpolatora skalarne funkcije nad zadanom domenom.

ESN mreža implementirana je u jeziku Verilog A, jeziku za opisivanje sklopovlja (eng. *hardware description language*, HDL), čime je omogućeno korištenje ESN mreža u komercijalnim sklopovskim simulatorima. Predstavljena metodologija za modeliranje ponašanja integriranih sklopova primijenjena je na pet praktičnih sklopova iz poluvodičke industrije: naponsko sljedilo, upravljački sklop prekidačkog izvora napajanja (eng. *DC-DC converter*), LIN sučelje, matematički oscilator s povratnom vezom te radiofrekvencijsko mješalo frekvencija (eng. *RF mixer*). Dobiveni rezultati pokazuju primjenjivost ESN mreža na modeliranje širokog raspona nelinearnog ponašanja opaženog u simulacijama integriranih sklopova. U ova ponašanja uključeni su efekti memorije sklopova, gdje su izlazni signali zakašnjeli u odnosu na ulazne signale za do tisuću vremenskih uzoraka te efekti sklopova koji sadrže dvije vrlo razmaknute vremenske konstante.

Usporedbom modela koji se temelji na ESN mreži s referentnim modelom temeljenim na RNN mreži pokazano je kako ESN mreža ostvaruje usporedivu preciznost izraženu pomoću mjere MSE (eng. *mean square error*), pri čemu se omogućuje korištenje bržeg i jednostavnijeg postupka treniranja i jamči stabilnost modela. Svojstva uopćavanja (eng. *generalization*) ESN mreža ograničena su na interpolaciju između podataka za treniranje unutar zadane domene te na ispravan odziv na trenirane ulazne signale na koje je dodan aditivni bijeli šum. U odnosu na tranzistorske modele s ekstrahiranim parazitnim elementima, ESN mreže postižu koeficijente ubrzanja sklopovskih simulacija do 77 puta. Vrijeme izvođenja sklopovskih simulacija s ESN modelima manje je ovisno o harmoničkoj distorziji modeliranih valnih oblika u vremenskoj domeni u odnosu na tranzistorske sklopove.

Predstavljena je arhitektura modela nelinearne impedancije temeljena na zavisnim naponskim i strujnim izvorima. Uvođenjem ESN mreže u modeliranje nelinearne impedancije omogućuje se izgradnja ponašajnih modela integriranih sklopova koji mogu zamijeniti tranzistorske modele, stoga se ovakvi ponašajni modeli nazivaju zamjenjivim modelima (eng. *interchangeable models*). Dana je metodologija za analizu toka signala integriranog sklopa, pri čemu su naponski i strujni signali svakog prolaza (eng. *port*) modeliranog sklopa podijeljeni u ulazne i izlazne signale ESN mreže. Ispitana su svojstva komercijalnih sklopovskih simulatora obzirom na izvršavanje simulacija otpornosti sklopova na vođene smetnje (eng. *conducted immunity simulations*), s naglaskom na simuliranje ponašanja u ustaljenom stanju (eng. *steady-state*) u vremenskoj domeni.

Arhitektura ponašajnog modela proširena je radi omogućavanja neovisnog modeliranja statičkog (eng. *direct current*, DC) i radiofrekvencijskog (eng. *radio-frequency*, RF) ponašanja modeliranog sklopa radi pojednostavljivanja postupka treniranja ESN mreže. Uvodi se blok za opažanje (eng. *monitor*) DC signala koji omogućuje odvajanje DC i RF komponenti naponskih valnih oblika u vremenskoj domeni. Dana je implementacija proširenog modela u jeziku Verilog A koja omogućuje korištenje modela u DC simulacijama te u tranzijentnim simulacijama koje započinju iz početnog uvjeta zadanog datotekom.

Predstavljeno je okruženje za simulacije otpornosti na vođene smetnje (eng. *conducted immunity simulation environment*), koje je primijenjeno na sklop naponske reference s odvojnim stupnjem (eng. *buffered voltage reference circuit*) iz postojećeg poluvodičkog proizvoda na tržištu. Odnosi između RF napona i RF struja u simulacijskom okruženju opisani su dijagramima toka svakog modeliranog podsklopa.

U navedenim simulacijama opažaju se dva dominantna nelinearna efekta: (i) harmonička distorzija RF signala (eng. *RF harmonic distortion*), (ii) pomak statičke radne točke uzrokovan RF smetnjom (eng. *RF-induced DC-shift*). Uvodi se metodologija za određivanje preciznosti ponašajnog modela temeljena na usporedbi svojstava vremenskih valnih oblika u frekvencijskoj domeni. Ova metodologija omogućuje tabličnu usporedbu ponašanja sklopova u simulacijskom okruženju gdje su jedan ili više podsklopova zamijenjeni ponašajnim modelom, omogućujući pregledan prikaz ponašanja niza RF napona i RF struja u više sklopovskih varijanti, u ovisnosti o frekvenciji i snazi RF smetnje. Predstavljen je algoritam za provođenje simulacija otpornosti na vođene smetnje prema standardu DPI (eng. *direct power injection*) kojim se minimizira potreban broj simulacija za određivanje DPI karakteristike metodom pretraživanja pomoću binarnog stabla.

Stabilnost ponašajnih modela u okruženju za simulacije otpornosti sklopova na vođene smetnje analizira se kroz tri aspekta: meta-stabilnost statičke radne točke, stabilnost u uvjetima malog signala te stabilnost početnog tranzijenta. Dana je poveznica između meta-stabilnosti i DC svojstava ESN modela izvan treniranog DC područja rada.

Izveden je dovoljan uvjet za meta-stabilnost zadanog ponašajnog modela. Uvodi se uvjet ravnoteže RF struja modeliranog sklopa te je dan primjer implicitnih veza između podsklopova kroz podlogu silicijske pločice. Razvijen je okvir za analizu interakcije između ESN mreža definiranih u disktrenoj vremenskoj domeni i tranzistorskih sklopova definiranih u kontinuiranoj vremenskoj domeni te je predstavljena metodologija za određivanje karakteristika ponašajnih modela u uvjetima malog signala.

Rješenja lineariziranih jednadžbi koja određuju frekvencijski odziv naponske reference s odvojnim stupnjem u uvjetima malog signala izvedena su na temelju frekvencijskih odziva pojedinih podsklopova. Stabilnost ponašajnog modela u ukupnom sklopu povezana je sa svojstvima modela izvan treniranog frekvencijskog područja. Dana je poveznica između početnih tranzijenata ponašajnih modela prije dostizanja ustaljenog stanja i impulsnog odziva pojedinih naponskih perturbacija u simulacijskoj shemi te koeficijenata trenirane ESN mreže u matrici izlaznih težinskih faktora.

Predstavljena je instanca ponašajnog modela odvojnog stupnja (eng. *buffer*) koja je stabilna kao zasebni element u BIBO smislu, ali unosi nestabilne polove u ukupni sklop u simulacijskoj shemi koja sadrži druge tranzistorske sklopove, zbog čega simulacija divergira. Izvedena je poveznica između frekvencijskih odziva ponašajnog modela i nestabilnih polova naponskih perturbacija u ukupnom sklopu.

Predstavljena je instanca ponašajnog modela naponske reference (eng. *bandgap*) koja je stabilna i kao zasebni element u BIBO smislu, i kao dio ukupnog sklopa u simulacijskoj shemi koja sadrži druge tranzistorske sklopove, ali unosi značajna nadvišenja u vremenskom odzivu napona pojedinih čvorova u shemi. Umjetna naponska nadvišenja mogu dovesti tranzistorske sklopove u područje rada za koje ponašajni model nije treniran. Izvedena je poveznica između naponskih nadvišenja i impulsnog odziva pridružene naponske perturbacije te svojstava trenirane ESN mreže.

Predstavljena je instanca ponašajnog modela naponske reference za DPI simulacije sklopa naponske reference s odvojnim stupnjem u frekvencijskom području od 30 MHz do 300 MHz pri RF snagama između -20 dBm i 0 dBm. Preciznost modela izražena je mjerom MSE i usporediva je s rezultatima dostupnima u literaturi.

Vrijeme izvršavanja ponašajnog modela u sklopovskoj simulaciji manje je ovisno o snazi RF smetnje u odnosu na tranzisorske sklopove. DPI karakteristika sklopa gdje je naponska referenca zamijenjena ponašajnim modelom nalazi se unutar 1 dB od DPI karakteristike tranzistorskog sklopa. Uskopojasni zamjenjivi ponašajni modeli svih triju podsklopova naponske reference s odvojnim stupnjem modeliraju rad sklopa na frekvenciji od 850 MHz pri snagama RF smetnje od -40 dBm do -2 dBm. Tri ponašajna modela ispitana su predstavljenom metodom za određivanje preciznosti modela te ispravno opterećuju tranzistorske sklopove koji su s njima spojeni.

Arhitektura modela nelinearne impedancije također omogućuje međusobno spajanje dvaju ponašajnih modela koji koriste međusobno dualne topologije modela. Pokazano je kako sva tri ponašajna modela ispravno opterećuju druge ponašajne modele u simulacijskom okruženju. Postignuti su koeficijenti ubrzanja simulacija do dva puta.

Dane su smjernice za nastavak istraživanja ponašajnog modeliranja. Jedan smjer istraživanja odnosi se na modeliranje naponske reference s odvojnim stupnjem koje u obzir uzima opterećenje odvojnog stupnja, koje zahtijeva skaliranje ponašajnih modela na više od dva ulazna signala. Drugi mogući smjer istraživanja odnosi se na modeliranje integriranih sklopova koji uz signale uzrokovane RF smetnjom sadrže i vremenski promjenljive funkcionalne signale niske frekvencije.

Predstavljena je mjerna metoda pulsiranja prijenosne linije (eng. *transmission line pulsing*, TLP) te je izveden model TLP generatora s pasivnim i distribuiranim elementima. Ponašajni model silicijski upravljanog ispravljača spregnutog s upravljačkom elektrodom n-kanalnog MOS tranzistora (eng. *gate-coupled NMOS silicon-controlled rectifier*, GCNSCR), elementa za zaštitu od elektrostatskih izboja (eng. *electrostatic discharge*, ESD) izgrađen je na temelju podataka dobivenih TLP mjerenjima. Budući da negativni dinamički otpor (eng. *snapback*) nije uključen u većinu biblioteka sklopovskih modela, ponašajni model GCNSCR elementa implementiran u jeziku Verilog A omogućuje izvršavanje TLP simulacija u vremenskoj domeni. Model ispravno modelira ponašanje elementa tijekom kvazistacionarnog stanja TLP impulsa u oba stanja provodljivosti (eng. *off-state, on-state*). Predstavljena metoda omogućuje izgradnju brzih i preciznih modela ESD elemenata s negativnim dinamičkim otporom u simulacijskom okruženju za TLP metodu.

Predstavljen je efekt reradijacije radiofrekvencijskog signala zbog harmoničke distorzije nelinearnih integriranih sklopova u magnetski spregnutom sustavu. Uzrok harmoničke distorzije povezan je s naponski ovisnim dinamičkim otporom i kapacitetom stezaljki za I2C komunikaciju. Predstavljena je metoda za određivanje naponski ovisnih vrijednosti pomoću simulacija u uvjetima malog signala (eng. *AC simulations*). Pomoću dobivenih karakteristika izgrađen je ponašajni model za simulaciju harmoničke distorzije. Ponašajni model se uspoređuje s mjerenjima metodom dipleksera (eng. *diplexer*).

Ponašajni modeli postižu koeficijente ubrzanja simulacija do 115 puta u odnosu na korištenje tranzistorskih sklopova s ekstrahiranim parazitnim elementima. Predstavljen je magnetski spregnut sustav koji se sastoji agresorske antene koja radi na 1.84 GHz, antene žrtve koja radi u WiFi pojasu na 5 GHz te od nelinearnog integriranog sklopa. Integrirani sklop prima RF smetnju koju generira agresorska antena te se na stezaljci sklopa zbog nelinearne distorzije generira treća harmonička frekvencija koja se reradijacijom šalje prema anteni žrtvi. Ponašajni model omogućuje uključivanje nelinearnog integriranog sklopa u radiofrekvencijsko simulacijsko okruženje.

Izvorni znanstveni doprinos sastoji se od tri komponente:

1. Metoda modeliranja nelinearnih sklopova u uvjetima velikog signala pomoću ESN mreža (eng. *echo state network*).
2. Adaptivni algoritam za odabir uzoraka nelinearnog ponašanja sklopova u vremenskoj domeni.
3. Metoda modeliranja nelinearne impedancije pomoću zavisnih izvora radi me đusobnog spajanja ponašajnih modela i spajanja s drugim sklopovima.

Ključni pojmovi: elektromagnetska kompatibilnost, ponašajno modeliranje, ESN mreže (eng. *echo state networks*), model nelinearne impedancije, analiza stabilnosti, DPI (eng. *direct power injection*), umjetne neuronske mreže, bandgap referenca, ubrzanje simulacija, adaptivno uzorkovanje, otpornost na vođene smetnje

Contents

Chapter 1

Introduction

The complexity of integrated circuits (IC) is growing rapidly, and electromagnetic compatibility (EMC) aware design has become the norm in the IC industry. Being able to simulate EMC behaviour of IC blocks in the design phase reduces the design cost and shortens the time-to-market. The need for more time- and memory-efficient IC models has made behavioural modelling an active research area in recent years [1–7]. In the behavioural modelling approach, the model is built using only the input-output behaviour of the modelled system, without any information about its inner physical structure, enabling model order reduction (MOR), simulation speed-up, and intellectual property (IP) protection. Different methods refer to behavioural models as macromodels [8], [9], empirical models [10], and surrogates [11].

ICs are nonlinear systems with memory, as the outputs are nonlinear transforms of the inputs and their previous values or "system history". Most behavioural modelling methods capture the system history by feeding the input and/or output signals through a delay line. Choosing the number and value of the delays is computationally expensive, involves case-specific knowledge of the modelled circuit, and often does not guarantee stability.

Recurrent neural networks (RNN) are artificial neural networks (ANN) that capture the system history using internal feedback connections between the neurons in one or more hidden layers. The main drawback of using RNNs for behavioural modelling is often slow training algorithms based on gradient descent [12], [13].

The thesis presents the study on building interchangeable behavioural models of ICs for conducted immunity simulations based on echo state networks (ESN) in combination with look-up tables and S-parameters. An ESN is a type of RNN with a very fast training procedure and guaranteed model stability [13].

The chapter is organized as follows. Section1.1presents an overview of the research area. Section1.2introduces the performed research with the original scientific contributions given in Section1.3, and Section1.4presents the outline of the thesis.

1.1 Behavioural modelling research area overview

An artificial neural network (ANN) is a behavioural model consisting of interconnected units or neurons. Each neuron is associated with an activation, a signal in the discrete time-domain that evolves based on the interaction of a neuron with other neurons in the network. The ANN activations are trained to mimic the complex relationships between the input and output signals of the modelled system in the time-domain using the training algorithms that define the connections between the neurons to fit the training data.

Many software packages for generating, training, and testing ANNs are readily available, e.g. the Neural Network Toolbox™ in MATLAB® [14]. In the computer science area, ANNs are evaluated using standard benchmark time-series prediction test cases, such as a 2nd order dynamical system [12], the NARMA series [15], or the Mackey-Glass chaotic series [13], [16], [17]. The network sizes used for these benchmark test cases are in the order of several hundred neurons [13].

ANNs are already successfully used in a variety of applications, e.g. model predictive control [18], active shunt power filters [19], [20], biomedical applications [21]. In the area of integrated circuit modelling, a 3-layer feedforward neural network is presented in [22] that models the response of a digital IC to a radio-frequency (RF) disturbance on its supply pin. The model is implemented in the circuit simulator as a mathematical expression. In [6], the model of an output buffer of a digital IC is built for signal integrity simulations. A combination of feedforward ANNs and recurrent neural networks (RNN) is used. Single-layer feedforward neural networks (SLFN) with 4 neurons are used to model the IV-characteristics of the buffer transistors, and the total buffer output current is modelled by weighting the currents of the output transistors, where the weights are implemented as recurrent neural networks with 10 neurons each. This model overcomes the limitation of using the I/O buffer information specification (IBIS) [23] that cannot properly model analog nonlinear behaviour, such as ringing and attenuation.

Most ANN training algorithms train all connections in the network using methods based on gradient descent, which often have slow convergence or do not converge at all, e.g. due to bifurcations during training [13], [24]. The echo state network (ESN) is a specific type of RNN introduced in [13], where the network is trained by generating random recurrent connections in the hidden layer, and by performing linear regression only on the weights of the readout layer. This approach makes the ESN training procedure computationally efficient and robust, while retaining the desirable properties of RNNs. The ESN models can be implemented in any hardware description language (HDL) for analog and/or mixed signals, e.g. Verilog A, VHDL-AMS, MAST [25]. The HDL implementation of ESN models makes them directly usable in commercial circuit simulators, such as Cadence® Spectre® and Mentor Graphics® Eldo.

The ESN is also used in a variety of modelling applications. In [1], the ESN model with 56 neurons is used for time-series prediction of the temperature in a hot blast stove system. In the power grid area, behavioural modelling is applied to build models of photovoltaic inverters [2] and electric vehicle battery chargers [3]. In the power electronics area, behavioural models of gallium nitride (GaN) transistors and their gate drivers are built [4], [26]. In [18] neural networks are used for the model predictive control (MPC) of an unknown nonlinear system. The ESN is used for system identification, and the control problem is formulated as a quadratic programming (QP) problem that is solved using a simplified dual neural network (SDN) with a single layer.

In [19] and [20], the ESN is used in a harmonic extraction block of a shunt active power filter (SAPF), that eliminates the higher harmonics from the output current caused by nonlinear loads in power systems. The ESN is used to extract the fundamental component of the load current. Although 100 neurons are used in [19], it is shown in [20] that an ESN with only 30 neurons is sufficient to achieve similar model accuracy, that is superior to a feedforward neural network, referred to as the multilayer perceptron (MLP). In [9] an ESN model with 30 neurons models the output current of a digital circuit as a function of the port voltage for signal integrity simulations, capturing the nonlinear RF voltage and RF current relationships observed in simulations of IC blocks.

Methodologies such as [8] are suitable for modelling circuits that operate in a small signal linear regime, while the methods such as [9], [10] model the nonlinear dependence of the currents flowing into the pins of transceiver driver circuits on the independently set voltage excitation signals. Several approaches to modelling the nonlinear behaviour of IC blocks, particularly in RF frequency bands, are presented in literature. In [3], an electric vehicle battery charger is modelled using a nonlinear model that covers different operating points by switching between several linear models. In [4], a GaN transistor gate driver is modelled by capturing the linear behaviour using IV-curves, and by capturing the nonlinear capacitance behaviour using CV-curves. In [26], the S-parameters of a GaN transistor are used to build a nonlinear model based on support vector machines (SVM). In addition to behavioural models built from simulations, behavioural models are also derived from measurements [5], [27].

In the EMC area, the RF immunity and RF emission of integrated circuits is typically measured according to standards, and root cause analysis requires recreating the measured behaviour in circuit simulations. Direct power injection (DPI) is an electromagnetic interference (EMI) conducted immunity test for integrated circuits, defined in the IEC-62132-4 standard [28]. The RF disturbance in the range between 150 kHz and 1 GHz is injected into the pin of the device-under-test (DUT) and the RF forward power is increased until the functionality of the circuit fails according to a failure criterion. It is practice during

the product development phase to run narrow-band simulations of the DPI test bench containing the transistor-level blocks at system-critical frequencies, in order to observe the RF behaviour of the circuit and to improve its conducted immunity using circuit techniques or filtering. A full electrical model of the DPI measurement setup is presented in [29], including the models of the IC package, the printed circuit board (PCB), the injection probe, and the decoupling capacitors.

The main bottleneck in the conducted immunity simulations of integrated circuits is the simulation time that increases with RF forward power levels due to the transistor-level model of the IC that is operating in an increasingly nonlinear regime. Additionally, the slow process of converging to the steady-state due to the large internal time constants of the transistor-level circuits results in long simulation times before reaching the steady-state operation.

The nonlinear modelling approaches such as [9], [10] are only valid if the RF voltage is known. The challenge in building models for DPI simulations is that the exact amplitude of the RF voltage injected into the DUT depends on the nonlinear input impedance seen looking into the DUT pin under test, and it is not known upfront [11], [28].

This issue is addressed in [11], where a behavioural model of a voltage regulator integrated circuit is built to improve the simulation time of the DPI harmonic balance simulations. The behavioural model, referred to as a surrogate, is based on a feed-forward neural network (FFNN) with two hidden layers implemented as an analytical expression. In order to properly load the DPI injection network consisting of a 50-Ω RF generator and a bias-tee, two FFNN models generate the numerical value of the DC resistance R_{IN} and the complex-valued small-signal impedance Z_{IN} as functions of the numerical values of the frequency and the amplitude of the RF disturbance voltage seen at the input pin. This enables the harmonic balance simulator to find the correct solution for the RF voltage amplitude seen at the pin of the modelled IC. A third FFNN model generates the DC value of the output voltage as a function of the same two input variables using an ideal DC voltage source. The training time is in the order of 5 hours, slowing down the process of optimising the hyper-parameters of the model [11].

The behavioural modelling methodologies presented in literature include an implicit or explicit step of design space sampling to obtain the training dataset for building the model. Several adaptive sampling algorithms are evaluated in [30], which combine the exploration sampling strategy that aims at uniformly sampling of the design space, and the exploitation strategy that aims at choosing more samples in the areas where the model accuracy is lower. The LOLA-Voronoi algorithm, introduced in [31], combines both sampling strategies, and it is shown to be superior to random sampling in the case of modelling the input noise current of a low noise amplifier (LNA). In [32], the LOLA-Voronoi algo-

rithm is used in a metamaterial geometry optimisation method to significantly reduce the required computing time by limiting the size of the dataset. In [11], the training dataset is obtained by sampling the RF design space defined by the RF frequency and RF forward power using the LOLA-Voronoi algorithm, in order to put more focus on the more nonlinear regions of the design space, where the circuit functionality starts to fail.

The original research presented in this thesis is performed within the context of the behavioural modelling of nonlinear effects in integrated circuits. The research is focused on building behavioural models of integrated circuits derived from circuit simulation data, which are able to correctly load the transistor-level circuits in the time-domain simulations.

The modelling approach introduced in [11] models the DC resistance and the small-signal impedance of the modelled circuit, and it is appropriate for the loading of linear networks, such as the DPI injection network. In order to enable the loading of other transistor-level circuits, the approach in [11] is modified in three ways. Firstly, the nonlinear input impedance is modelled using recurrent neural networks instead of feed-forward neural networks, in order to enable modelling the nonlinear and memory properties of the IC impedances. Secondly, instead of modelling the impedance components (i.e. the DC resistance R and the small-signal impedance Z) as functions of the RF frequency and RF amplitude, the time-domain waveform of the RF input current is modelled as a function of the RF input voltage. Thirdly, the model of the output voltage in [11] is extended to include the output impedance instead of an ideal voltage source.

1.2 Overview of the performed research

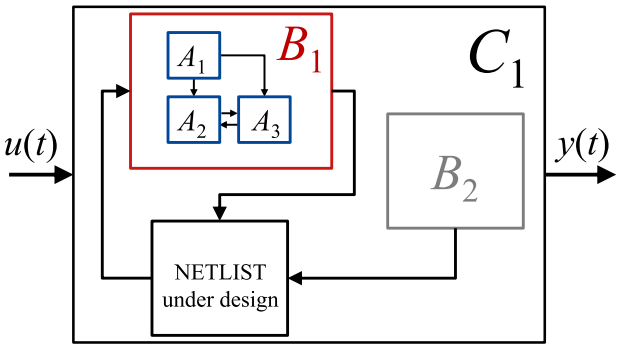


Figure 1.1: The interchangeable behavioural modelling concept presented on an example simulation test bench with three hierarchical levels A, B, C.

A behavioural model is interchangeable if the time-domain voltages and currents at the pins of the modelled transistor-level circuit remain unchanged when the modelled circuit is replaced by the behavioural model. Fig.1.1presents an example simulation test bench with three hierarchical levels labelled as A, B, C. The circuit C_1 consists of three interconnected subcircuits: B_1, B_2, and a netlist under design. The subcircuit B_1 represents a power management circuit that provides the supply voltage to the netlist under design. The subcircuit B_1 consists of three interconnected subcircuits A_1, A_2, A_3. The top-level circuit C_1 is simulated in the conducted immunity simulation test bench, where the RF interference signal $u\,(t)$ is injected into the C_1 supply pin, and its effect on the C_1 output signal $y\,(t)$ is observed within the RF design space defined by the frequency and amplitude of the RF interference.

Since the conducted immunity simulations of power management circuits can be very slow [11], the iterative process of implementing EMC-aware design techniques into the netlist under design becomes time-consuming, increasing the product development costs and the time-to-market. In order to speed-up the conducted immunity simulations, the power management circuit B_1 is replaced by an interchangeable behavioural model that replicates the behaviour of the modelled circuit B_1 under the given RF interference injection conditions and also reduces the complexity of the simulation test bench. The model of B_1 is built by connecting the behavioural models of its three subcircuits A_1, A_2, A_3.

The topic of the research presented in this thesis is the methodology for building interchangeable behavioural models that are used in the conducted immunity simulation environment. The models are able to correctly load the connected transistor-level circuits or other behavioural models by modelling the nonlinear impedance seen at the input and output pins of the modelled circuit. Due to the favourable properties presented in Section1.1, most importantly the fast training time of the model, the echo state network is chosen as the basis for the proposed behavioural modelling approach.

A Python library is developed that includes the tools required to perform the research. The Python module for generating and training ESN models is based on [13]. The Python module includes a Verilog A code generator that enables the use of the ESN models in the Cadence® Spectre® circuit simulator. The circuit simulations are run using the Python module that controls the circuit simulator, and enables sweeping the values of the RF frequency and RF forward power variables in the simulation. The resulting simulation outputs, consisting of DC values, time-domain waveforms, frequency domain spectra, and meta-data such as log files, are stored using [33] into SQL databases that are searchable by the RF frequency and RF forward power parameters for data post-processing.

The nonlinear and memory effects observed in the simulations of a range of integrated circuits are investigated. In [34], the ESN is applied to the modelling of the time-domain responses of a DC-DC driver IC and a LIN interface circuit, that exhibit long delay times between changes in the input and output signals due to the memory effects of the modelled ICs. The RF mixer modelling test case in [34] exhibits widely separated time-constants that are captured by the ESN model. In [35], the influence of the phase relationship between the RF interference signal and a low frequency functional signal on the conducted immunity of a non-inverting amplifier is analysed. In [36], a bandgap reference circuit is modelled, that exhibits RF-induced DC-shift of the bandgap voltage with increasing RF forward power in the DPI test bench due to nonlinear rectification.

The time-domain waveforms used for building the ESN model in [36] are collected by uniform sampling of the RF design space defined by the frequency and forward power of the RF interference signal. The drawback of this exploration sampling strategy is that the number of samples required to properly sample the nonlinear regions of the circuit may increase significantly. In [37], an adaptive sampling algorithm is proposed for sampling the nonlinear circuit behaviour in the time-domain. The presented algorithm is based on the LOLA-Voronoi algorithm [11], [31], taking into account the nonlinearity of the observed time-domain waveforms, and it enables accurate modelling of nonlinear circuits at high forward power levels of the RF disturbance using a lower number of samples.

In [38], the ESN modelling methodology proposed in [34] and [36] is extended to enable building interchangeable behavioural models of an industrial buffered voltage reference circuit consisting of three subcircuits. The models preserve the RF voltages and RF currents observed in the time-domain simulation of the top-level test bench where each modelled transistor-level subcircuit is replaced by its behavioural model. The ESN model reproduces not only the DC value of the output voltage as in [11], but also the time-domain voltages and currents observed at the pins of the modelled circuit, including the RF-induced DC-shift. The nonlinear input and output impedances are modelled in the RF conditions using the ESN with controlled sources in a feedback loop [38].

The stability of behavioural models in circuit simulators is defined by: (i) the stability of the ESN model, and (ii) the stability of the feedback loop defined by the ESN model and the controlled sources in the nonlinear impedance model. The bounded-input bounded-output (BIBO) stability of the recurrent connections in the hidden layer of the ESN models is based on the existence of the echo state property [13]. The methods for generating linearized ESN models with guaranteed BIBO stability are presented in [34], [38], [39], and the model stability is verified in [9], [40] by analysing the eigenvalues of the ESN model in the complex z-domain.

In [38], [41] the stability of the DC operating point stability of the ESN model in the DC simulations is analysed. The root causes for DC operating point instability are linked to the DC behaviour of the ESN model outside of the trained DC range. In order to simplify the model building procedure, the nonlinear impedance model architecture is extended to enable modelling the DC and RF behaviour independently.

In [42], the stability of the feedback loop in the nonlinear impedance model is analysed in the discrete time-domain, and a method for obtaining the poles of the resulting discrete-time system using the frequency response using optimization based on the Cauchy integral is proposed, based on [43]. In [38], the small-signal stability is analysed in the continuous time-domain, and the stability discussion is generalized to include the influence of the ESN model outside of the trained RF frequency range on the stability of the initial transients in the time-domain simulations.

The principles derived in this research have been applied to the building of behavioural models in ESD and EMC area. In [44], a behavioural model of an ESD protection device that exhibits snapback is built for simulations of the transmission line pulsing (TLP) test. In [45], the RF harmonic distortion of an I2C pin of an integrated circuit is modelled for the analysis of the re-radiated RF disturbance in a magnetically coupled wireless system. Both test cases demonstrate the ability of behavioural models to reproduce highly nonlinear behaviour of integrated circuits.

1.3 Original scientific contribution

The original scientific contribution presented in the thesis consists of three components:

1. Modelling method for nonlinear circuits in large signal operating conditions using the echo state networks.
2. Adaptive algorithm for sampling nonlinear circuit behaviour in the time-domain.
3. Nonlinear impedance modelling method based on controlled sources for behavioural model interconnectivity.

1.4 Thesis outline

The thesis is organized into five chapters and four appendices as follows.

Chapter2presents the echo state network as a nonlinear discrete-time element for modelling the relationships between the time-domain signals observed in integrated circuit simulations, including the mathematical definition, the training and verification procedures, the stability analysis, and the hyper-parameter selection guidelines. An adaptive algorithm is proposed for sampling the large-signal nonlinear behaviour of integrated circuits over the design space defined by the RF frequency and RF forward power in the conducted immunity simulation environment. The proposed methodology is applied to five modelling test cases of integrated circuits.

Chapter3presents the nonlinear impedance model architecture based on the echo state network with controlled voltage and current sources in a feedback loop. An overview of nonlinear effects in the conducted immunity simulation environment is given, a method for evaluating the model accuracy over the RF design space is proposed, and an algorithm for DPI simulations using binary search is presented. The stability of the behavioural models is analysed and sufficient conditions for model stability in the top-level test bench are derived. The proposed methodology is applied to an industrial buffered voltage reference integrated circuit by simulating various combinations of transistor-level and ESN model representations of the subcircuits.

Chapter4presents behavioural modelling applications in ESD and EMC area. A lumped-distributed model of a transmission line pulsing setup is presented, including a behavioural model of an ESD protection device that exhibits snapback. The behavioural model of the I2C pad of an industrial integrated circuit is presented that enables simulating the RF re-radiation due to RF harmonic distortion in a magnetically coupled system.

Chapter5concludes the thesis.

AppendixApresents the implementation of the behavioural model of a generic 2-port circuit in the hardware description language Verilog A, including the DC look-up table, the ESN model, and the ESN rescaling block.

AppendixBpresents the analysis of the small-signal behaviour of the transistor-level buffered voltage reference circuit, including the frequency responses of each subcircuit and the associated transfer functions. The closed-form solutions for each perturbation voltage and current in the conducted immunity simulation test bench are derived.

AppendixCpresents the analysis of the influence of the phase relationship between the RF interference and the functional signal on the DPI characteristics of an operational amplifier in the non-inverting configuration through the output reflection coefficient.

AppendixDpresents the methodology for determining the poles of a discrete-time system based on its frequency response using global optimization of the Cauchy integral.

Chapter 2

Modelling large-signal nonlinear circuit behaviour using echo state networks

2.1 Motivation

The echo state network (ESN) is presented as the building block for the behavioural modelling of nonlinear integrated circuits. The properties of the ESN models are investigated with focus on modelling the relationships of time-domain signals observed in integrated circuit simulations, which are characterized by memory effects and by widely separated time-constants. An adaptive algorithm for sampling the nonlinear behaviour of integrated circuits in the time-domain is presented, that enables building ESN models that cover a range of operation of the modelled circuit. The presented modelling methodology is applied to five modelling test cases.

The chapter is organized as follows. Section2.2presents the definition of the echo state network with the conditions for the bounded-input bounded-output (BIBO) stability, and the generic ESN training and verification procedures for time-series modelling. Section2.3presents the methodology for modelling nonlinear circuit behaviour consisting of multiple time-domain waveforms obtained by circuit simulations using the ESN, and the adaptive algorithm for sampling the nonlinear circuit time-domain behaviour that enables automating the construction of the training dataset. Section2.4presents five modelling test cases that demonstrate the ability of the ESN to capture the nonlinear relationships between time-domain signals observed in simulations of various integrated circuit blocks. The presented results are discussed in Section2.5, and Section2.6summarizes the chapter. The research from this chapter is presented in [34], [37].

2.2 Echo state networks

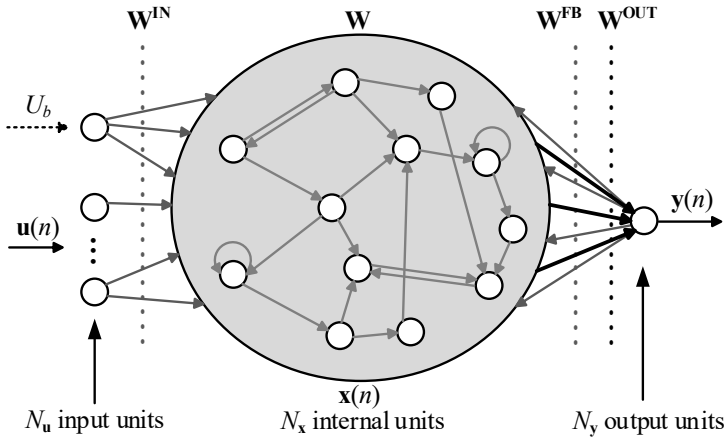


Figure 2.1: Generic diagram of the echo state network [34].

The echo state network (ESN) is a type of recurrent neural network (RNN) first proposed in [13]. Referring to Fig.2.1, the ESN consists of N_u input units in the input layer, N_x internal units in the hidden layer, and N_y output units in the output layer. Each unit, or neuron, is associated with an activation signal in the discrete time-domain that is defined by the recurrent connections between the units in the input, output, and hidden layers of the network. The connections from the input units to the internal units are defined by the input weight matrix $\mathbf{W^{IN}}$, the recurrent connections between the internal units are defined by the internal weight matrix $\mathbf{W}$, and the feedback connections from the output units to the internal units are defined by the output feedback weight matrix $\mathbf{W^{FB}}$. The output unit activations are constructed from the activation signals available in the input and hidden layers using the connections defined by the output weight matrix $\mathbf{W^{OUT}}$.

Unlike the training procedures of general recurrent neural networks, where all connections in the RNN are trained using slow training algorithms based on gradient descent, the idea behind the ESN is to train only the connections from the input and internal units to the output units of an ESN instance with randomly generated recurrent connections in the hidden layer, significantly reducing the complexity of the training procedure. The validity and the bounded-input bounded-output (BIBO) stability of this modelling approach is based on the echo state property, which states that the influence of the input sequence on the internal unit activations fades away exponentially in time. In this way, the internal unit activations become nonlinear "echoes" of the input data sequence fed to the input units, and the ESN retains the memory of the previous input signal values in its hidden layer. A sufficient condition to guarantee the echo state property of a randomly generated ESN is derived and proven in [39]. The formal mathematical definition of the ESN as a discrete-time system and the BIBO stability analysis are presented next.

2.2.1 ESN definition in the discrete time-domain

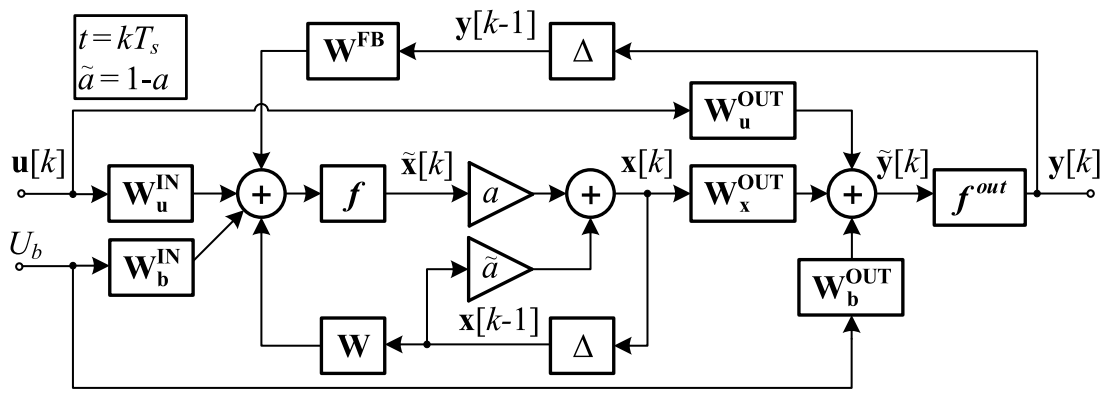


Figure 2.2: The signal flow-diagram of the echo state network as a discrete-time system with the constant sampling time T_s and the leaky integrator neuron model defined by the leaking rate a.

Fig.2.2presents the ESN as a discrete-time system with the constant sampling time T_s. The vector $\mathbf{u}\left[k\right] \in \mathbb{R}^{N_\mathbf{u}}$ is the input unit activation vector that contains the instantaneous values of the $N_\mathbf{u}$ input signals at the moment $t = kT_s$, and the signal U_b is a time-constant bias term. The bias term U_b and the input signal vector $\mathbf{u}\left[k\right]$ define the extended input signal vector $\tilde{\mathbf{u}}\left(n\right) = \left[U_b; \mathbf{u}\left[k\right]\right] \in \mathbb{R}^{N_\mathbf{b}+N_\mathbf{u}}$ by concatenation, where $N_\mathbf{b} \in \{0, 1\}$ indicates if the bias-term U_b is used or not. The vector $\mathbf{x}\left[k\right] \in \mathbb{R}^{N_\mathbf{x}}$ is the internal unit activation vector that contains the instantaneous values of the $N_\mathbf{x}$ activation signals within the hidden layer, and the vector $\mathbf{y}\left(n\right) \in \mathbb{R}^{N_\mathbf{y}}$ is the output signal vector that contains the instantaneous values of the $N_\mathbf{y}$ output signals. At each time-step k, the internal unit activation update vector $\tilde{\mathbf{x}}\left[k\right] \in \mathbb{R}^{N_\mathbf{x}}$ is defined by the update equation given in Eq. (2.1):

$$\tilde{\mathbf{x}}\left[k\right] = f\left(\mathbf{W}^{\mathbf{IN}}\tilde{\mathbf{u}}\left[k\right] + \mathbf{W}\mathbf{x}\left[k-1\right] + \mathbf{W}^{\mathbf{FB}}\mathbf{y}\left[k-1\right] + \mathbf{v}_\sigma\left[k\right]\right) \tag{2.1}$$

where f is the nonlinear activation function of the internal units, typically the hyperbolic tangent tanh, as in [13]. The matrices $\mathbf{W}^{\mathbf{IN}} \in \mathbb{R}^{N_\mathbf{x}\times(N_\mathbf{b}+N_\mathbf{u})}$, $\mathbf{W}^{\mathbf{FB}} \in \mathbb{R}^{N_\mathbf{x}\times N_\mathbf{y}}$ are the input and output feedback weight matrices that define the connections from the input and output units to the internal units. The recurrent connections between the internal units in the hidden layer are defined by the internal weight matrix $\mathbf{W} \in \mathbb{R}^{N_\mathbf{x}\times N_\mathbf{x}}$. The vector $\mathbf{v}_\sigma\left[k\right] \in \mathbb{R}^{N_\mathbf{x}}$ is a white noise term with the variance σ that is used as a regulariser for the internal unit activation update vector. The internal units use the "leaky integrator" neuron model defined in [13], where the internal state vector $\mathbf{x}\left[k\right]$ is defined using the leaking rate $a \in (0, 1]$ as a linear combination of its value $\mathbf{x}\left[k-1\right]$ in the previous time-step, and the update vector $\tilde{\mathbf{x}}\left[k\right]$, according to Eq. (2.2):

$$\mathbf{x}\left[k\right] = a\tilde{\mathbf{x}}\left[k\right] + \left(1-a\right)\mathbf{x}\left[k-1\right] \tag{2.2}$$

The extended input signal vector $\tilde{\mathbf{u}}[k]$ and the internal unit activation vector $\mathbf{x}[k]$ define the collected states vector $\mathbf{z}[k] = \left[U_b; \mathbf{u}[k]; \mathbf{x}[k]\right] \in \mathbb{R}^{N_\mathbf{b}+N_\mathbf{u}+N_\mathbf{x}}$ by concatenation. Optionally, the collected states vector can be augmented by concatenating additional input and internal unit activation vector transforms obtained using the augmented activation function f^{aug}, resulting in $\mathbf{z}[k] = \left[U_b; \mathbf{u}[k]; \mathbf{x}[k]; f^{aug}\left(\mathbf{u}[k]\right); f^{aug}\left(\mathbf{x}[k]\right)\right] \in \mathbb{R}^{N_\mathbf{b}+2N_\mathbf{u}+2N_\mathbf{x}}$. The typical augmented activation function f^{aug} is the square function, as in [13]. The output unit activation vector $\mathbf{y}[k]$ is defined by the output equation given in Eq. (2.3):

$$\mathbf{y}[k] = f^{out}\left(\mathbf{W}^{\mathbf{OUT}}\mathbf{z}[k]\right) \tag{2.3}$$

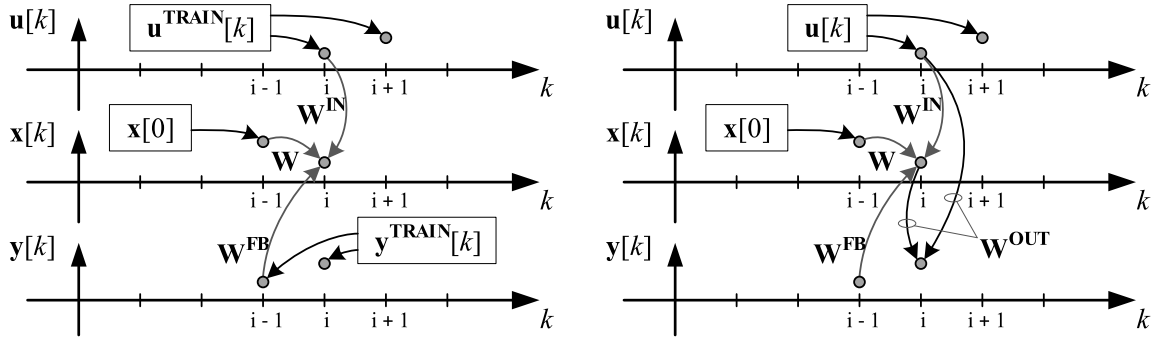
where f^{out} is the output unit activation function, typically the identity function, as in [13], and the matrix $\mathbf{W}^{\mathbf{OUT}} \in \mathbb{R}^{N_\mathbf{y}\times(N_\mathbf{b}+N_\mathbf{u}+N_\mathbf{x})}$ is the output weight matrix.

For a given ESN instance, the input weight matrix $\mathbf{W}^{\mathbf{IN}}$ and the output feedback weight matrix $\mathbf{W}^{\mathbf{FB}}$ are generated randomly using the values from user-selected distributions, typically the uniform distribution in $[-1, 1]$, as in [13]. The BIBO stability of the recurrent connections in the hidden layer is based on the existence of the echo state property of a given ESN model instance. According to the sufficient condition derived and proven in [39], the echo state property is guaranteed if the internal weight matrix $\mathbf{W}$ is diagonally Schur stable. This is achieved by randomly generating an initial matrix $\tilde{\mathbf{W}} \in \mathbb{R}^{N_\mathbf{x}\times N_\mathbf{x}}$ with all positive entries, determining its spectral radius $\tilde{r}$, and globally rescaling it to any spectral radius $r < 1$ using Eq. (2.4):

$$\mathbf{W} = \tilde{\mathbf{W}}\frac{r}{\tilde{r}} \tag{2.4}$$

Finally, the signs of randomly selected entries in $\mathbf{W}$ are changed in order to obtain negative entries. During the training and the execution of a given ESN instance, the weight matrices $\mathbf{W}^{\mathbf{IN}}$, $\mathbf{W}$, $\mathbf{W}^{\mathbf{FB}}$ remain unchanged, while the output weight matrix $\mathbf{W}^{\mathbf{OUT}}$ is trained to generate the correct output signals from the activation signals available in the hidden layer using training algorithms based on linear regression. The ESN training and verification procedures are presented next.

2.2.2 ESN training and verification procedures



(a) ESN training. (b) ESN verification.

Figure 2.3: Graphical representation of the ESN training and verification procedures [34].

The ESN training procedure is presented in Fig.2.3a. The training dataset consists of the sequence of the desired instantaneous output training values $\mathbf{y}^{\mathbf{TRAIN}}[k] \in \mathbb{R}^{N_\mathbf{y}}$ that is associated with the sequence of the input training values $\mathbf{u}^{\mathbf{TRAIN}}[k] \in \mathbb{R}^{N_\mathbf{u}}$ for the discrete-time steps $k = 1, \ldots, T$, where T is the training period in the discrete time-domain. The values of the input and output training sequences over the training period T are collected in the training matrices $\mathbf{U}^{\mathbf{TRAIN}} \in \mathbb{R}^{N_\mathbf{u} \times T}$ and $\mathbf{Y}^{\mathbf{TRAIN}} \in \mathbb{R}^{N_\mathbf{y} \times T}$. During the ESN training procedure, the input units are driven by the input training sequence $\mathbf{u}^{\mathbf{TRAIN}}[k]$, and the internal unit activations $\mathbf{x}$ are updated starting from a random initial value $\mathbf{x}[0]$. If the feedback connections from the output units to the internal units are used, the output units are driven by the desired output sequence $\mathbf{y}^{\mathbf{TRAIN}}[k]$. In order to allow the influence of the random initial condition on the internal unit activations to fade away according to the echo state property, a number of initial time-steps is discarded. The values of the resulting collected state vector sequence $\mathbf{z}[k]$ over the discrete-time steps $n = 1, \ldots, T'$ are collected in the design matrix $\mathbf{Z} \in \mathbb{R}^{(N_\mathbf{b}+N_\mathbf{u}+N_\mathbf{x}) \times T'}$, where T' is the training period after the initial discard period. The output weight matrix $\mathbf{W}^{\mathbf{OUT}}$ is calculated by solving the linear regression problem given in Eq. (2.5):

$$\mathbf{Y}^{\mathbf{TRAIN}} = \mathbf{W}^{\mathbf{OUT}}\mathbf{Z}, \tag{2.5}$$

where the output weight matrix $\mathbf{W}^{\mathbf{OUT}}$ is the unknown that determines the model output signal vector sequence $\mathbf{y}[k] \in \mathbb{R}^{N_\mathbf{y}}$ from the collected state vector sequence $\mathbf{z}[k]$ according to the output equation Eq. (2.3). The optimal solution for $\mathbf{W}^{\mathbf{OUT}}$ minimises an error measure $E\left(\mathbf{y}[k], \mathbf{y}^{\mathbf{TRAIN}}[k]\right)$ over the training period, where the error measure E is determined by the selected regression method used for solving Eq. (2.5), and it largely determines the properties of the resulting echo state network. Most researchers use ridge regression [13], also known as regression with Tikhonov regularization, to find the opti-

mal $\mathbf{W^{OUT}}$, as given in Eq. (2.6):

$$\mathbf{W^{OUT}} = \mathbf{Y^{TRAIN}}\mathbf{Z}^{\top}\left(\mathbf{Z}\mathbf{Z}^{\top} + \beta\mathbf{I}\right)^{-1}, \tag{2.6}$$

where β is the regularization coefficient, $\mathbf{I}$ is the identity matrix, and $\square^{-1}$ is the matrix inversion operator. In the special case with $\beta = 0$, Eq. (2.6) becomes the solution of a linear regression problem that minimises the L2-norm of the model error. Adding the white noise term $\mathbf{v}_{\sigma}[k]$ as an additional regulariser in Eq. (2.1) during the ESN training procedure, as suggested in [13], is shown to improve the stability and the generalisation properties of the trained ESN and results in the output coefficients with lower values that reduce the over-fitting of the model to the training dataset. The linear regression methods based on minimising the L1-norm are shown to drive most output weights to zero [46]. This is a desirable mathematical property, as it enables reducing an initially large network to a more compact size. The presented training algorithm is an offline method, because the output weights are calculated after driving the ESN with the full training dataset. Online training methods that dynamically update the output weights while the network is being driven by the training dataset are not considered in this work.

The verification process of a trained ESN is shown in Fig.2.3b. The input units of the trained ESN are driven by the input sequence $\mathbf{u}[k]$ from the verification dataset. The ESN produces the output sequence $\mathbf{y}[k]$ based on the output equation Eq. (2.3), and it is compared to the desired output sequence $\mathbf{y^{TRAIN}}[k]$ using any error measure E, typically the mean-square error (MSE), as defined in Eq. (2.7):

$$\mathbf{MSE}\left(\mathbf{y}[k], \mathbf{y^{TRAIN}}[k]\right) = \sum_{k=1}^{N_{test}} \left(\mathbf{y}[k] - \mathbf{y^{TRAIN}}[k]\right)^2 \tag{2.7}$$

where N_{test} is the number of discrete-time samples in the verification dataset, the vector $\mathbf{MSE} \in \mathbb{R}^{N_{\mathbf{y}}}$ contains the mean square error for each output signal, and the squaring operation is performed element-wise on the difference vector.

The presented ESN training procedure for reproducing the output discrete-time series $\mathbf{y}[k]$ as a function of the given input discrete-time series $\mathbf{u}[k]$ is the basis for defining the methodology for modelling integrated circuit behaviour observed in time-domain simulations that is presented next.

2.3 Method for modelling circuit time-domain behaviour

The proposed method for modelling the time-domain behaviour of integrated circuits using echo state networks is presented in Fig.2.4.

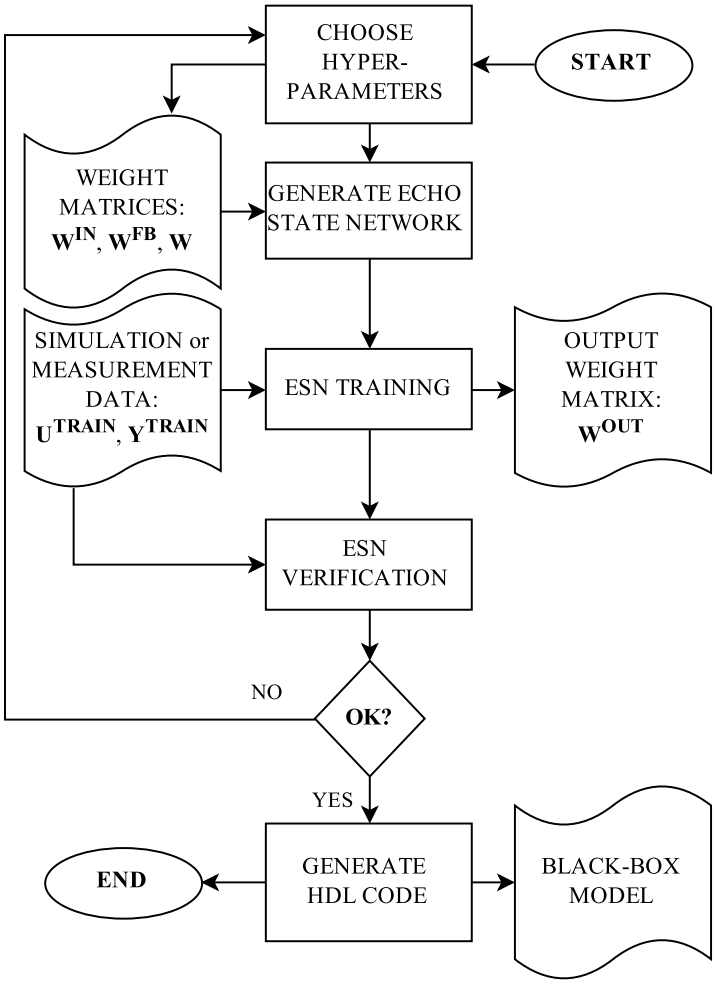


Figure 2.4: The proposed method for modelling simulated or measured behaviour of integrated circuits in the time-domain using echo state networks [34].

The ESN hyper-parameters are selected using the guidelines given in Section2.3.1, and a BIBO stable ESN model is generated using the procedure presented in Section2.2.1. The ESN model is trained according to the ESN training procedure given in Section2.2.2 using the simulated or measured data covering the desired operating range of the model, obtained either by uniform sampling, or using the adaptive sampling algorithm presented in Section2.3.2. In order to test its interpolation properties, the trained ESN model is tested using the verification dataset containing time-domain signals not included in the training dataset. The procedure is repeated with modified hyper-parameters until acceptable ESN model accuracy is achieved, and the final ESN model is implemented in any hardware description language using the procedure in Section2.3.3.

2.3.1 ESN hyper-parameter selection

ESN hyper-parameters are the network parameters that define the common properties of ESN instances that are built by iteratively generating the random recurrent connections in the ESN hidden layer. The guidelines for the selection of each hyper-parameter presented below are based on the research published in [9], [13], [21], [34], [36], [37]. Within the scope of this work, all hyper-parameters are set manually, and optimized by iterative trials that are enabled by the fast training procedure of the ESN.

The hyper-parameters related to the echo state network topology are: the number of internal units N_x in the hidden layer, the spectral radius r, the leaking rate a, the internal unit activation function f, the output unit activation function f^{out}, and the augmented activation function f^{aug}.

The number of internal units N_x should be small enough to prevent the ESN over-fitting the training dataset. An over-fitted ESN is characterized by very large coefficients in the output weight matrix $\mathbf{W^{OUT}}$, that enable modelling the training dataset with high accuracy, but with poor interpolation between the trained data points [39]. Within this work, most ESN models use up to 15 internal units, and the largest ESN uses 60 internal units. The spectral radius r determines the properties of the input signal "echoing" in the hidden layer, and it is set to values between 0.8 and 0.99 for the circuit applications presented in this work. The leaking rate a is used to "smooth-out" the ESN response, by reusing the internal unit activations from the previous time-step in the update equation of the neurons in the hidden layer. The modelling results presented in this work demonstrate that the leaking rate a is a useful knob in building the ESN models that capture sinewave-shaped waveforms observed in conducted immunity simulations, with values between 0.07 and 1. The typical internal unit activation function f used in this work and in literature is the hyperbolic tangent tanh, that has a linear characteristic around zero appropriate for modelling the RF voltage and RF current waveforms with low amplitude, while the modelled signals with higher amplitude use the more nonlinear regions of the tanh function. The output unit activation function f^{out} and the augmented activation function f^{aug} are typically not used in the modelling of integrated circuit behaviour.

The hyper-parameters related to the weight matrices of the echo state network are the distribution limits of the coefficients in the weight matrices and the bias-term U_b. The randomly generated weight matrix coefficients are typically selected from the uniform distribution between -1 and 1. The bias-term U_b enables adding a random bias level to each internal unit activation through the input weight matrix coefficients related to the bias-term, allowing different neurons to model different regions of nonlinearity. Typical values of the bias-term U_b are between 0 and 1, depending on the nonlinearity of the modelled time-domain signals.

The hyper-parameters related to the training procedure are the uniform sampling time T_s, the variance σ of the additive white noise term $\mathbf{v}_\sigma[k]$ in Eq. (2.1), the length T of the training dataset, the linear regression method used to solve the optimization problem in Eq. (2.5), the ridge regression coefficient β in case linear regression is run using the ridge regression method based on Eq. (2.6).

The signals obtained by circuit simulations are non-uniformly sampled time-domain waveforms. Since the ESN is a discrete-time system, the modelled waveforms are interpolated to a uniform sampling time T_s, that is for the Nyquist frequency required by the bandwidth of the modelled signals. The sampling times used in the presented work depend on the application, and vary from 0.5 ps for very fast signals up to 100 ps for slower signals. The values of the variance σ of the additive white noise regulariser term are chosen to be several orders of magnitude lower than the amplitude of the modelled signals, typically below $5{\cdot}10^{-4}$.

The training period T is used to set weighting factors on the time-domain waveforms in the training dataset that have a wide range of amplitudes, in order to avoid the waveforms with larger amplitudes dominating over the waveforms that have lower amplitudes in the overall model error measure E used to train the ESN. By increasing the training period of the waveforms with lower amplitudes, approximately equal weighting between all RF waveforms can be achieved in the training dataset.

The methods used for linear regression include different implementations of the L2 or L1 norm minimisation of the model error available in the scientific packages in Python. Additional hyper-parameters related to the special properties of the hidden layer are the connectivity factor that determines the sparsity of the connections in the hidden layer, the limitation of the input weight matrix coefficients to the two extreme values defined by the coefficient distribution limits, and setting the selected connections from the input units directly to the output units to zero [13]. These hyper-parameters have more application in the computer science applications of the ESN, rather than the circuit modelling applications.

The final group of hyper-parameters is related to the rescaling of the time-domain signals observed in integrated circuit simulations that are fed to the ESN model. The voltages and currents observed in circuit simulations often have DC values and amplitudes of widely different orders of magnitude. The modelled signals are therefore rescaled to a normalized range defined for each ESN input and output signal as follows. Referring to Fig.2.5, the input signal u is rescaled from the range $[u_{min}, u_{max}]$ defined by the input signals in the training dataset to the rescaled value u_r in the range $[u_{r\_min}, u_{r\_max}]$, and it is fed to the ESN as an input signal. The ESN output signal y_r is rescaled from the normalized range $[y_{r\_min}, y_{r\_max}]$ to the restored value y in the range $[y_{min}, y_{max}]$ defined

by the output signals in the training dataset. The input and output signals are rescaled using the expressions in Eq. (2.8):

$$\begin{aligned} u_r &= (u - u_{min}) \cdot \frac{u_{r\_max} - u_{r\_min}}{u_{max} - u_{min}} + u_{r\_min} \\ y &= (y_r - y_{r\_min}) \cdot \frac{y_{max} - y_{min}}{y_{r\_max} - y_{r\_min}} + y_{min} \end{aligned} \tag{2.8}$$

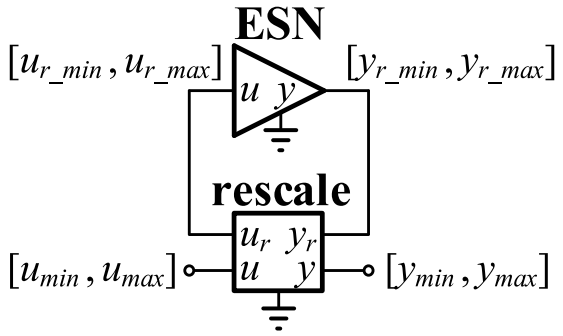


Figure 2.5: Echo state network with the rescaling block.

The typical values of the rescaled ranges are $[-1, 1]$ for more nonlinear datasets, which enables reaching the nonlinear regions of the tanh activation function, and $[-0.1, 0.1]$ for more linear datasets. The implementation of the rescaling block in the hardware description language Verilog A is given in AppendixA.

2.3.2 Adaptive algorithm for sampling nonlinear circuit behaviour

Using a single ESN model to capture the time-domain behaviour of an integrated circuit block within a given range of operation requires building a training dataset that consists of a representative series of time-domain waveforms. These waveforms are obtained by running time-domain simulations of the modelled circuit at the selected simulation conditions within the design space defined by one or more variables. In the context of conducted immunity simulations according to the Direct RF Power Injection (DPI) standard [28], the two-dimensional design space for selecting the time-domain waveforms included in the training dataset is defined by the frequency f_{RF} and forward power P_{RF} of the radio-frequency (RF) disturbance signal that is injected into the circuit under test, [11], [36] [37]. If the (f_{RF}, P_{RF}) design space is sampled uniformly, as in [36], the model error tends to be non-uniform across the design space, due to the varying nonlinearity of the modelled circuit. In order to enable building a training dataset that has a more uniform model error over the design space by placing more samples into the more nonlinear regions of the given design space, the adaptive sampling algorithm shown in Fig.2.6is proposed as

follows. The test case comparing the presented adaptive sampling algorithm to uniform sampling is presented in Section2.4.1.

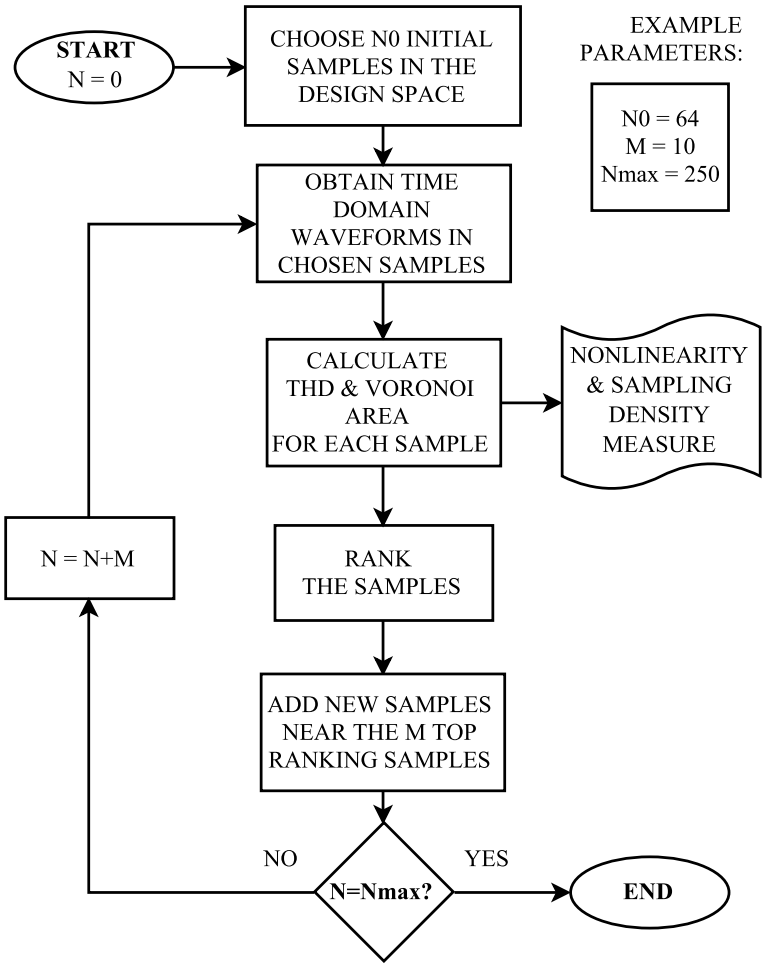


Figure 2.6: Flow chart of the proposed adaptive algorithm for sampling the nonlinear circuit behaviour in the time-domain [37].

An initial set of N_0 samples in the (f_{RF}, P_{RF}) design space is selected either uniformly, randomly, or using the latin hypercube design, as in [11]. The time-domain waveforms corresponding to the chosen samples are obtained by time-domain simulations of the modelled circuit. The nonlinearity of each sample is quantified using the total harmonic distortion (THD) as a scalar figure of merit:

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1} \tag{2.9}$$

where V_1 is the amplitude of the fundamental frequency component of the modelled time-domain waveform, and the terms $V_k, k \in \{2, 3, \dots\}$ are its higher order harmonics obtained using the fast Fourier transform (FFT). The design space is divided into sub-regions containing a single sample using Voronoi tessellation [31], and the size of each sub-region associated with each selected sample quantifies the sampling density of the

design space. The samples are then ranked using a weighted sum of the nonlinearity and the sampling density. New samples are added in the neighbourhood of the M top-ranked points, that represent the most nonlinear, and the most under-explored regions. This procedure is repeated for the new set of $(N_0 + M)$ samples. New samples are added until a stopping criterion is met, in this case a predetermined maximum number of samples N_{max}.

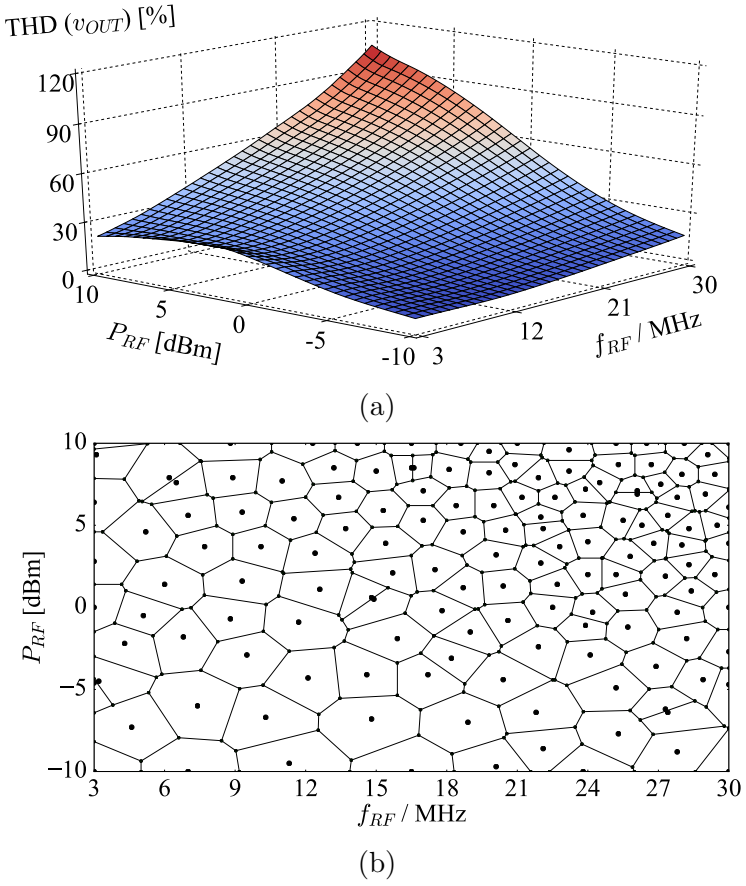


Figure 2.7: (a) Total harmonic distortion of the modelled v_{OUT} waveform in the design space, (b) Adaptively chosen samples with the Voronoi regions [37].

The proposed adaptive algorithm applied to building the training dataset for modelling the output voltage v_{OUT} of an output buffer in a DPI simulation test bench, in the (f_{RF}, P_{RF}) design space defined by the RF frequency f_{RF} from 3 MHz to 30 MHz, and the RF forward power P_{RF} from -10 dBm to 10 dBm. The THD of the buffer output voltage in these RF conditions is shown in Fig.2.7a, and the 144 adaptively selected samples in the given (f_{RF}, P_{RF}) design space are shown in Fig.2.7b.

The proposed sampling algorithm combines the exploitation and exploration strategies that are defined in [31]. The exploitation part of the algorithm aims to select more samples in the more nonlinear regions of the design space, and the exploration part of the algorithm aims to select more samples in the under-sampled regions that are more linear. This approach is a modification of the LOLA-Voronoi sampling algorithm used

in [11], which is suitable for design space sampling based on the nonlinearity of a scalar function of the design space variables. In [11], the mean value of the output voltage of a voltage regulator is modelled as a function of the frequency and RF forward power of the RF disturbance $V_{OUT} = V_{OUT}(f_{RF}, P_{RF})$, and the local linear approximation (LOLA) part of the algorithm identifies the regions where this 2D surface is the most nonlinear. Since each design space sample in the presented modelling approach is associated with a time-domain waveform, rather than a scalar function, the LOLA part of the algorithm is replaced with the THD of the modelled time-domain waveform as the measure of nonlinearity. The second modification is related to the Voronoi tessellation of the samples closest to the edge of the design space. In the default implementation of the Voronoi tessellation, the samples at the edge of the design space that have no neighbours in a one direction have unbounded sub-regions with an infinite area assigned to them. In order to obtain finite Voronoi region areas, the default Voronoi tessellation is intersected with the limits of the design space.

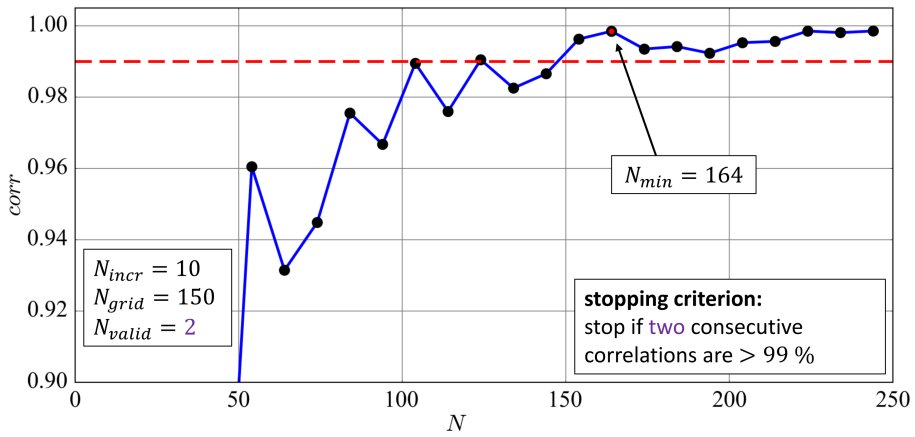


Figure 2.8: Spearman correlation between the consecutive interpolators of the total harmonic distortion.

Fig.2.8shows the Spearman correlation between the 2D interpolators of the THD in Fig.2.7a, obtained using the consecutive sets of additively selected design space samples shown in Fig.2.7b. The 2D interpolators are based on the piecewise cubic interpolating Bezier polynomial obtained using the Clough-Tocher scheme. As more samples are added, the accuracy of the resulting 2D interpolator converges to the value obtained by running the simulation in a dense uniform grid in the (f_{RF}, P_{RF}) design space, and adding more samples does not significantly increase the 2D interpolator accuracy. This approach enables identifying an unknown THD characteristic of the modelled waveform using a reduced number of circuit simulations, and it can be used as an alternative stopping criterion for the adaptive sampling algorithm during the building of the training dataset.

2.3.3 Hardware description language implementation of the ESN

After building the training dataset using to the procedure given in Section2.3.2and training and verifying the ESN model using the ESN training and verifications procedures given in Section2.2.2, the trained ESN model is implemented in a hardware description language, such as Verilog A, VHDL-AMS, MAST [25], to enable using it in commercial circuit simulators, such as Cadence® Spectre® or Mentor Graphics® Eldo. In the scope of this work, all behavioural models are implemented in Verilog A. The implementation of the ESN update equation (2.1) and the ESN output equation (2.3) in Verilog A is given in Listing2.1, using an example ESN with two input units $u1$, $u2$, a bias-term $u0$, two internal units $x1$, $x2$, and one output unit $y1$ with output feedback connections.

Listing 2.1: Code snippet of the ESN update and output equations implemented in Verilog A.

```
V(x1,gnd) <+ (1-a) * absdelay(V(x1,gnd), Ts);
V(x1,gnd) <+ a * tanh(V(x1_tilde));
V(x1_tilde,gnd) <+ Win_1_0 * V(u0,gnd);
V(x1_tilde,gnd) <+ Win_1_1 * V(u1,gnd);
V(x1_tilde,gnd) <+ Win_1_2 * V(u2,gnd);
V(x1_tilde,gnd) <+ W_1_1 * absdelay(V(x1.gnd), Ts);
V(x1_tilde,gnd) <+ W_1_2 * absdelay(V(x2,gnd), Ts));
V(x1_tilde,gnd) <+ Wfb_1_1 * absdelay(V(y1,gnd), Ts));
// analogously for V(x2,gnd)

V(y1,gnd) <+ Wout_1_0 * V(u0,gnd);
V(y1,gnd) <+ Wout_1_1 * V(u1,gnd);
V(y1,gnd) <+ Wout_1_2 * V(u2,gnd);
V(y1,gnd) <+ Wout_1_3 * V(x1,gnd);
V(y1,gnd) <+ Wout_1_4 * V(x2,gnd);
```

All statements in the Verilog A code are executed simultaneously, and the multiple contribution statements "<+" to the voltage of the nodes $x1$, $x1\_tilde$, and $y1$ are summed together. The discrete-time delay is implemented using the *absdelay* function, the internal unit activation function is the hyperbolic tangent tanh, and the output unit activation function is the identity function. The weight matrix coefficients Win_i_j, W_i_j, Wfb_i_j, $Wout\_i\_j$, the leaking rate a, and the sample time Ts are defined as variables of the type *real*. The input and output units are *inout* pins, and the internal units and the bias-term are defined as internal electrical nodes. The sequential contribution statements in the presented code can be generalized into for-loops that enable implementing ESN models with a variable number of neurons and the corresponding weight matrix coefficients. The full implementation of the echo state network in Verilog A is given in AppendixA.

2.4 Modelling results

The presented modelling results demonstrate the ability of the ESN to capture nonlinear relationships between time-domain signals in four test cases: a voltage follower, the driver IC of a DC-DC converter, an RF mixer, and a LIN interface circuit. In each test case, the time-domain signals observed in circuit simulations are split into ESN input and output signals. The trained ESN is implemented in Verilog A and driven by the piecewise linear (PWL) voltage source containing the input signal, and the ESN output signal is compared to the desired output signal using the mean square error (MSE). The achieved simulation speed-up factor is observed as an additional figure of merit.

2.4.1 Test case 1: Voltage follower

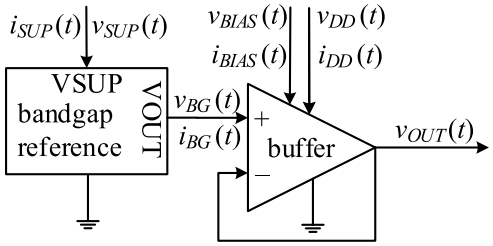


Figure 2.9: Simulation test bench of the voltage follower (buffer) at the output of a bandgap reference circuit [37].

The schematic of the circuit under test is given in Fig.2.9. The voltage follower (buffer) is an operational amplifier with a unity gain feedback connection, and it buffers the output voltage $V_{BG} = 1.234$ V of a bandgap reference circuit. The buffer is supplied from the supply voltage $V_{DD} = 5$ V, the reference current $I_{BIAS} = 5$ µA defines the bias for the operational amplifier circuit. An RF interference signal is injected into the power supply V_{DD} of the buffer using an injection network according to the DPI standard [28]. The design space for selecting the time-domain waveforms for modelling is defined by the RF frequency f_{RF} in the range [3 MHz, 30 MHz] and by the RF forward power P_{RF} in the range [−10 dBm, 10 dBm]. The transistor-level circuit with extracted layout parasitic elements is simulated within the design space using the Cadence® Spectre® circuit simulator to obtain the time-domain waveforms in the steady-state. The waveforms of the supply current $i_{DD}(t)$, input current $i_{BG}(t)$, bias current $i_{BIAS}(t)$, and output voltage $v_{OUT}(t)$ under the RF disturbance are modelled as functions of the supply voltage $v_{DD}(t)$, input voltage $v_{BG}(t)$, and bias voltage $v_{BIAS}(t)$ using four ESN models. In the design space, 144 samples are selected in two ways: (i) using the proposed adaptive sampling algorithm with respect to the nonlinearity of the output voltage waveform $v_{OUT}(t)$, (ii) by uniformly sampling the design space with the same number of points.

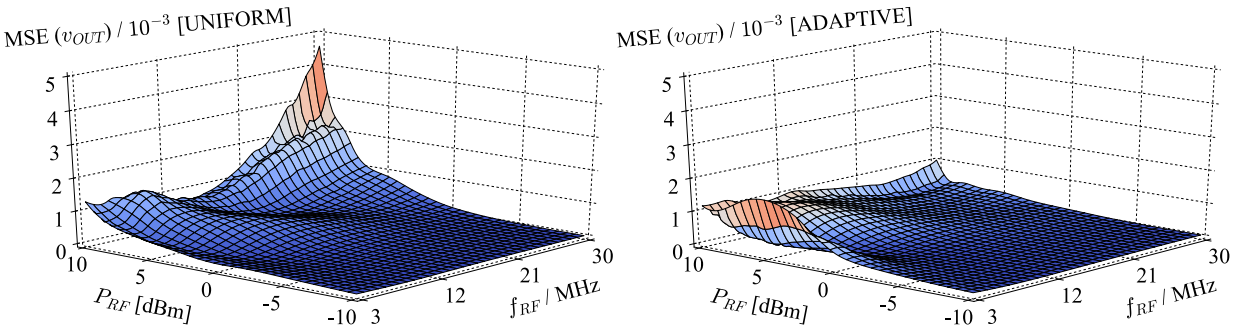


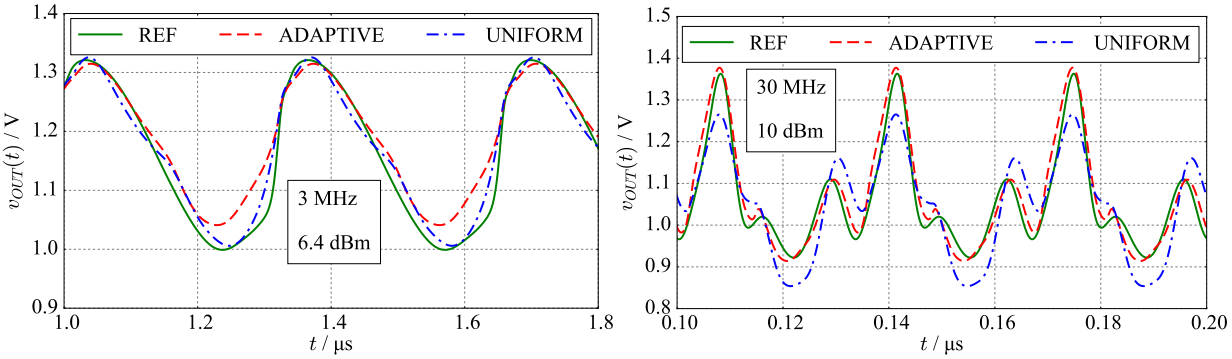
Figure 2.10: MSE of the v_{OUT} model of the voltage follower built using: (a) uniform sampling, with $\text{MSE}_{\max} = 4.59{\cdot}10^{-3}$, (b) adaptive sampling, with $\text{MSE}_{\max} = 1.60{\cdot}10^{-3}$ [37].

The ESN models are simulated in the Cadence® Spectre® circuit simulator. The THD of the output voltage v_{OUT} over the (f_{RF}, P_{RF}) design space is shown in Fig.2.7a, with the maximum THD value of 105.6% observed at (30 MHz, 10 dBm). The THD of the ESN input waveforms v_{BG}, v_{DD}, v_{BIAS} in the same point equal to 9.88%, 1.51%, 2.73% indicate that the voltage follower nonlinearity increases with the RF forward power. Two ESN models of the output voltage v_{OUT} are obtained using the uniform and adaptive sampling, and the MSE accuracy of the best performing model instances is presented in Fig.2.10over the (f_{RF}, P_{RF}) design space. Table2.1summarizes the MSE accuracy of the remaining ESN models, showing the worst-case MSE, and the MSE evaluated at the design space point with the highest value of the THD for each modelled signal. The verification dataset consists of the data points that are not present in the training dataset used to build the model.

The v_{OUT} models are built using ESNs with 25 neurons and identical hyper-parameters. The remaining ESN models each use 15 neurons to achieve good accuracy. In total, the four ESN models use 70 neurons to model the nonlinear behaviour of the voltage follower in the presented RF conditions as a function of the RF input signals defined by piecewise linear (PWL) voltage sources in the circuit simulator.

Table 2.1: Performance of the buffer model in the maximum MSE and the maximum THD points [37].

model	$\text{MSE}_{\max}$	MSE @ $\text{THD}_{\max}$
v_{OUT} [ADAPTIVE]	$1.60{\cdot}10^{-3}$	$1.00{\cdot}10^{-3}$
v_{OUT} [UNIFORM]	$4.59{\cdot}10^{-3}$	$4.59{\cdot}10^{-3}$
i_{DD}	$4.66{\cdot}10^{-8}$	$2.61{\cdot}10^{-8}$
i_{BG}	$1.47{\cdot}10^{-12}$	$2.26{\cdot}10^{-14}$
i_{BIAS}	$6.93{\cdot}10^{-12}$	$3.45{\cdot}10^{-12}$



(a) (b)

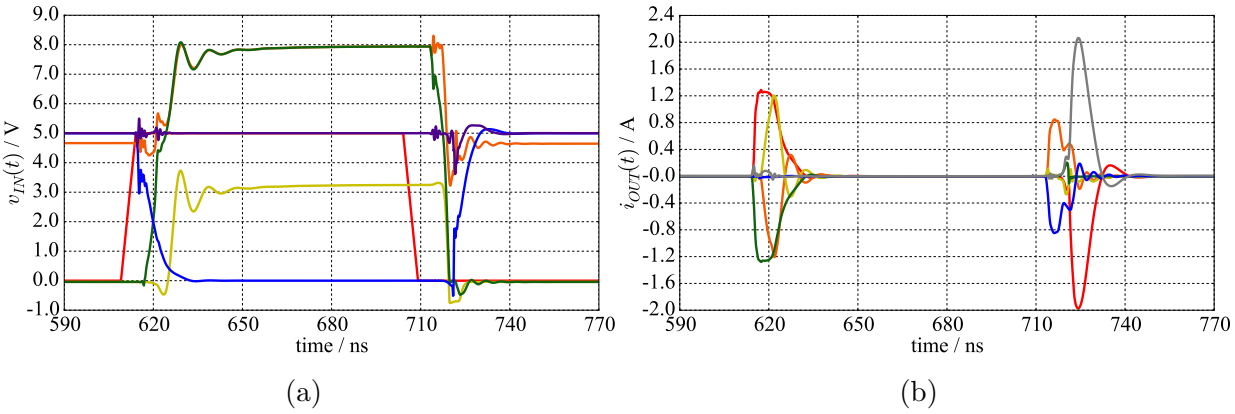
Figure 2.11: Comparison of model and netlist of the v_{OUT} model in: (a) the worst-case MSE point, with $\text{MSE}_{\text{adaptive}} = 1.60{\cdot}10^{-3}$, $\text{MSE}_{\text{uniform}} = 5.09{\cdot}10^{-4}$, (b) the highest THD point, with $\text{MSE}_{\text{adaptive}} = 1.00{\cdot}10^{-3}$, $\text{MSE}_{\text{uniform}} = 4.59{\cdot}10^{-3}$ [37].

Fig.2.11apresents the time-domain waveforms of the output voltage $v_{OUT}(t)$ of the two ESN models in the design space point (3 MHz, 6.4 dBm), where the maximum MSE of the ESN model built using the adaptive sampling algorithm is observed. Fig.2.11b presents the same waveforms at the design space point (30 MHz, 10 dBm), where the maximum THD of the output voltage v_{OUT} is observed. Table2.2presents the simulation speed-up observed when running all four ESN models in the commercial circuit simulator, compared to simulating the netlist that includes the extracted layout parasitics, at six design space points, compared to the THD of the output voltage v_{OUT}. The simulation time T_{REF} of the transistor-level schematic increases with RF forward power due to increasing nonlinearity observed through the THD of the output voltage v_{OUT}.

Table 2.2: The simulation times required for simulating 100 periods of the RF disturbance using the extracted netlist (T_{REF}) and the adaptive ESN model (T_{MOD}) [37].

f_{RF} [MHz]	P_{RF} [dBm]	T_{REF} [s]	T_{MOD} [s]	speed-up factor	THD_{VOUT} [%]
3	-10	2.59	3.03	0.85	7.67
	10	6.55	6.50	1.01	19.85
15	-10	3.00	3.32	0.90	8.43
	10	16.00	6.38	2.51	50.19
30	-10	3.06	3.27	0.94	16.51
	10	26.9	6.18	4.35	108.10

2.4.2 Test case 2: DC-DC driver IC



(a) (b)

Figure 2.12: Time-domain signals obtained by simulating the transistor-level driver IC of a DC-DC converter: (a) ESN input signals, (b) ESN output signals. The sampling time is 100 ps [34].

Fig.2.12presents the simulated time-domain voltages and currents associated with several pins of the driver IC of a DC-DC converter that are modelled using a single ESN model with multiple inputs and multiple outputs. The ESN input signals are the seven steady-state voltage waveforms shown in Fig.2.12a, and the ESN output signals are the six steady-state current waveforms shown in Fig.2.12b, obtained by simulating the transistor-level model of the IC in the Cadence® Spectre® circuit simulator, and by interpolating the waveforms to the sampling time of 100 ps. The training dataset consists of a total of 630513 data points. The ESN input and output signals are not rescaled, as modelled current waveforms are in the same order of magnitude as the voltage waveforms.

Table 2.3: MSE performance of the ESN and RNN models [34].

MSE	RNN		ESN	
	training	verification	training	verification
IOUT1	$4.37{\cdot}10^{-5}$	$4.51{\cdot}10^{-5}$	$3.59{\cdot}10^{-6}$	$4.93{\cdot}10^{-6}$
IOUT2	$1.88{\cdot}10^{-5}$	$1.87{\cdot}10^{-5}$	$1.64{\cdot}10^{-5}$	$2.06{\cdot}10^{-5}$
IOUT3	$1.86{\cdot}10^{-5}$	$1.84{\cdot}10^{-5}$	$1.01{\cdot}10^{-5}$	$1.17{\cdot}10^{-5}$
IOUT4	$1.76{\cdot}10^{-5}$	$1.83{\cdot}10^{-5}$	$1.86{\cdot}10^{-6}$	$3.05{\cdot}10^{-6}$
IOUT5	$4.84{\cdot}10^{-6}$	$5.03{\cdot}10^{-6}$	$1.00{\cdot}10^{-5}$	$1.23{\cdot}10^{-5}$
IOUT6	$2.79{\cdot}10^{-5}$	$2.88{\cdot}10^{-5}$	$3.70{\cdot}10^{-6}$	$4.74{\cdot}10^{-6}$
AVERAGE	$2.19{\cdot}10^{-5}$	$2.24{\cdot}10^{-5}$	$7.61{\cdot}10^{-6}$	$9.55{\cdot}10^{-6}$

The ESN hyper-parameters are selected manually in a short trial-and-error process. The hidden layer has $N_{\mathbf{x}} = 60$ internal units, with the hyperbolic tangent tanh as the internal unit activation function, and the spectral radius r of 0.9. The random input weight matrix coefficients are selected from the uniform distribution within $[-1, 1]$. The output feedback connections are not used in order to keep the output signals independent from each other. A white noise term having the variance $\sigma = 5 \cdot 10^{-4}$ is added during ESN training. The leaking rate a is set to 0.1, and a bias-term $U_b = 1$ is used. The verification dataset is constructed by adding a white noise term having the variance σ defined as 0.1% of the maximum value of each modelled signal. The trained ESN model is implemented in Verilog A and simulated in the Cadence® Spectre® circuit simulator.

The ESN model is benchmarked against a reference recurrent neural network (RNN) model implemented using the nonlinear autoregressive neural network (NARX) topology available in the Neural Network Toolbox™ in MATLAB®. The reference RNN has the same number of 60 neurons as the ESN model, and it is trained using the Bayesian regularisation backpropagation algorithm, defined in [47], [48], on the same training and verification datasets as the ESN model.

The performance of the ESN and RNN models is summarised in Table2.3for each output signal separately. The ESN model achieves on average 57% better MSE accuracy than the reference RNN model on the verification dataset. The time-domain output of the ESN model on the verification dataset is presented in Fig.2.13. The time needed to build the RNN model is between 1 and 2 hours, compared to the training time of less than 1 second for the ESN model. The transient simulation of the ESN model is 16.4 s, compared to the transistor-level model that requires 99.3 s, providing a speed-up factor of six. All simulations are run on a workstation with the dual Intel® Xeon® X5675 CPU @ 3.2 GHz and 50 GB of RAM.

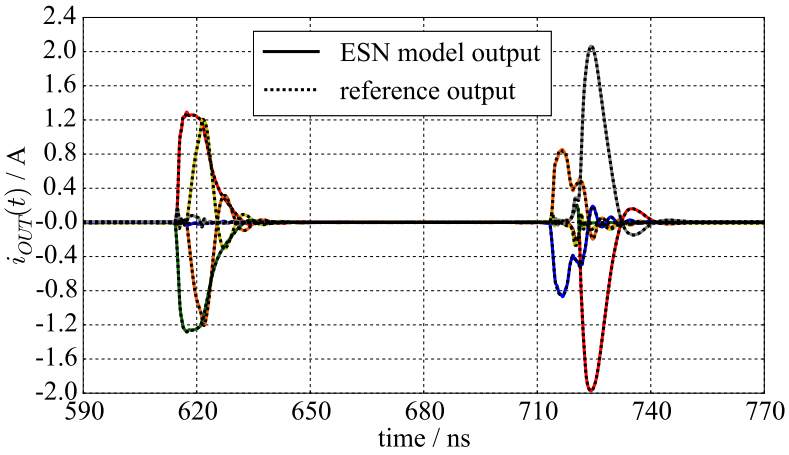


Figure 2.13: Performance of the ESN model compared to the reference output signal. The verification dataset is obtained by adding a white noise term to the training dataset [34].

2.4.3 Test case 3: LIN interface

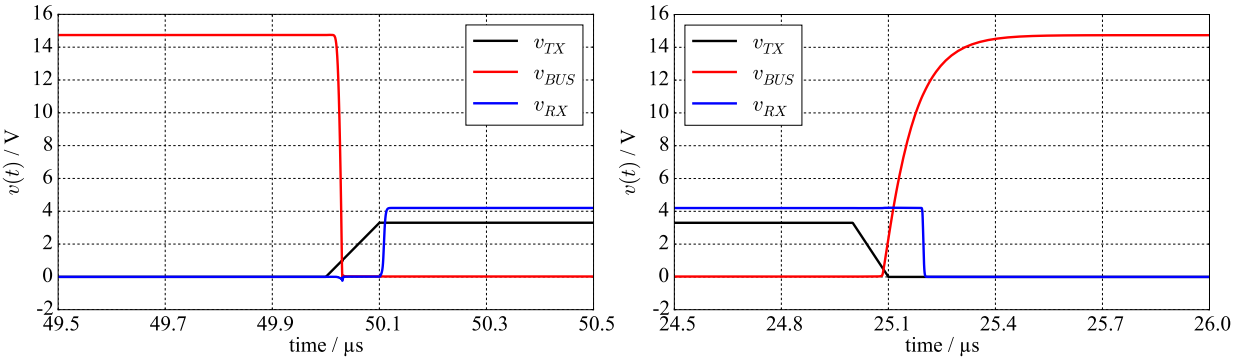


Figure 2.14: The input (red) and output (blue) signals obtained using the transistor-level model of the LIN interface with the included parasitic elements: (a) rising edge of the signals, (b) falling edge of the signals. The uniform sampling time is 100 ps [34].

Fig.2.14presents the signals associated with a local interconnect network (LIN) interface that are modelled using an ESN model. A pulse waveform with the rise- and fall-times of 100 ns is transmitted to the LIN bus. The width of the transmitted pulse v_{TX} is 25 µs, with the high- and low-levels of 3.3 V and 0 V. The signal on the bus v_{BUS} is in negative logic, with the high- and low-levels of 0 V and 15 V. The signal v_{RX} is received at the receiver after a finite delay-time, with the high- and low-levels of 4.2 V and 0 V. The full transistor-level model of the LIN interface including the extracted layout parasitic elements is simulated, and the obtained time-domain waveforms are interpolated to a uniform sampling time of 100 ps.

The inventory of the simulation test bench is presented in Table2.4. The bus signal v_{BUS} is used as the ESN input signal, and the received signal v_{RX} is used as the ESN output signal. During the rising edge of v_{RX} shown in Fig.2.14b, the ESN input signal v_{BUS} reaches its stationary value of 0 V almost immediately after the change on the bus occurs, and the response at the ESN output signal occurs after a delay-time of approximately 100 ns, corresponding to 1000 samples in the time-domain. The training dataset contains $1.15{\cdot}10^6$ samples, and the testing dataset contains $1.5{\cdot}10^6$ samples. A single ESN is used to model the behaviour of the signal on the RX pin as a function of the signal on the bus, including the stationary state, the rising edge, and the falling edge of the signal. The hidden layer has $N_{\mathbf{x}} = 30$ internal units with the spectral radius r set to 0.8. The hyperbolic tangent tanh is used for both the internal unit activation function f, and for the output unit activation function f^{out}. The coefficients of the input weight matrix $\mathbf{W^{IN}}$ are uniformly distributed between -0.99 and 0.99. The output feedback connections are not used. A white noise term having the variance $\sigma = 1 \cdot 10^{-3}$ is added during the training phase. The leaking rate a is set to 0.005, and a bias-term $U_b = 0.5$ is used.

Table 2.4: The circuit inventory of the LIN interface transistor-level model with the included layout parasitic elements [34].

circuit inventory	total number
nodes	2109
equations	2939
bsim3v3	15
capacitor	5490
cccs	4862
diode	11
inductor	390
jfet	18
inductors	2431
resistor	1726
vcvs	9
vsource	399

The generalisation properties of the ESN model are tested by changing the width of the transmitted pulses from 25 µs to 12.5 µs, while retaining the rise-and fall-times. The results are presented in Fig.2.15in the time-domain for the rising and falling edges of the signals, with the MSE value of $1.771{\cdot}10^{-3}$. The simulation time is improved from 192.0 s for the transistor-level circuit to 2.47 s for the ESN model, corresponding to a simulation speed-up factor of 77. All simulations are run on a workstation with the Intel® Core® i7 CPU @ 3.0 GHz and 12 GB of RAM.

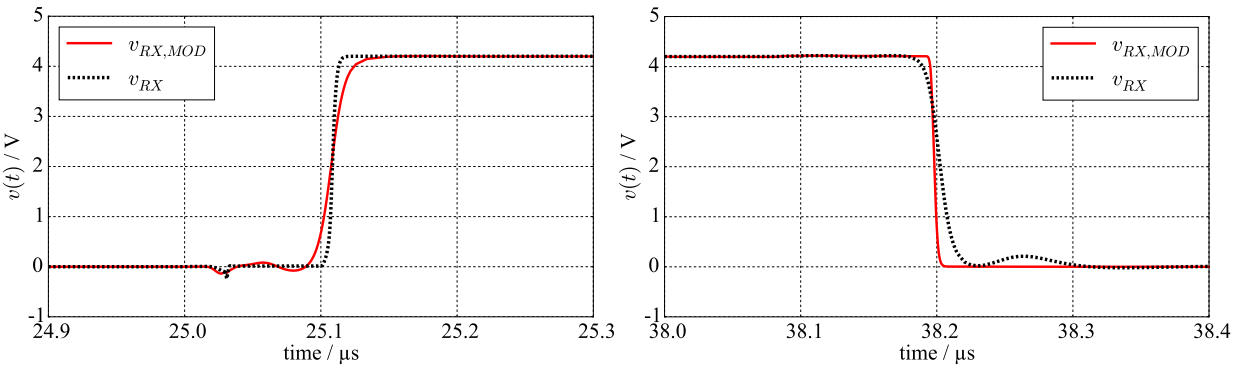


Figure 2.15: ESN model output compared to the reference output signal: (a) rising edge of the modelled signal, (b) falling edge of the modelled signal. The mean square error is $1.771{\cdot}10^{-3}$ [34].

2.4.4 Test case 4: Oscillator with feedback

An oscillator with a feedback connection and a period of 440 samples analytically defined by Eq. (2.10) in the discrete-time domain is modelled using an echo state network:

$$y[n] = A\sin\left(y[n-1] + \frac{n}{N}\right) + A\sin\left(y[n-1] + m \cdot \frac{n}{N}\right) + D \tag{2.10}$$

where $A = 0.2$, $N = 70$, $m = 15$, $D = 0.4$. The modelled system with memory due to the feedback connection, with two time-constants separated by a factor of 15. Since the ESN model has no input neurons, the hidden layer containing 40 neurons is excited using the output feedback connections defined by the output feedback weight matrix $\mathbf{W^{FB}}$. The spectral radius r is set to 0.99, the leaking rate a is equal to 0.07, the bias-term $U_b = 1$ is used, and a white noise term having the variance of $1{\cdot}10^{-5}$ is added during ESN training.

Fig.2.16presents the behaviour of the trained ESN model in the modified verification phase for autonomous ESN models that have no input neurons. During the first $10{\cdot}10^3$ samples, the ESN model is in the "teacher forcing" phase, as defined in [13], where the ESN output unit activations are driven by the wanted output signal. The connections from the hidden layer to the output unit, defined by the output weight matrix $\mathbf{W^{OUT}}$, are disconnected, and the internal unit activations are defined by the output feedback connections according to the output feedback weight matrix $\mathbf{W^{FB}}$. The internal unit activations are "locked" to the correct oscillation that contains the two time-constants. After this phase, the feedback loop is closed, and the ESN model is run completely autonomously for the following $35{\cdot}10^3$ samples, with the output signal from that point forward generated exclusively by the ESN model with the feedback loop defined by the output feedback weight matrix $\mathbf{W^{FB}}$. Fig.2.16ashows the ESN model output during the initial teacher forcing phase and the transition to the autonomous phase, and Fig.2.16b shows the ESN model output after $26{\cdot}10^3$ samples of autonomous operation.

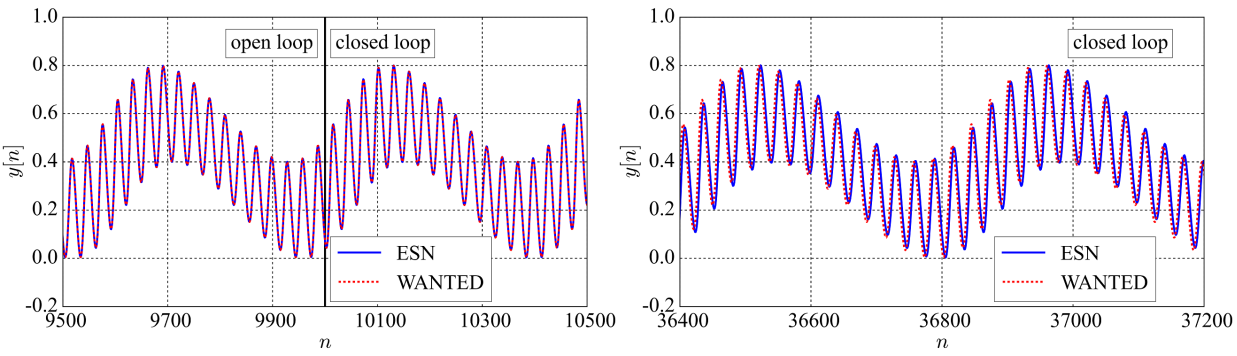
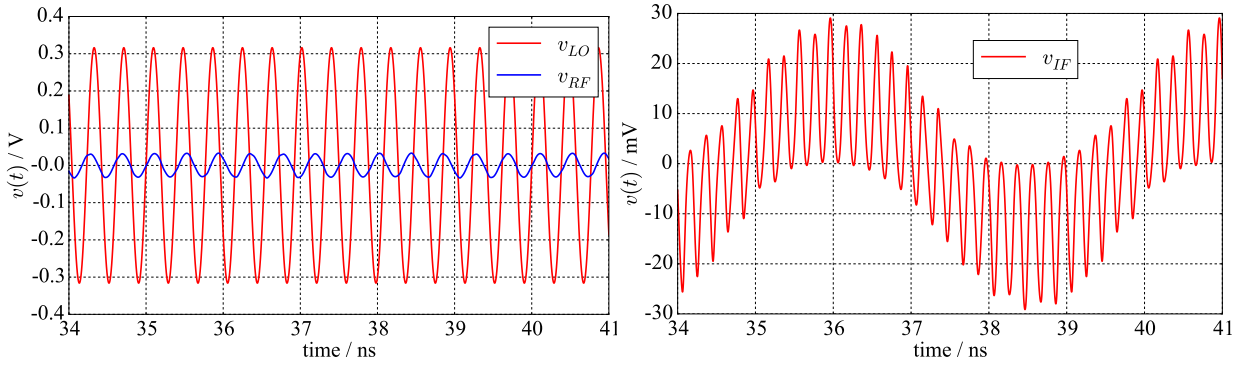


Figure 2.16: The behaviour of the ESN model of the oscillator with a feedback connection: (a) in the "teacher forcing" phase during the first $10{\cdot}10^3$ samples, (b) during the autonomous phase.

2.4.5 Test case 5: RF mixer



(a) (b)

Figure 2.17: The input and output test signals obtained using the transistor-level models of the RF mixer "HCBT2" in [49] with $f_{RF} = 2.4$ GHz, $f_{LO} = 2.6$ GHz, $f_{IF,LOW} = 200$ MHz, $f_{IF,HIGH} = 5.0$ GHz: (a) ESN input signals, (b) ESN output signals. The sampling time is 0.5 ps [34].

Fig.2.17presents the transient simulation data of the RF mixer labelled as "HCBT2" in [49], that was kindly provided by the authors of the paper. The RF mixer has two input signals: the radio-frequency (RF) signal v_{RF} that has a fixed frequency of 2.4 GHz in the Wi-Fi band, and the local oscillator (LO) signal v_{LO} that has an adjustable frequency. The output signal is the intermediate frequency (IF) signal v_{IF} that contains the sum and the difference frequency components of the input signals: $f_{IF,HIGH}$ and $f_{IF,LOW}$. The frequency of the local oscillator is adjusted to achieve one of the following intermediate frequencies $f_{IF,LOW}$: 20 MHz, 30 MHz, 40 MHz, 50 MHz, 100 MHz, 150 MHz, 200 MHz, and the corresponding sum frequencies $f_{IF,HIGH}$. The v_{RF} and v_{LO} signals have constant amplitudes of 32 mV and 316.1 mV, respectively, and the amplitude of the resulting IF signal envelope is 29.5 mV. The sampling time for all signals is 0.5 ps in order to capture the high frequency components of the output signal.

A single ESN is used to model the intermediate frequency signal v_{IF} as a function of the RF and LO signals v_{RF} and v_{LO} for all selected values of the intermediate frequency $f_{IF,LOW}$. In order to test the generalisation properties of the ESN model, only the $f_{IF,LOW}$ values of 20 MHz, 40 MHz, 100 MHz and 200 MHz are used in the training dataset. The time-series waveforms at each intermediate frequency contain 599985 samples, giving the total number of samples of $2.4{\cdot}10^6$ in the training dataset, and $4.2{\cdot}10^6$ in the testing dataset. The hidden layer of the ESN model has $N_{\mathbf{x}} = 40$ internal units. The initial weight matrix $\tilde{\mathbf{W}}$ is rescaled to the spectral radius $r = 0.99$. The coefficients of the input weight matrix $\mathbf{W^{IN}}$ are uniformly distributed between -0.7 and 0.7. The internal unit activation function f is the hyperbolic tangent (tanh), and the output unit activation function f^{out} is the identity function. The output feedback connections are not used. A

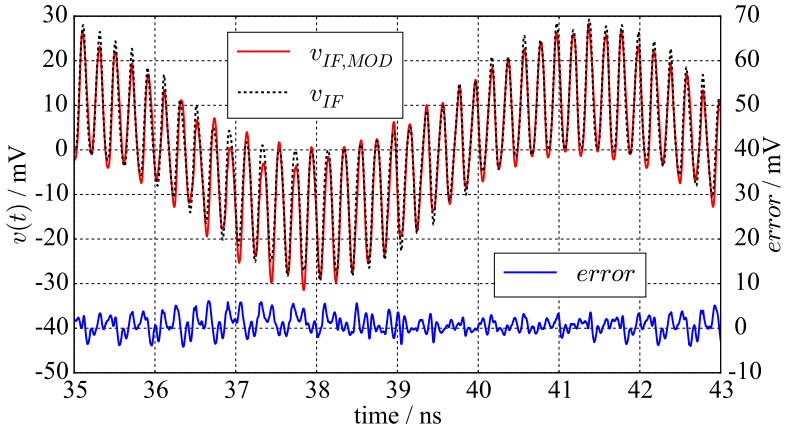


Figure 2.18: Performance of the ESN model compared with the reference output signal for the case with $f_{IF,LOW} = 150$ MHz, $f_{RF} = 2.40$ GHz, $f_{LO} = 2.55$ GHz, $f_{IF,HIGH} = 4.95$ GHz, $error = v_{IF} - v_{IF,MOD}$ [34].

white noise term having the variance $\sigma = 1 \cdot 10^{-5}$ is added during ESN training. The leaking rate is set to $a = 0.07$, and a bias-term $U_b = 0.2$ is used. Since the amplitudes of the ESN input signals have a ratio of 1:10, the ESN input signals are rescaled to the range from -0.7 to 0.7 using the rescaling method presented in Section2.3.1. The ESN model is simulated in the Cadence® Spectre® circuit simulator for all available $f_{IF,LOW}$ values.

Fig.2.18shows the modelling results for the case with $f_{IF,LOW} = 150$ MHz in the time-domain, and Table2.5presents the MSE accuracy of the ESN model over the values $f_{IF,LOW}$ for the training phase and the verification phase separately, including model execution times in the circuit simulator. Since the ESN model is built directly from the provided time-series data without the related execution time, the comparison of simulation times is not possible.

Table 2.5: MSE performance of the ESN model for the RF mixer [34].

$f_{IF,LOW}$	MSE		model execution time
[MHz]	training	verification	[s]
20	$1.75{\cdot}10^{-6}$	$4.91{\cdot}10^{-6}$	13.9
30	-	$4.72{\cdot}10^{-6}$	14.9
40	$1.47{\cdot}10^{-6}$	$4.58{\cdot}10^{-6}$	13.7
50	-	$4.43{\cdot}10^{-6}$	14.5
100	$1.15{\cdot}10^{-6}$	$4.06{\cdot}10^{-6}$	14.3
150	-	$4.26{\cdot}10^{-6}$	14.0
200	$2.33{\cdot}10^{-6}$	$5.00{\cdot}10^{-6}$	14.2

2.5 Discussion

This section discusses the favourable properties of the echo state network that enable modelling a wide range of behaviour observed in time-domain simulations of various integrated circuits, their dependence on the selected hyper-parameters, and the merits and limitations of the proposed sampling algorithm for building the training dataset. The five modelling test cases presented in Section2.4demonstrate that the echo state network is applicable for modelling a wide range of behaviour observed in time-domain simulations of various integrated circuits.

In the DC-DC driver IC and LIN interface test cases presented in Sections2.4.2 and2.4.3, the instantaneous values of the modelled time-domain waveforms cannot be constructed as a nonlinear combination of the instantaneous values of the input signals, since the variations in the ESN output signals are delayed with respect to the variations in the ESN input signals by up to 1000 discrete-time samples. The ESN model has to generate the modelled output signals using the echoes of the previous values of the ESN input signals that are available in the hidden layer neuron activations, demonstrating the memory properties of the ESN models. The LIN interface test case also shows that the ESN model correctly responds to the changes in the input signal regardless of when they occur in time, with a stable stationary value of the ESN output signal during the stationary period regardless of its length.

The oscillator test case presented in Section2.4.4is a purely analytical discrete-time system, used for demonstrating the theoretical ability of the ESN to model systems with widely separated time-constants, and this ESN property is applied to modelling the behaviour of an industrial RF mixer block in the test case presented in Section2.4.5. The oscillator test case also demonstrates the ESN ability to run autonomously without input signals using the teacher forcing method. A small drift between the model and wanted output is observed after $27{\cdot}10^3$ samples of autonomous operation, corresponding to about 60 periods of the low-frequency component of the output signal. This behaviour is attributed to the accuracy of the ESN model approximation of the true eigenvalue of the modelled system that corresponds to the slower oscillating frequency. The RF mixer test case also demonstrates the excellent interpolation properties of the echo state network, where certain values of the local oscillator frequency in the verification dataset are not included in the training dataset. Excellent MSE accuracy is achieved for the full verification dataset, including the omitted frequencies.

Since the behavioural models are not physical models, the generalization of the echo state network is limited to interpolating the model behaviour within the range of operation covered by the training dataset, and the behaviour of the modelled circuit cannot be extrapolated outside of the modelled design space. In addition to interpolation, the

ESN generalization is also observed when adding noise to the data in the verification dataset of the DC-DC driver IC test case, demonstrating that the trained ESN model is not over-trained on the exact values used in the training phase.

The good interpolation properties of the ESN model also depend on the quality of sampling the modelled circuit behaviour in a given design space. The adaptive sampling algorithm presented in Section2.4.1enables the construction of training datasets for building models of highly nonlinear circuits over a wide range of operation using a limited number of simulation runs. The presented ESN model of the voltage follower built using the adaptively selected points has a lower MSE over the overall design space than the ESN model built by uniformly sampling the design space using the same number of samples. The uniform model has better performance in the worst-case MSE point of the adaptive model, however the MSE increases with the nonlinearity of the modelled circuit, while the adaptive model minimizes the MSE uniformly over the given design space. Adjusting the weights associated with the exploration and the exploitation parts of the adaptive sampling algorithm enables tuning the focus of the training dataset between the highly nonlinear regions of circuit operation and the overall coverage of the operating conditions of the modelled circuit. As an additional use case, the dynamic stopping criterion based on the Spearman correlation enables evaluating any scalar property of a given circuit design using a reduced number of required design space samples selected using the adaptive algorithm. Empirically, the required number of simulated sampling points is smaller than when using a uniform grid or random sampling for the achieved accuracy of the evaluated scalar property, such as the total harmonic distortion of a given signal over the (f_{RF}, P_{RF}) design space.

The echo state network model of the DC-DC driver IC is benchmarked against a reference nonlinear autoregressive neural network (NARX), and the achieved MSE accuracy of the ESN model is better or comparable to the reference NARX model that has the same number of neurons. Building the ESN model is much simpler than building the NARX model because it is not necessary to select the number and value of the input and feedback delays in the topology of the NARX model to achieve stable model behaviour. The stability of the ESN model depends on the existence of the echo state property, and the presented method for generating the recurrent connections in the ESN hidden layer ensures the existence of the echo state property according to[39], therefore guaranteeing the stability of the resulting ESN model. The ESN training time is also significantly shorter compared to the NARX model, as it is reduced to a computationally inexpensive linear regression task, compared to the relatively complex backpropagation algorithm used for training the NARX model. The number of internal units in the ESN hidden layer does not have a significant impact on the ESN model training time. For example, if the

number of internal units is increased by a factor of 10, the training time remains in the order of several seconds.

The fast ESN training procedure enables running the iterative trial-and-error process of selecting the hyper-parameters significantly faster than for the NARX model, as the modelling method flow-chart shown in Fig.2.4requires running the training algorithm multiple times. It is also possible to let the ESN "decide" which input signals from the modelling dataset are important, by connecting all available inputs to the ESN. All presented models are relatively insensitive to the exact value of the hyper-parameters. The leaking rate a is shown to be the most critical hyper-parameter of the ESN models presented in LIN interface and RF mixer test cases. The small value of the leaking rate enables the formation of the necessary dynamics in the hidden layer of the ESN required to successfully retain the memory of the previous input values, which is necessary to model the delay between the input and output signals in the LIN interface test case, and to model different time-scales present in the RF mixer test case.

Compared to the transistor-level models with included extracted layout parasitic elements, the ESN model achieves simulation speed-up factors from 6 in the DC-DC driver IC modelling test case, up to 77 in the LIN interface modelling test cases. Table2.4shows that the extracted layout parasitic elements add significant complexity to the transistor-level model, with several thousand parasitic RLC elements, while not fundamentally altering the nature of the modelling problem. Since the ESN model uses only the input-output behaviour of the modelled circuit, versions of the circuit with and without the extracted layout parasitic elements can both be modelled using ESN models of similar size, expressed as the number of neurons in the hidden layer. The simulation speed-up factors presented in Table2.2show that the simulation time of the transistor-level circuit with the extracted layout parasitic elements in the conducted immunity simulation test bench increases with increasing RF forward power levels. This increase is attributed to the circuit entering the nonlinear region of operation that is observed by the increasing values of the total harmonic distortion of the modelled time-domain waveforms. The execution time of the ESN model is almost constant for a given RF forward power level, regardless of the total harmonic distortion of the modelled waveforms, and it is mostly defined by the selected number of internal units in the hidden layer. The selected ESN sizes up to 60 neurons in presented test cases provide a good trade-off between model accuracy and the execution time in the circuit simulator. In addition to the simulation speed-up, the black-box approach of modelling only the input-output behaviour of the modelled circuit enables hiding the intellectual property of the modelled transistor-level block by reproducing the time-domain behaviour of the modelled circuit in a selected range of operation without revealing the implementation details.

2.6 Summary

The echo state network is introduced as the building block for modelling large-signal behaviour of nonlinear integrated circuits. The formal mathematical definition of the echo state network is given with the procedure for guaranteeing bounded-input bounded-output (BIBO) stability. The procedures for the training and the verification of an echo state network with randomly generated recurrent connections in the hidden layer are presented for time-series modelling. The proposed method for modelling the nonlinear circuit behaviour defines the modifications to the generic ESN training procedure for time-series modelling required for modelling the time-domain waveforms obtained by simulations of integrated circuits. An iterative method for manually selecting the ESN hyper-parameters is given, with a set of guidelines that describe the influence of each ESN hyper-parameter on the properties of the iteratively generated ESN instances.

An adaptive algorithm for sampling the nonlinear circuit behaviour in the design space is presented that enables building the ESN training dataset with more samples placed in the design space regions with higher nonlinearity expressed as total harmonic distortion of the modelled waveforms, while avoiding the under-sampling of linear regions. Two stopping criteria for the adaptive sampling algorithm are presented, based on a fixed maximum number of samples, and on Spearman correlation between consecutive 2D interpolators of the user-selected scalar function above a defined design space.

The implementation of the echo state network in the hardware description language Verilog A is given. The Verilog A implementation enables the use of the ESN model in commercial circuit simulators. The proposed modelling methodology is applied to five industrial test cases: a voltage follower, a DC-DC driver IC, a LIN interface, an analytical oscillator with a feedback connection, and an RF mixer. The presented modelling results demonstrate the feasibility of using the echo state network to model a wide range of nonlinear behaviour observed in integrated circuit simulations, including the memory effects with delays between the input and output signals of up to 1000 samples, and the behaviour associated with circuits that have two widely separated time-constants (eigenvalues).

The ESN model is benchmarked against the reference recurrent neural network model, and it is shown to enable obtaining comparable accuracy expressed as mean square error using a faster and simpler training procedure with guaranteed BIBO stability. The generalization properties of the ESN model are limited to interpolation within a trained design space, and to the ability to react to input signals with additive white noise. Simulation speed-up factors up to 77 are observed compared to the transistor-level circuits with included layout parasitic elements, and the execution time of the ESN model less dependent on the total harmonic distortion of the modelled time-domain waveforms observed in the integrated circuit.

Chapter 3

Nonlinear impedance model for behavioural model interconnectivity

3.1 Motivation

A nonlinear impedance model based on the echo state network is proposed. The model enables building interchangeable behavioural models of integrated circuits in the conducted immunity simulation environment according to the IEC-62132-4 Direct RF Power Injection (DPI) standard [28], and it is applied to a buffered voltage reference integrated circuit that consists of three subcircuits.

An overview of nonlinear effects observed in the conducted immunity simulations of the modelled circuit is presented, and the methodology for evaluating the accuracy of the modelled time-domain waveforms is introduced. The stability of the presented behavioural models is analysed, including the DC operating point stability, the small-signal stability, and the initial transient stability.

The chapter is organized as follows. The architecture for building interchangeable behavioural models using echo state networks is presented in Section3.2, including the model extension that enables modelling the DC and RF behaviour independently. Section3.3 presents the simulation environment for evaluating the conducted immunity of integrated circuits. The presented modelling method applied to the modelling of buffered voltage reference circuit consisting of three subcircuits, and an overview of nonlinear effects observed in the top-level test bench is given. Section3.4presents the stability analysis of the behavioural models in the simulation environment, and Section3.5presents three modelling test cases that demonstrate the ability of the presented behavioural models to correctly load the connected transistor-level circuits and other behavioural models. The presented results are discussed in Section3.6, and Section3.7summarizes the chapter. The research from this chapter is presented in [36], [38], [41], [42].

3.2 Interchangeable behavioural model architecture

3.2.1 Nonlinear impedance model based on controlled sources

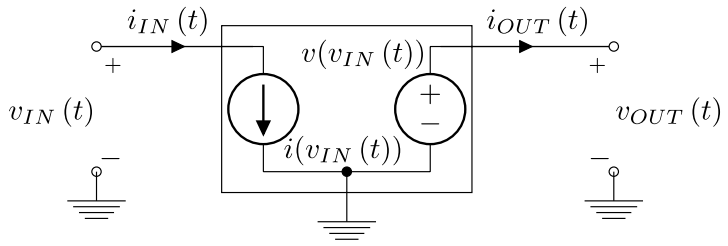


Figure 3.1: The basic interchangeable behavioural model architecture [36].

When a top-level test bench consists of several transistor-level subcircuits, a behavioural model of a subcircuit is "interchangeable" if the DC and RF voltages and currents observed in the time-domain simulation of the top-level test bench are preserved when the modelled transistor-level subcircuit is replaced by its behavioural model. Fig.3.1presents the basic architecture for modelling the nonlinear input impedance seen at the pin of the modelled subcircuit using a voltage-controlled current source (VCCS) is used to define the input current $i_{IN}(t)$ as a function of the input voltage $v_{IN}(t)$.

E.g. a purely resistive input impedance is modelled using a VCCS with the function:

$$i\left(v_{IN}(t)\right) = \frac{v_{IN}(t)}{R} \tag{3.1}$$

where R is the modelled input resistance.

In a general case, the function $i\left(v_{IN}(t)\right)$ is a nonlinear function of the instantaneous input voltage $v_{IN}(t)$ and its previous values. The modelling results presented in Chapter2 demonstrate that the echo state network is an appropriate building block for implementing such nonlinear functions with memory.

The output voltage $v_{OUT}(t)$ is modelled as a function of the input voltage $v_{IN}(t)$ using a voltage-controlled voltage source (VCVS), and the output current $i_{OUT}(t)$ is defined by the load impedance connected to the output pin of the behavioural model, as a function of the output voltage $v_{OUT}(t)$.

The main limitation of the basic model architecture in Fig.3.1is its "uni-directionality": (i) for a given input voltage v_{IN}, the behavioural model generates the same output voltage v_{OUT} regardless of the load impedance connected to its output pin, and (ii) a voltage signal driving the output pin of the behavioural model cannot propagate to its input pin. The basic behavioural model architecture is therefore extended with an additional output feedback loop that senses the load impedance connected to the output pin through the output current i_{OUT} as an additional input signal of the behavioural model.

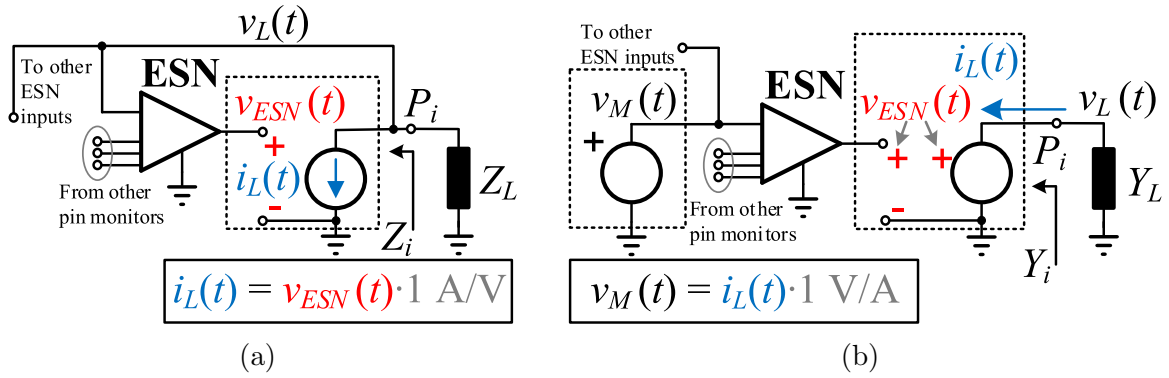


Figure 3.2: Dual nonlinear impedance behavioural models based on the echo state network (ESN) with a feedback loop: (a) monitoring voltage $v_L(t)$ and driving current $i_L(t)$, (b) monitoring current $i_L(t)$ and driving voltage $v_L(t)$ [38].

Fig.3.2presents the proposed architecture for modelling nonlinear impedances using two dual approaches based on the echo state network with a feedback loop. The basic input impedance model in Fig.3.1is implemented using the ESN model according to the approach shown in Fig.3.2a. The current i_L flowing into the pin P_i is driven by the ESN voltage v_{ESN} using a voltage-controlled current source (VCCS). The monitored pin voltage v_L is connected to the ESN input, in addition to any monitored signals from other pins, and it is defined by the nonlinear load impedance Z_L of the circuit connected to the pin P_i, and by the branch current i_L driven by the ESN. These voltage and current relationships are summarized in Eq. (3.2):

$$\begin{aligned} i_L(t) &= v_{ESN}(t) \cdot 1\,\text{A/V} \\ v_{ESN}(t) &= f_{ESN}\left(v_L(t), \dots\right) \\ v_L(t) &= Z_L\left(i_L(t)\right) \end{aligned} \tag{3.2}$$

In this feedback loop, the ESN drives the branch current i_L as a function of the monitored node voltage v_L at the pin P_i, through the interaction between the nonlinear impedances Z_i and Z_L.

The extension of the basic output voltage model in Fig.3.1that enables sensing the output current is shown in Fig.3.2b. The pin voltage v_L is driven by the ESN output voltage v_{ESN} using a voltage-controlled voltage source (VCVS). The current i_L flowing into the pin P_i is converted into the monitor voltage v_M with the same instantaneous numerical value using a current-controlled voltage source (CCVS), and it is connected to the ESN input in addition to any monitored signals from other pins. The monitored pin current i_L is defined by the nonlinear load admittance Y_L of the circuit connected to the pin P_i, and by the pin voltage v_L driven by the ESN. These voltage and current relationships are summarized in Eq. (3.3):

$$
\begin{aligned}
v_L(t) &= v_{ESN}(t) \\
v_{ESN}(t) &= f_{ESN}\left(v_M(t), \dots\right) \\
v_M(t) &= i_L(t) \cdot 1\,\mathrm{V/A} \\
i_L(t) &= Y_L\left(v_L(t)\right)
\end{aligned}
\tag{3.3}
$$

This feedback loop is dual to the feedback loop in Eq. (3.2). The ESN drives the node voltage v_L as a function of the branch current i_L at the pin P_i, through the interaction between the nonlinear admittances Y_i and Y_L.

The stability of the proposed feedback loops is analysed in Section3.4.

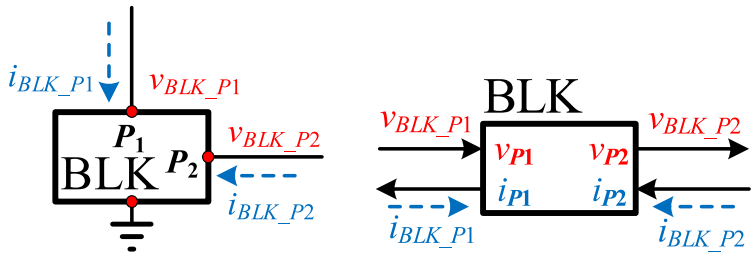


Figure 3.3: Definition of a generic 2-port circuit: (a) circuit schematic, (b) signal flow-diagram. The port voltages are referenced to the ground pin, and the port current direction is indicated by dashed arrows. The solid arrows in (b) indicate if a voltage or current is an input or an output signal [38].

The presented nonlinear impedance model architecture is applied to the modelling of a generic 2-port circuit BLK shown in Fig.3.3afor RF interference injection into port P_1 that is propagated to port P_2 using the following procedure:

- Each port P_i is associated with the pin voltage v_{BLK_Pi} referenced to the ground pin, and with the pin current i_{BLK_Pi} flowing into the BLK circuit by definition, as indicated by the dashed arrows.
- Each pin voltage v_{BLK_Pi} is classified either as a monitored input signal, or as a driven output signal, based on the model application. For the BLK circuit, v_{BLK_P1} is a monitored signal, and v_{BLK_P2} is a driven signal. Fig.3.3adoes not clearly show if a voltage is driven or monitored.
- Each pin current i_{BLK_Pi} is classified opposite to the pin voltage v_{BLK_Pi}. For the BLK circuit, i_{BLK_P1} is a driven signal because the voltage v_{BLK_P1} is monitored, and i_{BLK_P2} is a monitored signal.
- The pins P_i where the pin voltage v_{BLK_Pi} is monitored are modelled using the case in Fig.3.2a. The ESN model drives the pin current i_{BLK_Pi} using the monitored pin voltage v_{BLK_Pi} as one of its input signals. This model is selected for BLK port P_1.

- The pins P_i where the pin voltage v_{BLK_Pi} is driven are modelled using the case in Fig.3.2b. The ESN model drives the pin voltage v_{BLK_Pi} using the monitored pin current i_{BLK_Pi} as one of its input signals. This model is selected for BLK port P_2.
- The propagation of the RF voltage within the BLK circuit is modelled by using the monitored pin voltage v_{BLK_P1} as an input signal of the ESN that drives the pin voltage v_{BLK_P2}.

The BLK voltages and currents are split into the ESN input signals (v_{BLK_P1}, i_{BLK_P2}) and the ESN output signals (i_{BLK_P1}, v_{BLK_P2}). Eq. (3.4) presents the BLK nonlinear functions that are modelled using two echo state networks with controlled sources:

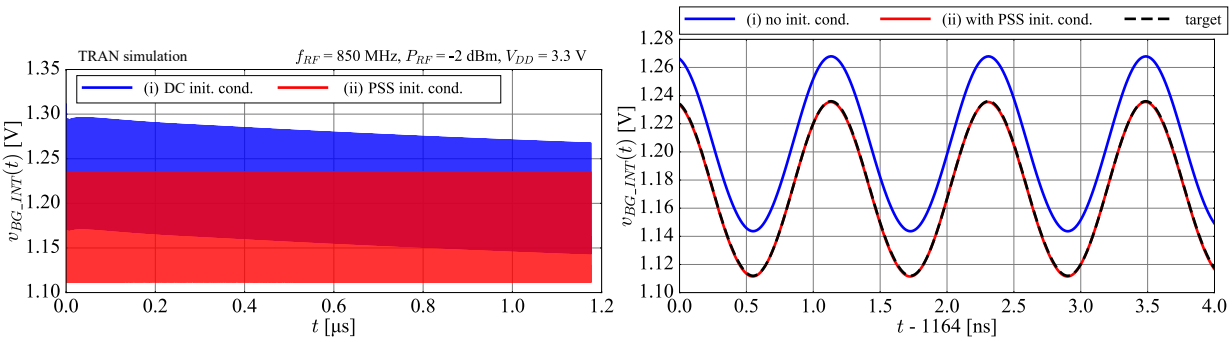
$$\begin{aligned} i_{BLK\_P1} &= i_{BLK\_P1}\left(v_{BLK\_P1}, i_{BLK\_P2}\right) \\ v_{BLK\_P2} &= v_{BLK\_P2}\left(v_{BLK\_P1}, i_{BLK\_P2}\right) \end{aligned} \tag{3.4}$$

Fig.3.3bpresents the definition of the BLK circuit in the signal flow-diagram, where the monitored ESN input signals are indicated by the solid arrows pointing into the BLK circuit, and the driven ESN output signals are indicated by the solid arrows pointing outward from the BLK circuit. Each port P_i has two sub-ports: one associated with the pin voltage v_{BLK_Pi} towards the reference ground, and one associated with the pin current i_{BLK_Pi} with the direction indicated by the dashed arrows, i.e. a two-port circuit has four ports in the signal flow-diagram representation.

The signal flow-diagram representation of a generic circuit block in Fig.3.3bis the basis for defining the dependencies between the time-domain signals observed in the conducted immunity simulations of the test benches with interconnected subcircuits, such as the test circuit presented in Section3.3. The interchangeable behavioural models are evaluated in the circuit simulator by replacing one or more transistor-level subcircuits with the behavioural model, and by observing the time-domain waveforms of the voltages and currents in the resulting test bench, that are defined by the interaction between the behavioural models and the transistor-level circuits, according to the feedback loops identified in Eqs. (3.2), (3.3).

The algorithms of the solvers available in commercial circuit simulators used for running the conducted immunity simulations are discussed next. The nonlinear impedance model architecture presented in Fig.3.2is extended to support the particular requirements related to the solver algorithms, and the implementation of the resulting behavioural model architecture in the hardware description language Verilog A is presented, that enables simulating the test benches where behavioural models are connected to transistor-level circuits in the RF steady-state.

3.2.2 Separating the DC and RF sub-models



(a) (b)

Figure 3.4: (a) Example of a TRAN simulation output of a conducted immunity test bench at 850 MHz, (b) zoom-in after 1000 periods [41].

The conducted immunity simulations can be run in the time-domain using the transient (TRAN) solver or using the periodic steady-state (PSS) solver [7]. The TRAN solver runs the differential equations of the simulated circuit in the time-domain starting from the DC operating point established in a DC simulation that is run prior to the TRAN simulation, or from an initial condition defined by the state of the circuit at the end of another TRAN or PSS simulation run. The main disadvantage of the TRAN solver, that is observed in conducted immunity simulations of many integrated circuits, are the long transient periods required to reach the steady-state in which the voltages and currents are settled, and the mean value of all capacitor currents and inductor voltages is equal to zero. The blue curve in Fig.3.4shows the output of a TRAN simulation of an example conducted immunity test bench under the RF disturbance at 850 MHz, starting from the DC operating point that is defined in the DC simulation run. The RF voltage signal labelled as $v_{BG\_INT}(t)$ converges towards the steady-state by decreasing the mean value. However, the steady-state is not reached even after 1000 periods of the RF signal.

The PSS solver enables avoiding the long transients by directly finding the solution of the circuit differential equations that corresponds to the steady-state. The output of the PSS simulation consists of a single period of all voltages and currents in the test bench in the steady-state [7]. The red curve in Fig.3.4shows the output of the TRAN simulation that starts from the initial condition defined by the PSS simulation of the same test bench. The steady-state is reached immediately, and it is maintained indefinitely.

The main disadvantage of the PSS solver is that behavioural models are not supported. The behavioural models connected to transistor-level circuits that exhibit very long transients before reaching the steady-state are therefore evaluated using the TRAN solver starting from the initial condition obtained by the PSS simulation of the transistor-level test bench.

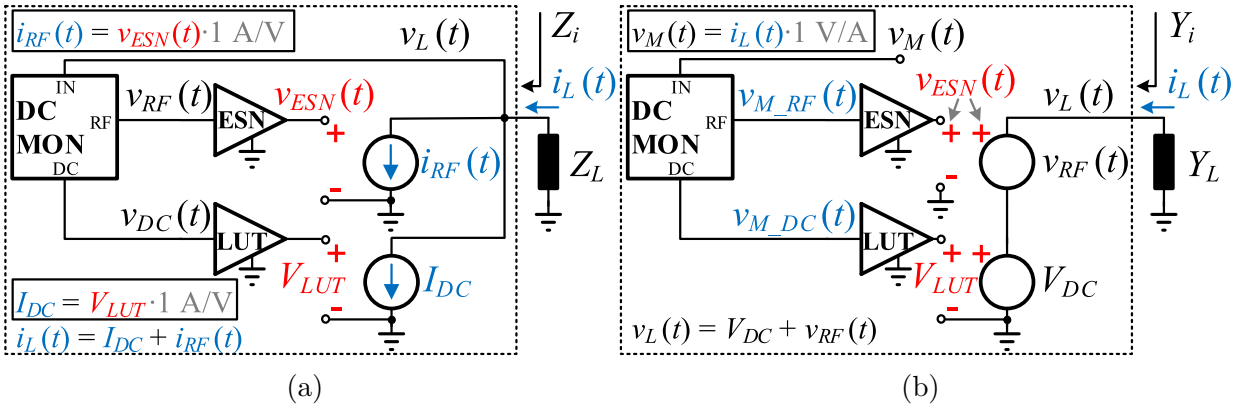


Figure 3.5: The extended nonlinear impedance model architecture that enables modelling the DC and RF behaviour of the modelled circuit independently, using separate DC and RF sub-models: (a) based on voltage-controlled current sources, (b) based on current-controlled voltage sources [38].

Due to these constraints that are specific to the conducted immunity simulation environment, the behavioural models are required to converge to the correct DC operating point in two scenarios: (i) in the DC simulation that precedes the TRAN simulation, and (ii) in the TRAN simulation that starts from a given initial condition. In the first approach to implement these requirements, the ESN training dataset is extended to include the time-domain waveforms observed at low RF forward power levels, that correspond to the single DC operating point of the conducted immunity simulation test bench.

This approach is used to build the behavioural model instances presented in Section3.5.1that converge to the correct DC operating point in the DC simulation, and it is observed that other behavioural model instances converge to an incorrect DC operating point. This behaviour is linked to the DC solvers, such as *gmin*, *dptran*, that explore a wide range of DC voltage-current points to find a stable DC operating point [50], [51].

Applying an untrained DC value to the input of a given ESN model instance during the DC simulation generates an untrained DC output signal, that is defined by the randomly generated coefficients of the input and internal weight matrices, and the trained output weight matrix coefficients. The untrained DC characteristic of the behavioural model may cause the DC solver to converge to an incorrect DC operating point.

Fig.3.5apresents the extension of the nonlinear impedance model architecture based on the voltage-controlled current source shown in Fig.3.2a, that enables independently modelling the DC and RF behaviour of the modelled circuit using separate DC and RF sub-models. The DC sub-model defines DC characteristic of the behavioural model in a wide range of DC conditions, and it is decoupled from the RF sub-model that defines the model behaviour in the RF conditions. The monitored voltage v_L is separated into the DC and RF components using the DC monitor block DC MON that implements the expressions given in Eq. (3.5):

$$v_{DC}(t) = \begin{cases} v_{IN}(t=0) & \text{in the TRAN simulation} \\ V_{IN} & \text{in the DC simulation} \end{cases} \tag{3.5}$$
$$v_{RF}(t) = v_{IN}(t) - v_{DC}(t)$$

In the TRAN simulation, the DC component v_{DC} is assigned the initial value $v_{IN}(0)$ of the voltage at the DC MON input, that is determined by the preceding DC simulation. In this way, the DC component v_{DC} of the monitored voltage $v_L(t)$ is continuously available.

The DC component v_{DC} is fed to the look-up table (LUT) that contains the DC values I_{DC} of the pin current i_L as a function of a wide range of DC values V_{DC} of the monitored voltage v_L, that are obtained by DC simulations of the transistor-level circuit.

The RF component v_{RF} of the voltage v_{IN} at the DC MON input is defined as the difference between its instantaneous value $v_{IN}(t)$ and its DC component $v_{DC}(t)$. The RF component v_{RF} is fed to the ESN model that is trained to model the RF component i_{RF} of the modelled pin current i_L as a nonlinear function of the RF component v_{RF} of the monitored voltage v_L, that is obtained by PSS simulations of the transistor-level circuit. The modelled pin current $i_L(t)$ is defined additively, as a parallel combination of the DC and RF sub-models output currents.

Fig.3.5bpresents the extension of the dual nonlinear impedance model topology based on the current-controlled voltage source shown in Fig.3.2b. The monitored pin current i_L is converted to the voltage v_M with the same instantaneous value, and it is fed to the DC monitor block. The DC and RF components v_{M_DC} and v_{M_RF} of the voltage v_M are defined by the DC monitor block, and are fed to the LUT and ESN models. The pin voltage v_L is defined additively, as a series combination of the DC and RF sub-model output voltages. During the DC simulation preceding the TRAN simulation, the voltage V_{IN} at the DC MON input is a DC signal that directly defines the DC output V_{DC} of the DC monitor block. Differentiating between the TRAN and DC simulations is enabled by the *analysis* statement in the hardware description language Verilog A, according to the basic implementation of the DC monitor block presented in Listing3.1:

Listing 3.1: The basic DC monitor block implementation in Verilog A.

```
@ (initial_step) val_dc = V(VIN,gnd);
if (analysis("dc"))
    V(VDC,gnd) <+ V(VIN,gnd);
else
    V(VDC,gnd) <+ val_dc;
V(VRF,gnd) <+ V(VIN,gnd) - V(VDC,gnd);
```

In the TRAN simulation, the initial value of the voltage $v_{IN}(0)$ at the DC MON input is stored in the real variable *val_dc* using the @(*initial_step*) statement, and it is assigned to the DC output voltage v_{DC}. In the DC simulation, the DC output voltage v_{DC} is assigned the DC value of the DC signal V_{IN} at the DC MON input, and the RF output $V_{RF}(t)$ of the DC monitor block, that is defined as the difference between the monitored voltage v_L or i_L and the DC output v_{DC}, is equal to zero. Since the DC operating point is defined additively by the LUT model and the ESN model that is fed the 0 V DC input value V_{RF} in the DC simulation, the ESN should generate a zero DC output voltage for a zero DC input voltage.

In the first approach to guarantee a zero ESN output voltage in the DC simulation, the *analysis*-statement in Verilog A is used to disconnect the ESN model from the behavioural output during the DC simulation. Disconnecting the ESN output during the DC simulation also sets the activation voltages of the internal units in the ESN hidden layer to zero in the moment $t = 0$ of the TRAN simulation. The initial output of the ESN model with all internal unit activations set to zero may cause the behavioural model to start the TRAN simulation from an untrained state that may not converge to the expected steady-state. Since the DC simulation also finds the stable DC operating point of the neurons in the ESN hidden layer under the zero-input condition, which is non-zero in the general case, the ESN model is always connected to the output of the behavioural model, and the ESN training dataset is extended to include the narrow DC condition to generate a zero DC output for a zero DC input.

According to the above discussion, the DC monitor block is also required to converge to the correct DC operating point if the TRAN simulation starts from an initial condition defined by a circuit state file instead of a DC simulation. The basic DC monitor block implementation in Listing3.1does not support initial condition files, as the LUT model is fed the final instantaneous value $v_L\left(t_{final}\right)$ of the monitored voltage v_L defined in the circuit state file, instead of its DC value V_L in the DC operating point Q defined by the DC simulation. Depending on the exact RF phase of v_L at $t = t_{final}$, an incorrect DC component of the driven supply current I_{DC} is generated, resulting in an incorrect RF output $v_{RF}(t)$ of the DC monitor that is fed to the ESN model. Since the ESN is trained to react to the RF component of the monitored signal defined against the DC operating point Q, the ESN behaviour exits the trained range and generates an erroneous RF component of the driven output current $i_{RF}(t)$. In order to enable using initial condition files, the DC monitor block implementation in Listing3.1is extended using the Verilog A code snipped given in Listing3.2:

Listing 3.2: The DC monitor block implementation in Verilog A that supports initial conditions.

```
@ (initial_step) begin
 if (analysis("dc") || (V(VIN_IC,gnd)==0)) begin
  val_dc = V(VIN,gnd);
  initCond = 0;
 end
 else begin
  val_dc = V(VIN_IC,gnd);
  initCond = 1;
 end
end
if (analysis("dc")) begin
 V(VDC,gnd) = V(VIN,gnd);
 V(VIN_IC,gnd) <+ 0.0;
end
else begin
 V(VDC,gnd) <+ val_dc;
 if (($abstime==0.0) && (initCond==0))
  V(VIN_IC,gnd) <+ 0.0;
 else if ($abstime > 0.0)
  V(VIN_IC,gnd) <+ V(VDC,gnd);
end
V(VRF,gnd) <+ V(VIN,gnd) - V(VDC,gnd);
```

An additional internal node V_{L_IC} is defined to handle the initial condition file that contains the correct DC value determined by the DC simulation that precedes the transient simulation. If the DC monitor block is run in a DC simulation, the DC monitor V_{DC} is assigned the monitored DC voltage V_L, and V_{L_IC} is assigned 0 V, regardless of the initial condition file. In the initial step of the TRAN simulation, the flag variable *initCond* detects if the initial condition file is provided or not by observing the value assigned to the V_{L_IC} node, that is defined as follows. In the moment $t = 0$, defined by the variable $\$abstime$, the internal node V_{L_IC} has no contribution statement, making it a high-Z node at $t = 0$. In this way, if an initial condition file is provided, a non-zero initial voltage is assigned to the initial condition node V_{L_IC}, and otherwise it is assigned the value 0 V. The real variable *val_dc* is assigned the value of the monitored voltage V_L if the DC monitor is run in the DC simulation, or if no initial condition is provided. Otherwise, it is assigned the value in V_{L_IC} that is defined by the initial condition file. This extension of the basic DC monitor block implementation in Listing3.1is presented because it enables evaluating the behavioural models that are connected to transistor-level circuits that exhibit long transients before reaching the steady-state. The full implementation of the extended behavioural model architecture in Verilog A is given in AppendixA.

3.3 Conducted immunity simulation environment

3.3.1 Buffered voltage reference in the top-level test bench

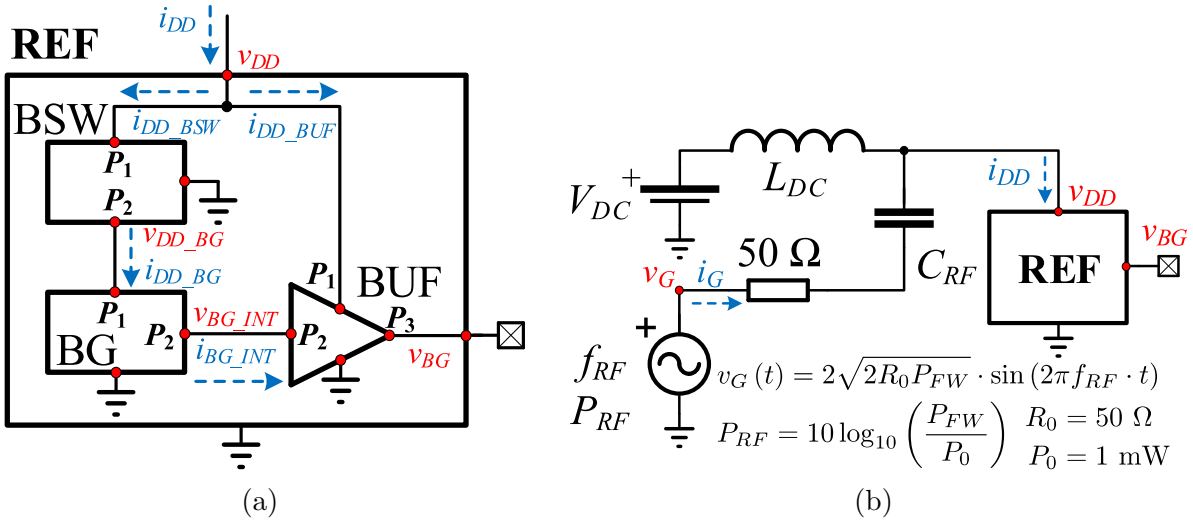


Figure 3.6: (a) The buffered voltage reference circuit (REF), consisting of three subcircuits: bulk switch BSW, bandgap BG, and output buffer BUF, (b) the top-level test bench for simulating injection of a single-tone RF interference signal into the supply pin of the REF circuit using a 50-Ω RF generator and a bias-tee network $V_{DC} = 3.3$ V, $L_{DC} = 430$ µH, $C_{RF} = 6.8$ nF [38].

The nonlinear impedance model architecture presented in Section3.2is applied to the block-wise behavioural modelling of an industrial buffered voltage reference integrated circuit REF shown in Fig.3.6a. The REF circuit consists of three subcircuits: the bulk switch BSW, the bandgap block BG, and the output buffer BUF. The supply voltage v_{DD_BG} of the BG circuit is supplied by the BSW circuit, and the BG output voltage v_{BG_INT} is buffered by the BUF circuit that generates the buffered reference voltage v_{BG}. The same supply voltage v_{DD} supplies the BSW and BUF circuits, and the supply currents of each subcircuit are labelled as: i_{DD_BSW}, i_{DD_BG}, i_{DD_BUF}. The total REF supply current i_{DD} is the sum of i_{DD_BSW} and i_{DD_BUF}. The BG circuit output current i_{BG_INT} is equal to zero in DC conditions and has non-zero instantaneous values in RF conditions. The buffered voltage reference is modelled without an output load.

The conducted immunity of the REF circuit is simulated in the time-domain by injecting a single-tone RF interference signal into its supply pin v_{DD} using the top-level simulation test bench based on the Direct RF Power Injection (DPI) standard [28] shown in Fig.3.6b. The effect of the RF interference on the voltages and currents within the test bench is observed as a function of the RF forward power level P_{RF} and the RF frequency f_{RF}, that are linked to the RF source frequency and amplitude by the expressions given in Fig.3.6b. The 50-Ω RF generator is coupled to the supply pin of the REF circuit through a bias-tee network that consists of an ideal inductor L_{DC} towards the DC voltage

source V_{DC}, and an ideal RF injection capacitor C_{RF} towards the RF generator. The value of the inductor L_{DC} is set to 430 µH in order to achieve an impedance of at least 400 Ω towards the DC voltage source V_{DC} in the full bandwidth from 150 kHz to 1 GHz, and the injection capacitor C_{RF} is set to the default value of 6.8 nF that is recommended in the DPI standard [28]. For a given (f_{RF}, P_{RF}) point, the test bench is simulated in the time-domain using either the transient (TRAN) solver, or the periodic steady state (PSS) solver, according to the discussion in Section3.2.2.

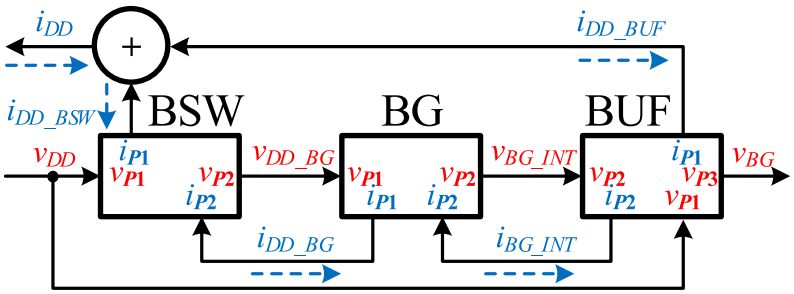


Figure 3.7: The flow-diagram of the REF circuit in the top-level test bench, showing the pin voltages and currents for each modelled circuit that are split into the monitored ESN input signals and the driven ESN output signals, as indicated by the direction of the solid arrows [38].

Fig.3.7shows the signal flow-diagram of the REF circuit, with the selected monitored and driven signals for each modelled subcircuit indicated by the direction of the solid arrows, according to the methodology presented in Section3.2.1. For the BSW circuit, the BSW supply current i_{DD_BSW} and the BG supply voltage v_{DD_BG} are selected as the ESN output signals that are driven as functions of the monitored supply voltage v_{DD} and the monitored BG supply current i_{DD_BG}, according to Eq. (3.6):

$$\begin{aligned} i_{DD\_BSW} &= i_{BSW\_P1}\left(v_{BSW\_P1}, i_{BSW\_P2}\right) \\ v_{DD\_BG} &= v_{BSW\_P2}\left(v_{BSW\_P1}, i_{BSW\_P2}\right) \\ v_{BSW\_P1} &= v_{DD}, \;\; i_{BSW\_P2} = -i_{DD\_BG} \end{aligned} \tag{3.6}$$

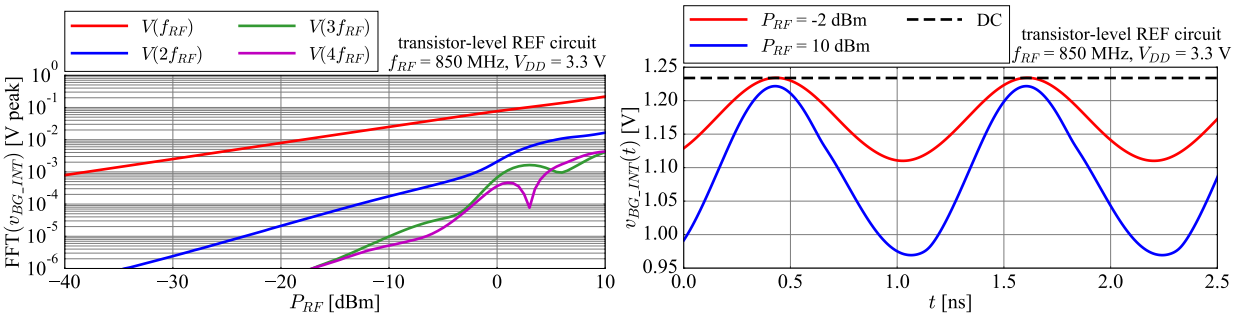
According to the convention defined in Section3.2.1, the monitored pin current i_{BSW_P2} flows into the BSW circuit by definition, and it is equal to the negative current i_{DD_BG} that flows outwards from the BSW circuit, as indicated by the dashed arrow in Fig.3.7. The ESN input and output signals of the BG circuit are defined analogously to the BSW circuit, such that the BG supply current i_{DD_BG} and the BG output voltage v_{BG_INT} are driven as functions of the monitored BG supply voltage v_{DD_BG} and the BG output current i_{BG_INT}, according to Eq. (3.7):

$$\begin{aligned} i_{DD\_BG} &= i_{BG\_P1}\left(v_{BG\_P1}, i_{BG\_P2}\right) \\ v_{BG\_INT} &= v_{BG\_P2}\left(v_{BG\_P1}, i_{BG\_P2}\right) \\ v_{BG\_P1} &= v_{DD\_BG}, \;\; i_{BG\_P2} = -i_{BG\_INT} \end{aligned} \tag{3.7}$$

The BUF circuit is a voltage follower implemented using an operational amplifier with a non-inverting unity-gain feedback loop. The supply current i_{DD_BUF}, the input current i_{BS_INT}, and output voltage v_{BG} of the BUF circuit are selected as the ESN output signals that are driven as functions of the monitored BUF supply voltage v_{DD} and input voltage v_{BG_INT}, according to Eq. (3.8):

$$\begin{aligned} i_{DD\_BUF} &= i_{BUF\_P1}\left(v_{BUF\_P1}, v_{BUF\_P2}\right) \\ i_{BG\_INT} &= i_{BUF\_P2}\left(v_{BUF\_P1}, v_{BUF\_P2}\right) \\ v_{BG} &= v_{BUF\_P3}\left(v_{BUF\_P1}, v_{BUF\_P2}\right) \\ v_{BUF\_P1} &= v_{DD}, \;\; v_{BUF\_P2} = v_{BG\_INT} \end{aligned} \tag{3.8}$$

3.3.2 Nonlinear effects in conducted immunity simulations



(a) (b)

Figure 3.8: RF forward power sweep simulation of the transistor-level REF circuit in the top-level test bench from -40 dBm to 10 dBm at a constant RF frequency of 850 MHz of the BG output voltage v_{BG_INT}: (a) harmonic components as a function of RF forward power P_{RF}, (b) time-domain waveforms at the RF forward power levels of -2 dBm and 10 dBm, with the DC operating point value of V_{BG_INT} = 1.23381 V [38].

The main two nonlinear effects observed in the conducted immunity test bench in Fig.3.6are the RF harmonic distortion and the RF-induced DC-shift of the RF voltages and RF currents observed under the RF interference injection into the supply pin of the REF circuit. Fig.3.8ashows the output of an RF forward power sweep simulation of the transistor-level REF circuit in the P_{RF} range from -40 dBm to 10 dBm at a constant RF frequency f_{RF} of 850 MHz, where the harmonic components of the BG output volt-

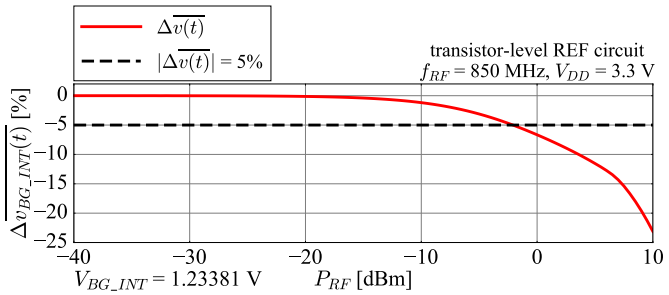


Figure 3.9: The RF-induced DC-shift of the BG output signal v_{BG_INT} as a function of RF forward power P_{RF}, expressed as a percentage of the DC operating point value $V_{BG\_INT} = 1.23381$ V. The limit line of 5% represents a DC-shift of 61.7 mV, and it is crossed at -2 dBm [38].

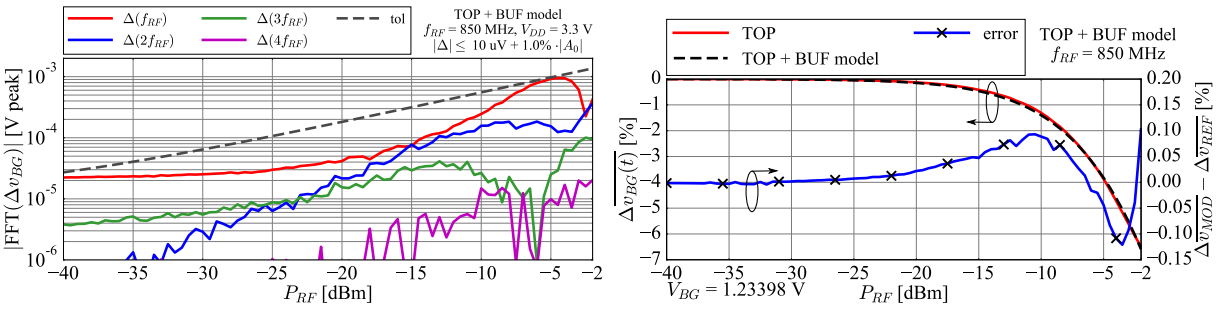
age v_{BG_INT}, that are obtained using the fast Fourier transform (FFT), are plotted as a function of the RF forward power level P_{RF}. For low RF forward power levels P_{RF}, the REF circuit is in the linear regime, where the steady-state RF voltages and RF currents are single-tone sinewaves of the RF generator frequency f_{RF}, with bias levels defined by the DC operating point of the top-level test bench, and with amplitude and phase relationships defined by the small-signal behaviour of the transistor-level subcircuits.

As the RF forward power level P_{RF} is increased, the nonlinearities of the transistor-level subcircuits generate higher order harmonic components at the integer multiples of the RF frequency f_{RF}. Fig.3.8bpresents the RF harmonic distortion observed in the time-domain at two RF forward power levels. At -2 dBm, equivalent to 500 $\mathrm{mV_{pp}}$ on a 50 Ω load, the ratio of the harmonic at $2f_{RF}$ and the fundamental tone of the BG output voltage v_{BG_INT} is equal to -36 dBc. At 10 dBm, equivalent to 2 $\mathrm{V_{pp}}$ on a 50 Ω load, this ratio increases to -22 dBc.

In addition to the RF harmonic distortion, the time-domain waveforms shown in Fig.3.8balso exhibit a significant change in the mean value with increasing RF forward power level P_{RF} due to nonlinear rectification, referred to as the RF-induced DC-shift. Fig.3.9shows the mean value shift of the BUF output voltage v_{BG} as a function of RF forward power P_{RF}. The 5% limit line represents a significant DC-shift of the voltage reference v_{BG} of 61.7 mV, and it is crossed at -2 dBm.

All functional signals of the buffered voltage reference REF are DC signals, and all time-varying signals in the conducted immunity test bench are defined only by the RF interference generator. This class of integrated circuits is appropriate for the feasibility study of the proposed behavioural modelling methodology. Integrated circuits with time-varying functional signals, such as ADCs, exhibit additional nonlinear effects related to the phase relationship between the RF disturbance and the functional signals. The analysis of these effects within transistor-level DPI simulations is presented in AppendixC. Behavioural modelling of this class of integrated circuits is outside of the scope of this work.

3.3.3 Evaluating time-domain waveform modelling accuracy



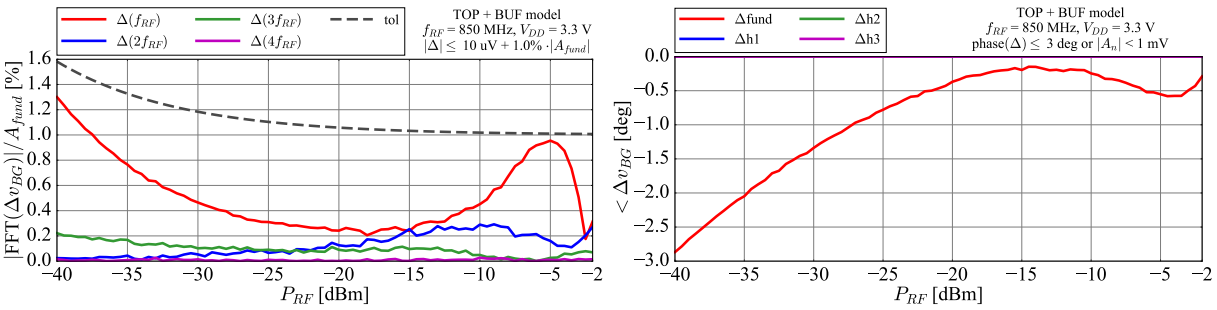
(a) (b)

Figure 3.10: BUF behavioural model accuracy in the RF forward power sweep of the top-level test bench at 850 MHz, for the BUF output voltage v_{BG}: (a) amplitude error per harmonic component, with the error bound of 10 µV plus 1% of the fundamental tone amplitude $|A_0|$, (b) RF-induced DC-shift error as a percentage of the DC value [38].

The behavioural models of the BSW, BG, and BUF subcircuits in the REF circuit are evaluated in the circuit simulator using seven simulation test benches, where one or more transistor-level subcircuits are replaced by their behavioural models. A total of nine RF voltages and RF currents in Fig.3.6aare observed in each test bench as a function of RF forward power P_{RF}, and compared to the transistor-level REF circuit.

The mean square error (MSE) model accuracy measure introduced in Chapter2does not offer insight into the type of model error: mean value error, error in the fundamental tone amplitude, error in the phase relationship, error in the higher order harmonics generated by the circuit nonlinearities, or the presence of artificial harmonics added by the behavioural model, that are not present in the transistor-level circuit. In order to enable a concise overview of these data, each RF signal in a given test bench is analysed using the figures of merit shown in Fig.3.10, that are defined on the example of the BUF output voltage v_{BG_mod} observed in the test bench when the BUF circuit is replaced by its behavioural model.

- For a given (f_{RF}, P_{RF}) point, all time-domain waveforms in the model and reference test benches are synchronized to remove the phase shift between the fundamental tones of the RF voltage for the REF supply voltage v_{DD}.
- Each modelled steady-state voltage and current is evaluated using the methodology presented in Section3.3.2to obtain the harmonic components and the associated RF-induced DC-shift of the modelled waveform as a function of RF forward power P_{RF}, that are compared to the corresponding harmonic components of the reference steady-state voltage. Fig.3.10presents the error amplitude of each harmonic component of $v_{BG\_mod}(t)$, and the RF-induced DC-shift associated with the BUF output voltage v_{BG}.



(a) (b)

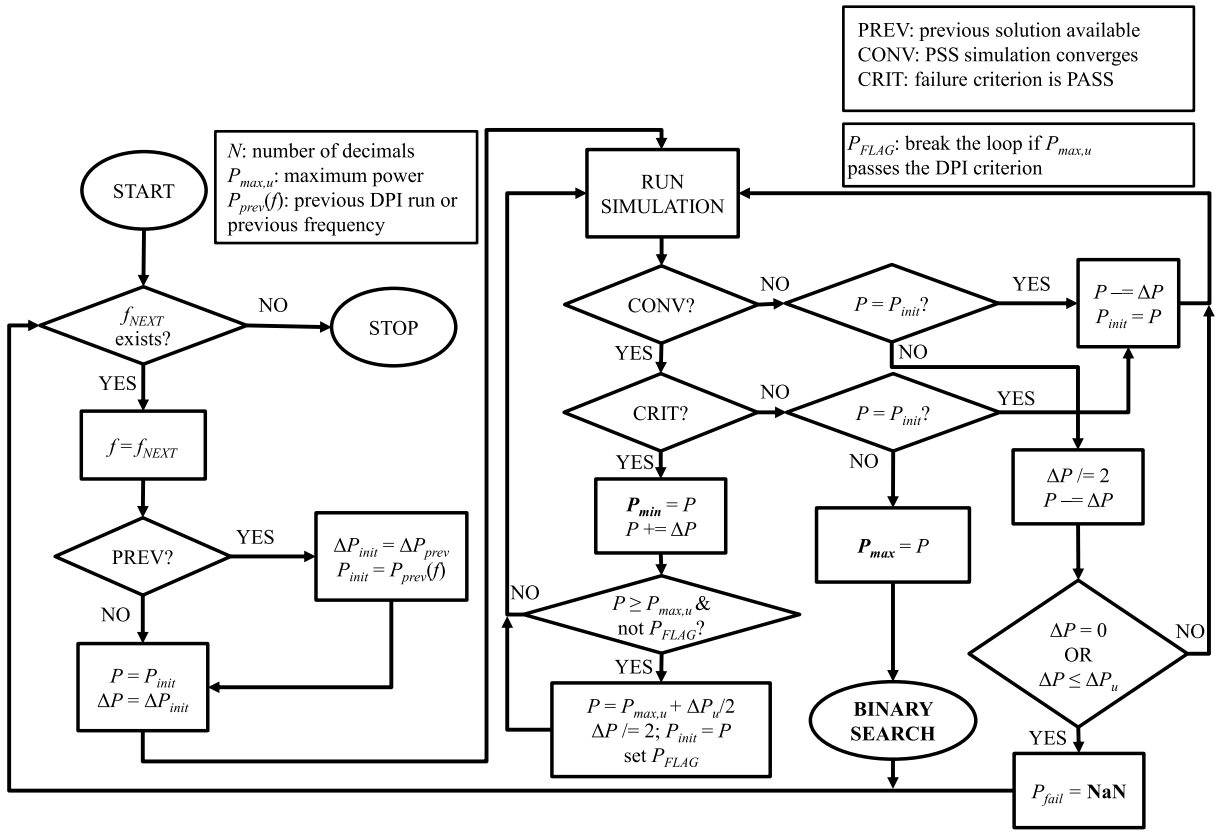
Figure 3.11: Behavioural model accuracy evaluation in the top-level test bench with the BUF behavioural model under an RF forward power sweep at 850 MHz: (a) relative amplitude error in percent, (b) phase error per harmonic component, with the tolerance limit of 3°.

- The amplitude error bound $|\Delta|$ is defined for each evaluated waveform as a percentage of the fundamental tone amplitude $|A_0|$ of the reference waveform, with an absolute minimum error value $|\Delta|_{min}$ for low amplitudes. All harmonic component errors of v_{BG} are bounded by 10 µV plus 1% of the fundamental tone amplitude, and the RF-induced DC-shift error is within 0.2% of the reference DC value of 1.23 V.
- Fig.3.11ashows the relative amplitude error $\left|\Delta/A_0\right|$ and the error bound $|\Delta|$ of v_{BG}, and Fig.3.11bpresents the phase error of the modelled voltage v_{BG} that is bounded by an absolute limit of 3°, for the harmonic components larger than 1 mV.

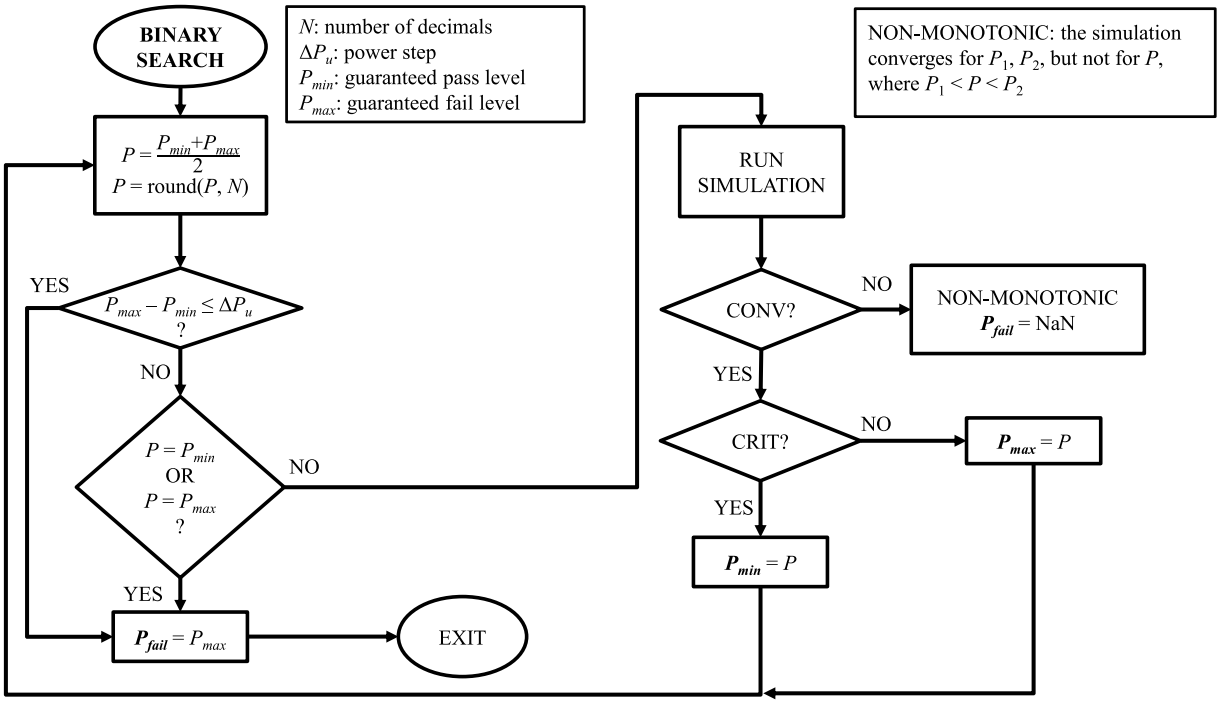
3.3.4 Simulating the Direct RF Power Injection (DPI) standard

According to the procedure outlined in the DPI standard [28], a failure criterion is defined that specifies if the device-under-test (DUT) passes or fails the functionality test at a given (f_{RF}, P_{RF}) point, and the maximum allowed RF forward power level P_{max} is determined at which the DUT passes the functionality test for RF frequency f_{RF} in the range from 150 kHz to 1 GHz [11], [28]. The failure criterion used in the REF circuit conducted immunity test case presented in Section3.3.1is the limit value of the RF-induced DC-shift [11], [36]. Fig.3.12presents the algorithm for finding the maximum RF forward power level P_{max} at which the failure criterion of a given test bench is satisfied as a function of RF frequency f_{RF} using binary search, in order to minimise the number of required PSS or TRAN simulation runs.

In addition to the wideband conducted immunity characterization, the DPI simulation environment is also used to find the root causes of the DUT conducted susceptibility at a system-critical RF frequency, or at the worst-case RF frequency at which the DUT fails the DPI test in the measurement setup. This is done by running narrow-band RF forward power sweep simulations of the DPI test bench [38], with the goal of improving the conducted immunity of the DUT using circuit techniques and/or filtering.



(a)



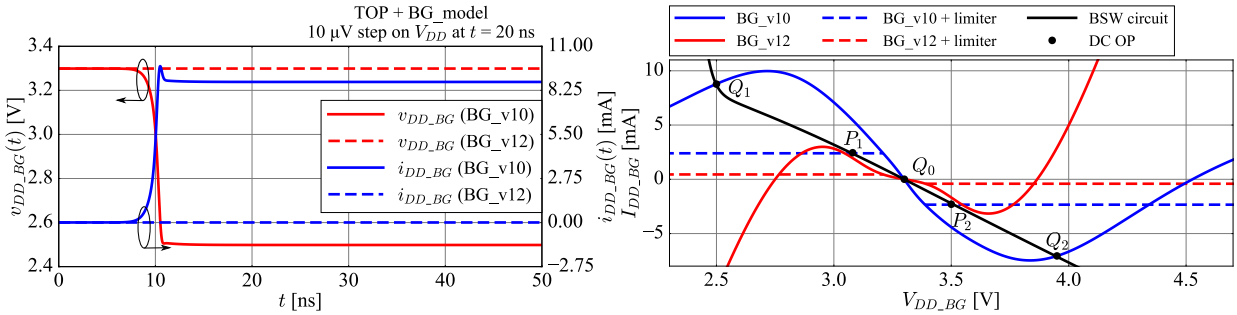
(b)

Figure 3.12: DPI simulation algorithm based on binary search: (a) the outer loop that defines the minimum and maximum limits P_{min}, P_{max}, (b) the binary search sub-routine.

3.4 Beahvioural model stability analysis

Behavioural models built using the nonlinear impedance model architecture presented in Section3.2are nonlinear systems based on the echo state network, a discrete-time system defined in Chapter2. In this section, the stability of the behavioural models connected to transistor-level circuits is analysed using various sub-optimal behavioural model instances of the BSW, BG, and BUF circuits presented in Section3.3. These model instances exhibit different classes of stability issues in the conducted immunity simulation environment. The best performing stable behavioural model instances are presented later in Section3.5.

3.4.1 DC operating point stability



(a) (b)

Figure 3.13: (a) Time-domain behaviour of the BG model instances v10 and v12 in the top-level test bench under a 10 µV step on the REF supply pin at $t = 20$ ns, (b) DC characteristics of the transistor-level BSW circuit, and the BG behavioural model instances v10 and v12 with and without an ESN input voltage limiter [41].

During the block-wise behavioural modelling of the REF circuit in Fig.3.6, several behavioural model instances of the BG subcircuit are built in order to achieve good model accuracy, using the extended model architecture with separate DC and RF sub-models presented in Section3.2.2. The RF sub-model instances are built iteratively using the same training dataset, according to the ESN modelling procedure presented in Chapter2.

Fig.3.13ashows the time-domain behaviour of the BG model instances v10 and v12 in the top-level test bench under a 10 µV step on the REF supply pin at $t = 20$ ns. In the moment $t = 0$, both BG model instances converge to the correct DC operating point Q_0 defined by the BG supply voltage V_{DD_BG} of 3.3 V, and the BG supply current I_{DD_BG} of 7.32 µA. After approximately 7 ns, the BG model instance v10 breaks away into an incorrect DC operating point Q_1 and remains in that point indefinitely, while the BG model instance v12 remains in the correct DC operating point Q_0. The DC operating point stability, referred to as "meta-stability" in [41], is a necessary condition for the large-signal stability of the behavioural model in the top-level test bench.

Fig.3.13bpresents the DC characteristics of the transistor-level BSW circuit and the two BG behavioural model instances, that are obtained by DC simulations of each circuit individually. The stable DC operating points $Q_i\,(V_{DD\_BG}, I_{DD\_BG})$ of the top-level test bench are defined in the intersections of the DC characteristics of the BSW and BG circuits. Both BG model instances produce the correct DC operating point Q_0(3.3 V, 7.32 µA), while the BG model instance v10 introduces two additional, incorrect DC operating points Q_1(2.5 V, 8.77 mA) and Q_2(3.95 V, -7.06 mA).

During the TRAN simulation at $t > 0$, any small shift in the instantaneous voltage $v_{DD\_BG}\,(t)$, including the numerical noise in the circuit simulator, moves the system operating point away from the DC operating point Q_0 by a small amount, allowing the system to re-converge into the incorrect DC operating point Q_1 or Q_2. The DC operating point stability of the behavioural models in the top-level test bench is guaranteed by having a unique intersection of the DC characteristics of the behavioural models and the connected transistor-level circuits. The two BG model instances in Fig.3.13exhibit significantly different DC characteristics that are defined additively by their DC and RF sub-models, according to the discussion in Section3.2.2.

The LUT model implements the DC characteristic in a wide range of DC input voltage values V_{DD_BG}, and the ESN model is trained to generate a zero output current $i_{RF}\,(t)$ for a zero input voltage $v_{RF}\,(t)$, in order to not disturb the DC operating point Q_0 defined by the DC sub-model. In addition to the narrowly and correctly trained DC condition, the ESN model also has an untrained DC characteristic for non-zero DC voltages applied to its input. This untrained part of the DC characteristic is defined by the randomly generated recurrent connections in the ESN hidden layer, and the trained output connections.

In order to avoid extending the ESN training dataset with a wide range of DC conditions, two approaches for removing the incorrect DC operating points from the untrained DC characteristic of the ESN model are explored. In the first approach, a voltage limiter is placed at the input of the ESN model that clips the ESN input voltage to the limited range between -100 mV to 100 mV around the DC operating point Q_0. The resulting DC characteristic of the BG behavioural model instances is shown in Fig.3.13in dashed lines. Since the incorrect DC operating points P_1(3.07 V, 2.45 mA) and P_2(3.51 V, -2.3 mA) are observed in the DC characteristic of the BG model instance v10, it follows that adding an input voltage limiter does not necessarily improve the DC operating point stability.

In the second approach, the unique DC operating point is achieved by iteratively rebuilding the RF sub-model until an acceptable DC characteristic of the ESN model is obtained that has a unique cross-section of the BSW and BG DC characteristics. This approach is enabled by the fast ESN training procedure presented in Chapter2, and it is selected for building behavioural models with stable DC operating points.

3.4.2 Implicit substrate connections

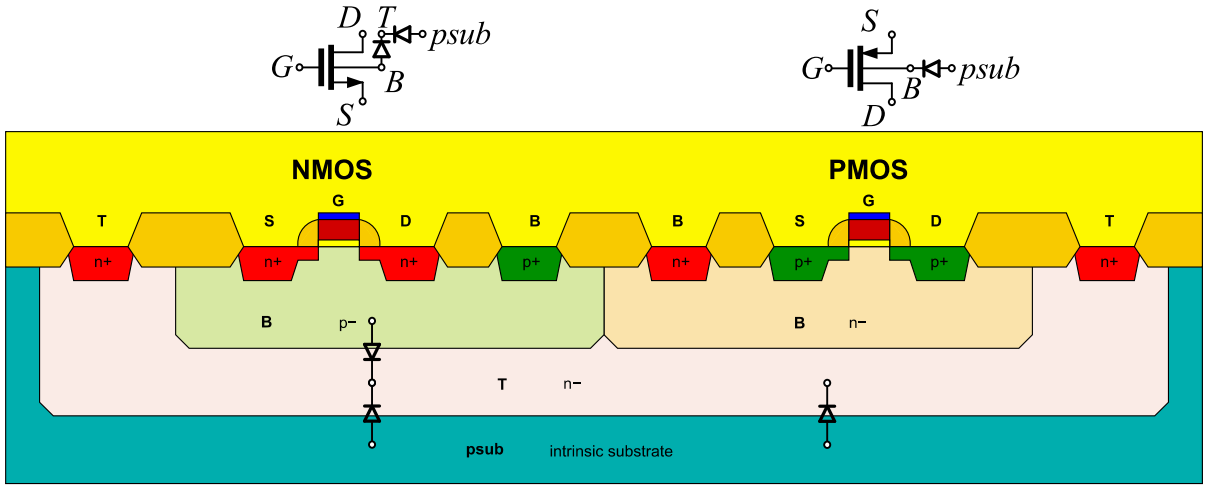


Figure 3.14: Implicit substrate connections between transistors in a generic CMOS technology.

The model architecture presented in Section3.2is based on the assumption that the sum of all RF currents flowing into the modelled transistor-level circuit is equal to zero, because all controlled current sources in the behavioural model sink the RF current from the modelled pin towards the ground pin. Fig.3.14presents the cross-section of a generic CMOS technology with isolated NMOS transistors, and identifies the implicit substrate connections between transistor-level subcircuits that allow the RF current to flow between subcircuits, and may introduce a non-zero RF current balance for an individual subcircuit in the top-level test bench. The behavioural models built using these incorrect RF current waveforms in the training dataset may introduce instabilities in the top-level test bench by driving the incorrect RF current from the other transistor-level subcircuits.

The isolated NMOS transistors are fabricated in individual p-type islands B that are placed in a single n-well T within the p-substrate $psub$. The parasitic capacitance between each isolated p-type island and the n-well, and between the n-well and the p-substrate form an implicit substrate connection between all isolated NMOS transistors in the test bench. An equivalent capacitive connection exists between the n-type bulk terminals B of all PMOS transistors.

If any of the p-substrate, n-well, or n-type bulk nets are assigned to global net names in the circuit netlist, an implicit substrate connection is formed between the subcircuits that appear to be separate in the schematic. In order to avoid this issue, the p-substrate connections $psub$ of each subcircuit are explicitly assigned to the local ground of the subcircuit, and the RF current balance of each modelled transistor-level circuit is verified by PSS simulations prior to constructing the training dataset, as a necessary condition for the stability of the resulting behavioural model in the top-level test bench.

3.4.3 Discrete-time system stability analysis

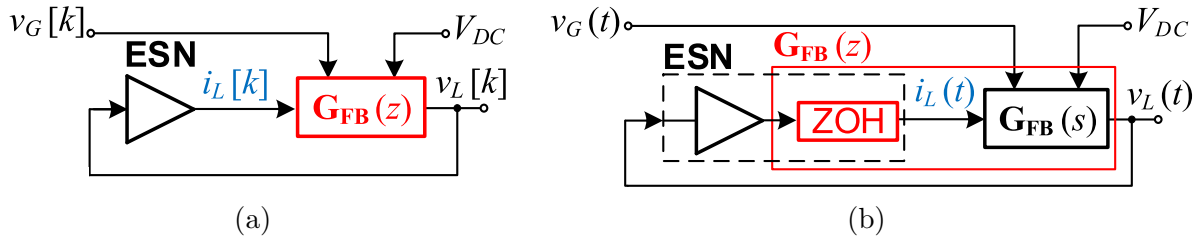


Figure 3.15: The flow-diagrams of the feedback loop in the nonlinear impedance model architecture based on the voltage-controlled current source: (a) in the discrete time-domain, (b) in the continuous time-domain [42].

The bounded-input bounded-output (BIBO) stability of the standalone ESN model as a discrete-time system is discussed in Chapter2, based on the diagonal Schur stability of the internal weight matrix that is derived as a sufficient condition for the echo state property (ESP) in [39]. The stability of the recurrent connections in the ESN hidden layer is confirmed in [9], where the eigenvalues of the linearized ESN model are derived from the coefficients of the internal and output weight matrices, and are shown to be within the unit circle in the complex z-domain.

In addition to the BIBO stability of the ESN model, the stability of the behavioural model is determined by the stability of the feedback loops defined in Fig.3.2by the ESN model and the controlled sources through Eqs. (3.2) and (3.3). Since the ESN model is a discrete-time system and the transistor-level circuits are continuous-time systems, two approaches to the stability analysis of the nonlinear impedance model are explored.

Fig.3.15shows the flow-diagrams in the discrete time-domain and in the continuous time-domain that represent the feedback loop associated with the same behavioural model of the nonlinear impedance seen looking into port P_1 of the BG circuit. The modelled BG circuit is simulated in the top-level test bench shown in Fig.3.6, and the model is built using the ESN and a voltage-controlled current source (VCCS) according to Fig.3.2a.

In Fig.3.15a, the nonlinear function f_{ESN} of the ESN model drives the pin current samples $i_L[k]$ in the discrete time-domain as a function of the samples $v_L[k]$ of the pin voltage $v_L(t)$ sampled at $t = kT_s$. The pin voltage $v_L(t)$ is defined in the continuous time-domain through the linearized transfer function $\mathbf{G_{FB}}(s)$ in Fig.3.15b, as a function of the pin current $i_L(t)$, the RF generator voltage $v_G(t)$, and the DC supply voltage V_{DC}.

The interaction between the discrete-time ESN model and the continuous-time transfer function $\mathbf{G_{FB}}(s)$ is enabled by the zero-order hold (ZOH) block that defines the pin current $i_L(t)$ in the continuous time-domain as a piecewise-constant signal using the discrete-time samples of the pin current $i_L[k]$, according to [52].

These relationships are summarized in Eq. (3.9), where $\mathcal{L}^{-1}$ is the inverse Laplace transform, $\mathcal{Z}^{-1}$ is the inverse Z-transform, and $*$ is the convolution operator:

$$\begin{aligned} &i_L[k] = f_{ESN}\left(v_L[k]\right), \quad i_L(t) = i_L[k]\,|_{k=\lfloor t/T_s \rfloor}, \quad v_L[k] = v_L(t)\,|_{t=kT_s} \\ &v_L(t) = f_{FB}\left(v_G(t), i_L(t), V_{DC}\right) = \mathcal{L}^{-1}\left\{\mathbf{G_{FB}}(s)\right\} * \left[v_G(t); i_L(t); V_{DC}\right] \\ &v_L[k] = \mathcal{Z}^{-1}\left\{\mathbf{G_{FB}}(z)\right\} * \left[v_G[k]; i_L[k]; V_{DC}\right] \end{aligned} \tag{3.9}$$

Depending on the grouping of the ZOH block in Fig.3.15b, two approaches to the stability analysis of the feedback loop in the nonlinear impedance model are identified.

In the first approach shown in Fig.3.15b(solid red line), the ZOH block is grouped with the continuous-time transfer function $\mathbf{G_{FB}}(s)$. The resulting discrete-time transfer function $\mathbf{G_{FB}}(z)$ in Fig.3.15agenerates the discrete-time samples of the pin voltage $v_L[k]$ as a function of the discrete-time samples of the pin current $i_L[k]$ and the RF generator voltage $v_G[k]$, according to Eq. (3.9). The stability of the resulting discrete-time feedback loop is defined by the positions of the closed-loop poles in the complex z-domain relative to the unit circle, which are derived as follows.

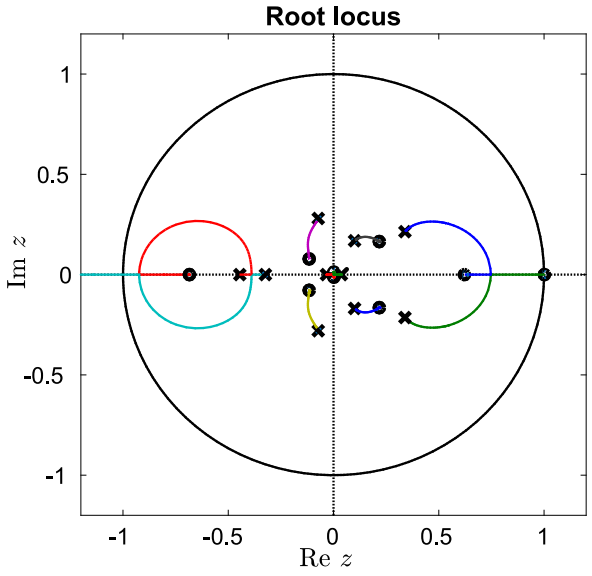


Figure 3.16: The root locus of a discrete-time system with 10 poles and 10 zeroes obtained using MATLAB®. The open-loop poles are marked by crosses and the open-loop zeroes are marked by circles [42].

Based on the root locus method from [52], the closed-loop poles are uniquely defined by the known eigenvalues of the linearized ESN model, the known poles and zeroes of the transfer function $\mathbf{G_{FB}}(z)$, and by the strength of the feedback loop that is defined by the loop gain K_L. Fig.3.16presents the root locus of an example discrete-time system with 10-poles and 10 zeroes, and a feedback connection with an adjustable loop gain K_L.

As the strength of the feedback connection is increased by increasing the loop gain K_L, the closed-loop poles follow the curves that originate in the open-loop poles marked by crosses for $K = 0$, and tend towards the open-loop zeroes marked by circles, as $K \to \infty$. Since one open-loop zero of the example system is located outside of the unit circle, the critical loop gain K_{L_cr} exists for which a closed-loop pole exits the unit circle, making the feedback loop unstable. A method for obtaining the poles in the z-domain using the simulated frequency domain data is proposed in AppendixD, based on [43].

In the second approach shown in Fig.3.15b(dashed line), the ZOH block is grouped with the ESN model. The resulting continuous-time system generates the piecewise-constant pin current $i_L(t)$ as a function of the discrete-time samples $v_L[k]$ of the continuous-time pin voltage $v_L(t)$ sampled at $t = kT_s$, where T_s is the uniform sampling time. The continuous-time transfer function $\mathbf{G_{FB}}(s)$ defines the pin voltage $v_L(t)$ as a function of the pin current $i_L(t)$ and the RF generator voltage $v_G(t)$, according to Eq. (3.9). The stability of the continuous-time feedback loop is determined by the positions of its closed-loop poles relative to the left half-plane (LHP) of the complex s-domain [43]. The closed-loop poles are defined by the poles of each transistor-level subcircuit and behavioural model in the test bench, which are derived from the associated frequency responses.

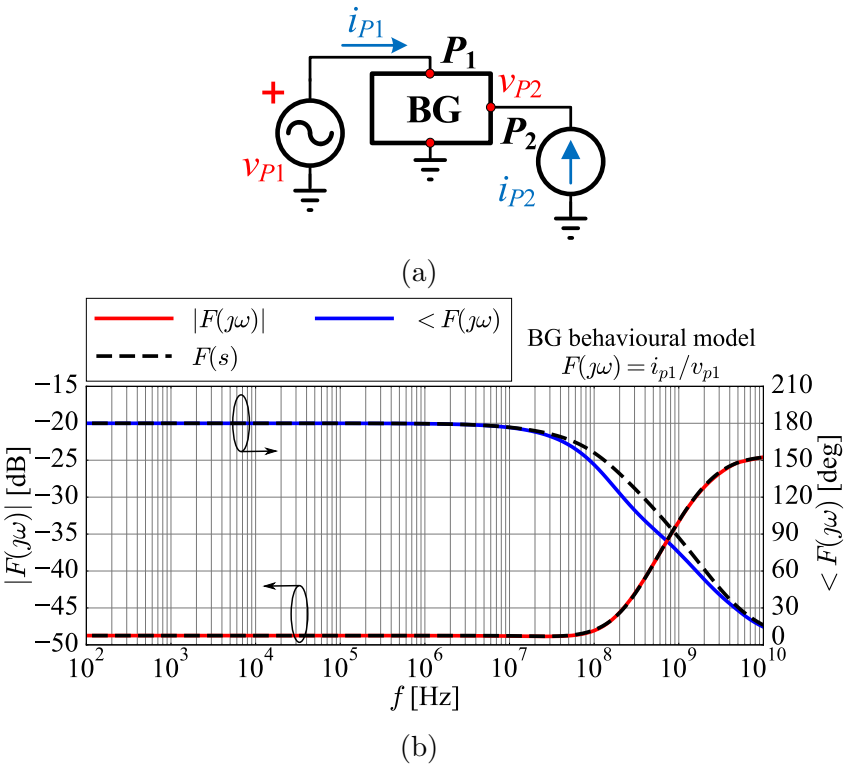


Figure 3.17: (a) AC test bench for simulating the small-signal behaviour of the BG behavioural model, (b) frequency response $F(\jmath\omega)$ of the ESN that models the admittance seen looking into the port P_1 of the BG behavioural model (solid lines), and the frequency response of the fitted transfer function $F(s)$ with 3 poles and 3 zeroes (dashed lines).

Fig.3.17apresents the AC test bench used to simulate the small-signal frequency responses associated with the BG behavioural model, according to the selected ESN input and output signals given in Fig.3.7and Eq. (3.7). The frequency response $F(\jmath\omega)$ associated with the transfer function from the BG input voltage v_{BG_P1} to the BG input current i_{BG_P1} obtained by TRAN simulations of the AC test bench is shown in Fig.3.17b in solid lines. This frequency response represents the small-signal impedance seen looking into the port P_1 of the BG behavioural model, and it is obtained as follows:

- The DC operating point $Q(V_{P1}, I_{P2})$ is defined by the DC voltage source at the port P_1 and the DC current source at port P_2. The DC sources are set to the values $V_{P1} = 3.2989$ V and $I_{P2} = 0$ A, that are obtained by running DC simulations of the top-level test bench in Fig.3.6.
- A sinewave voltage source with a small amplitude v_{p1} is placed at the port P_1. The current $i_{P1}(t)$ flowing into the port P_1 and the voltage $v_{P2}(t)$ at the port P_2 are simulated using the PSS or the TRAN simulations of the AC test bench over the frequency range from 100 Hz to 10 GHz.
- The phasors i_{p1} and v_{p2} are obtained by calculating the FFT of current $i_{P1}(t)$ and the voltage $v_{P2}(t)$ for each simulated frequency point. The frequency response $F(\jmath\omega)$ is calculated as the complex-valued ratio of the phasors i_{p1} and v_{p1}.
- The transfer function $F(s)$ is obtained analytically by fitting 3 poles and 3 zeroes in the complex s-domain to approximate the frequency response $F(\jmath\omega)$ obtained by simulations. The frequency response of the fitted transfer function $F(s)$ is shown in Fig.3.17bin dashed lines.
- The frequency responses of the BG behavioural model versus the second ESN input variable i_{P2} are obtained by placing a sinewave current source with a small amplitude i_{p2} at the port P_2. The two ESN output signals $i_{P1}(t)$ and $v_{P2}(t)$ are simulated over the frequency range from 100 Hz to 10 GHz. The resulting phasors i_{p1} and v_{p2} are obtained using FFT, and the frequency responses are obtained as complex-valued ratios of the corresponding phasors.

Compared to the discrete-time analysis, the continuous-time approach avoids the discretization step of the continuous-time transfer functions associated with the transistor-level circuits that are connected to the behavioural model in the top-level test bench. Observing the ESN models as continuous-time systems enables the usage of the above methodology to obtain the associated small-signal frequency responses. Thus, this methodology is selected as the basis for the analysis of the small-signal stability of behavioural models connected to transistor-level subcircuits, that is presented next.

3.4.4 Small-signal stability

The small-signal stability of the feedback loops in the flow-diagram of the REF circuit in Fig.3.7is analysed by linearizing Eqs. (3.6), (3.7), (3.8) around the DC operating point Q, according to Eqs. (3.10), (3.11), and (3.12):

$$\begin{aligned} i_{dd\_bsw} &= \left.\frac{\partial i_{BSW\_P1}}{\partial v_{BSW\_P1}}\right|_Q \cdot v_{dd} - \left.\frac{\partial i_{BSW\_P1}}{\partial i_{BSW\_P2}}\right|_Q \cdot i_{dd\_bg} \\ v_{dd\_bg} &= \left.\frac{\partial v_{BSW\_P2}}{\partial v_{BSW\_P1}}\right|_Q \cdot v_{dd} - \left.\frac{\partial v_{BSW\_P2}}{\partial i_{BSW\_P2}}\right|_Q \cdot i_{dd\_bg} \end{aligned} \tag{3.10}$$

$$\begin{aligned} i_{dd\_bg} &= \left.\frac{\partial i_{BG\_P1}}{\partial v_{BG\_P1}}\right|_Q \cdot v_{dd\_bg} - \left.\frac{\partial i_{BG\_P1}}{\partial i_{BG\_P2}}\right|_Q \cdot i_{bg\_int} \\ v_{bg\_int} &= \left.\frac{\partial v_{BG\_P2}}{\partial v_{BG\_P1}}\right|_Q \cdot v_{dd\_bg} - \left.\frac{\partial v_{BG\_P2}}{\partial i_{BG\_P2}}\right|_Q \cdot i_{bg\_int} \end{aligned} \tag{3.11}$$

$$\begin{aligned} i_{dd\_buf} &= \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{dd} + \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{bg\_int} \\ i_{bg\_int} &= \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{dd} + \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{bg\_int} \\ v_{bg} &= \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{dd} + \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{bg\_int} \end{aligned} \tag{3.12}$$

The voltages and currents in lower-case letters, such as v_{dd_bg}, represent small-signal perturbations of the signals in the top-level test bench in Fig.3.6around the DC operating point Q. For the generic circuit BLK, the partial derivative of an output signal at the port i against an input signal at the port j represents the small-signal frequency response labelled as $BLK_{ij}(\jmath\omega)$, that is associated with the transfer function $BLK_{ij}(s)$ in the s-domain. This convention is applied to the BSW, BG, and BUF subcircuits according to the input and output signals and ports defined in Fig.3.7. E.g. the partial derivative of the BSW output voltage v_{BSW_P2} against the BSW output current i_{BSW_P2} is labelled as $BSW_{22}(\jmath\omega)$, and the associated transfer function is labelled as $BSW_{22}(s)$.

The interaction between the connected transistor-level or behavioural model subcircuits in the top-level test bench is defined by the poles and zeroes associated with the closed-form solutions of the perturbation signals at the shared nodes, that are obtained by solving the system of linearized equations Eqs. (3.10), (3.11), (3.12). The closed-form solutions for the ten voltage and current perturbations in the top-level test bench in Fig.3.6 relative to the RF generator voltage source perturbation v_g are derived in AppendixB.

Several behavioural model instances of the BUF subcircuit are built for the RF forward power sweep simulations of the top-level test bench at the RF frequency of 850 MHz, described in Section3.3.2. The ESN training dataset is constructed using the time-domain waveforms obtained by PSS simulations, according to the input and output signal definitions of the BUF circuit given in Fig.3.7.

All BUF behavioural model instances generate accurate output signals when driven by the wanted input signals using piecewise linear (PWL) voltage sources that read from file, analogously to the modelling test cases presented in Chapter2.

When the transistor-level BUF subcircuit is replaced by its behavioural model in the top-level test bench, it is observed that certain BUF model instances generate instability of the resulting test bench, resulting in a divergent TRAN simulation. The stability of a BUF behavioural model instance is determined by the closed-form solutions of all perturbation signals in the test bench. Eq. (3.13) presents the closed-form solution for the BG output voltage perturbation v_{bg_int} relative to the REF supply voltage perturbation v_{dd}:

$$\begin{aligned}
\left[\frac{v_{bg_int}}{v_{dd}}\right](s) &= \frac{f_3(s)}{f_1(s)\cdot f_2(s)} \\
f_1(s) &= 1 + BG_{22}(s)\cdot BUF_{22}(s) \\
f_2(s) &= f_1(s)\cdot\big(1 + BSW_{22}(s)\cdot BG_{11}(s)\big) \\
&\quad - BSW_{22}(s)\cdot BG_{12}(s)\cdot BG_{21}(s)\cdot BUF_{22}(s) \\
f_3(s) &= BSW_{21}(s)\cdot BG_{21}(s)\cdot f_1(s) \\
&\quad - BG_{22}(s)\cdot BUF_{21}(s)\cdot f_2(s)
\end{aligned} \tag{3.13}$$

Replacing the transistor-level BUF subcircuit by its behavioural model is equivalent to replacing the transfer functions $BUF_{ij}(s)$ in Eq. (3.13) by the transfer functions $BUF_{mod\_ij}(s)$ of the used model instance, which are derived from the simulated frequency responses $BUF_{mod\_ij}(\jmath\omega)$ of the model using the procedure in Section3.4.3.

The frequency response $BUF_{mod\_22}(\jmath\omega)$ of the BUF behavioural model instance is shown in Fig.3.18ain solid lines, and the associated transfer function $BUF_{mod\_22}(s)$ is obtained by manually placing the 3 poles and 3 zeroes shown in Fig.3.18bin the s-domain that fit the simulated frequency response $BUF_{mod\_22}(\jmath\omega)$. The frequency response corresponding to the fitted transfer function $BUF_{mod\_22}(s)$ evaluated in $s = \jmath\omega$ is shown in Fig.3.18ain dashed lines. One zero and all three poles of the BUF behavioural model are in the left half-plane (LHP), and two zeroes are in the right half-plane (RHP) of the complex s-domain. This BUF behavioural model instance is therefore stable as a standalone element driven by PWL voltage sources, as it is guaranteed by the sufficient condition for the BIBO stability of the ESN model.

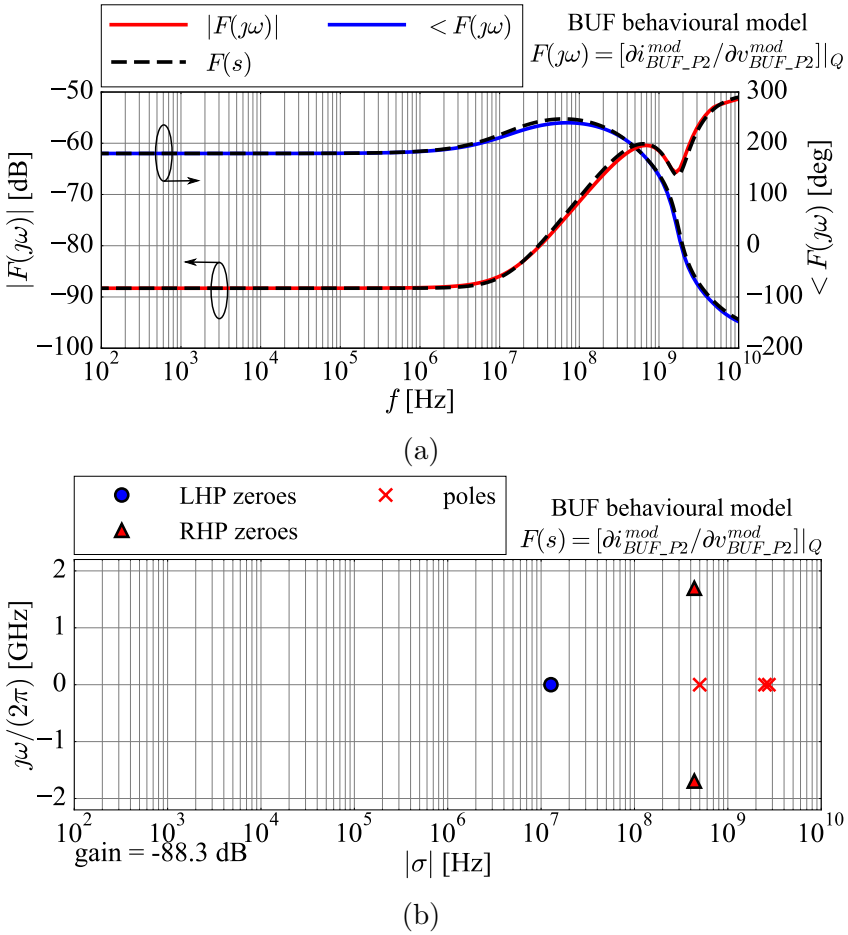


Figure 3.18: (a) Frequency response $BUF_{mod\_22}(j\omega)$ of the transfer function from the input voltage v_{BUF_P2} to the input current i_{BUF_P2} of the BUF behavioural model, obtained by simulations (solid lines), and the frequency response of the fitted transfer function with the poles and zeroes shown in (b) (dashed lines), (b) positions of the 3 poles and 1 zero in the LHP, and the 2 zeroes in the RHP of the s-domain of the analytical small-signal mode $BUF_{mod\_22}(s)$ [38].

The frequency responses $BLK_{ij}(j\omega)$ and the fitted transfer functions $BLK_{ij}(s)$ of the transistor-level BSW, BG, and BUF subcircuits are derived in AppendixB. The poles and zeroes associated with the closed-form solution for v_{bg_int} in Eq. (3.13) are calculated from the known transfer functions $BLK_{ij}(s)$ of each transistor-level and behavioural model subcircuit in the test bench using the following procedure.

The polynomials in the variable s of the numerator and the denominator of the closed-form solution for v_{bg_int} in Eq. (3.13) are calculated using the symbolic library SymPy [53] and the scientific libraries Numpy [54] and SciPy [55] available in Python. Since the transfer function $BUF_{22}(s)$ appears in the denominator of the expression, the poles associated with the perturbation voltage v_{bg_int} are partially defined by the zeroes of the transfer function $BUF_{22}(s)$. In this way, the two RHP zeroes of the BUF behavioural model transfer function $BUF_{mod\_22}(s)$ shown in Fig.3.18bgenerate four unstable RHP poles of the perturbation voltage v_{bg_int} in Eq. (3.13).

As the unstable RHP poles of the closed-form solution are triggered by any voltage change during the TRAN simulation, including numerical noise, exponentially increasing values of the unstable perturbation voltage v_{bg_int} are generated and the TRAN simulation diverges. It is noted that RHP zeroes of the behavioural model do not necessarily generate unstable RHP poles, and that the behavioural models without RHP zeroes may generate unstable RHP poles associated with the closed-form solutions of certain perturbation signals in the top-level test bench.

A behavioural model instance is stable in the top-level test bench if all poles associated with the closed-form solutions of all perturbation signals in the test bench are in the left half-plane of the s-domain. The BG model instance ver-A with sub-optimal accuracy is presented next, that is stable in the top-level test bench. The model is built using the time-domain signals obtained in the same RF forward power sweep simulation at 850 MHz that is used when the unstable BUF behavioural model instance above is built.

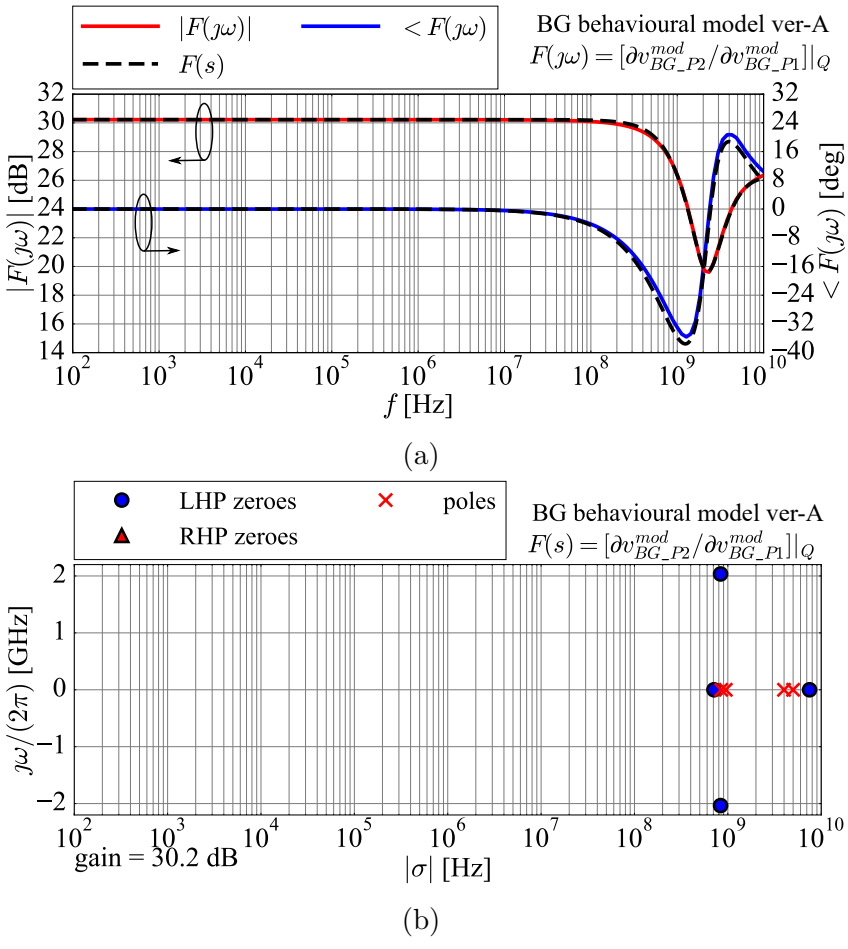


Figure 3.19: (a) Frequency response $BG_{mod\_21}(j\omega)$ of the transfer function from the supply voltage v_{BG_P1} to the output voltage v_{BG_P2} of the BG behavioural model instance ver-A, obtained by simulations (solid lines), and the frequency response of the fitted transfer function with the poles and zeroes shown in (b) (dashed lines), (b) positions of the 4 poles and 4 zeroes in the LHP of the s-domain of the analytical small-signal model $BG_{mod\_21}(s)$ [38].

Fig.3.19apresents the frequency response $BG_{mod\_21}(j\omega)$ (solid line) associated with the transfer function $BG_{mod\_21}(s)$ (dashed line) obtained by fitting the 4 poles and 4 zeroes shown in Fig.3.19b. All poles and all zeroes are in the LHP of the complex s-domain, indicating the BIBO stability of the BG model instance ver-A as a standalone element. When the transfer functions $BG_{ij}(s)$ in Eq. (3.13) and in the other closed-form solutions are replaced by the transfer functions $BG_{mod\_ij}(s)$, all resulting poles associated with all perturbation signals in the test bench are in the LHP of the complex s-domain, indicating that the behavioural model is also stable in the top-level test bench.

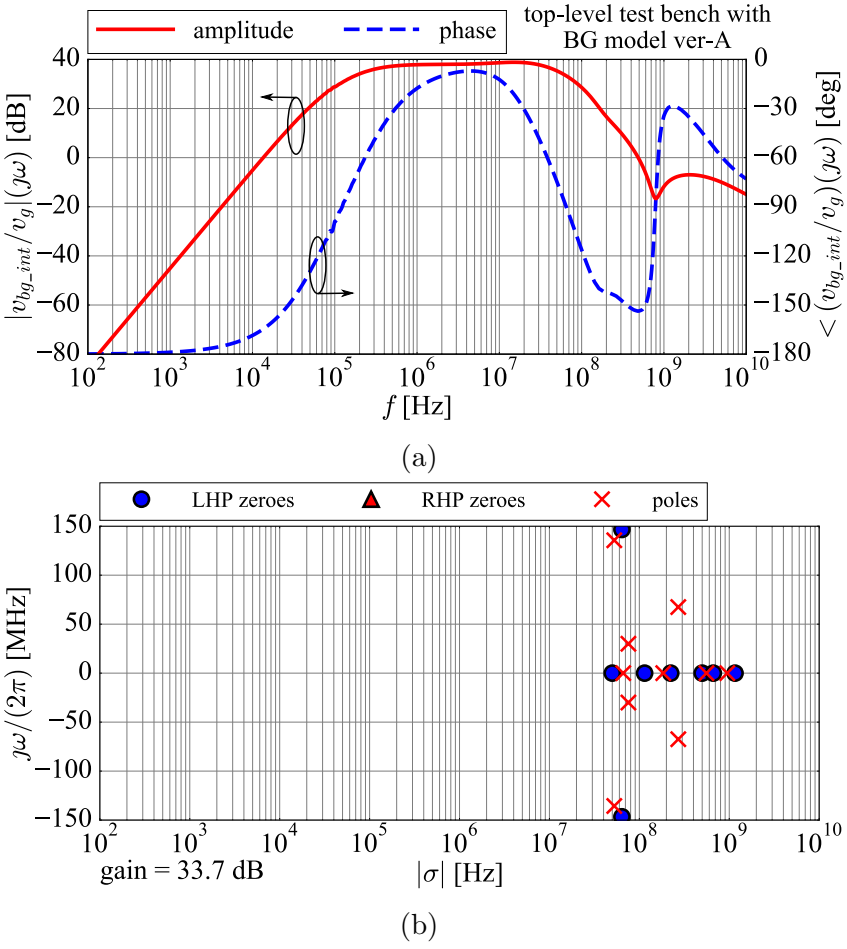


Figure 3.20: (a) Frequency response associated with the closed-form solution of the voltage perturbation v_{bg_int} versus the RF generator v_g in the top-level test bench with the BG behavioural model instance ver-A, (b) analytical small-signal model fitted to the frequency response, with 12 poles and 12 zeros in the LHP of the s-domain [38].

Fig.3.20presents the frequency response and the transfer function associated with the BG output voltage perturbation v_{bg_int} relative to the RF generator perturbation voltage v_g in the test bench with the BG model ver-A. At the trained RF frequency of 850 MHz, the frequency response is equal to -15.8 dB∠-60.9°, while the corresponding value observed in the transistor-level test bench is -18 dB∠-43.2°. The 2.2 dB∠17.7° discrepancy is associated with the sub-optimal accuracy of the BG model ver-A.

The frequency response below 100 kHz is associated with the high-pass transfer function of the bias-tee from the RF generator v_G to the REF supply pin v_{DD} in Fig.3.6.

Outside of the trained RF frequency range, the amplitude response of v_{bg_int} reaches a maximum of 38.9 dB at 14.5 MHz, compared to the maximum of -6.4 dB observed in the transistor-level test bench. It is obvious that this large amplitude response is an unphysical artefact of this particular model instance that appears in the untrained region, and it is associated with the small-signal gain of 30.2 dB observed in the BG behavioural model transfer function $BG_{mod\_21}(s)$ shown in Fig.3.19.

While the steady-state behaviour of the model at the trained narrow-band RF frequency does not depend on the untrained wideband frequency response, the poles and zeroes of the behavioural model transfer functions are defined by the full bandwidth of the behavioural model frequency responses, including in the untrained RF frequency range, by the randomly generated input and internal weight matrices of the ESN models.

Similarly to the approach to achieve DC operating point stability in Section3.4.1, small-signal stability is achieved by iteratively rebuilding the behavioural model if any RHP poles are observed in the calculated closed-form solutions of the top-level test bench perturbation signals. Fig.3.21presents the frequency response of the v_{bg_int} in the test bench with an iteratively re-built BG model instance ver-B. The amplitude response reaches a maximum of 1.9 dB at 285 kHz, compared to 38.9 dB in the BG model ver-A.

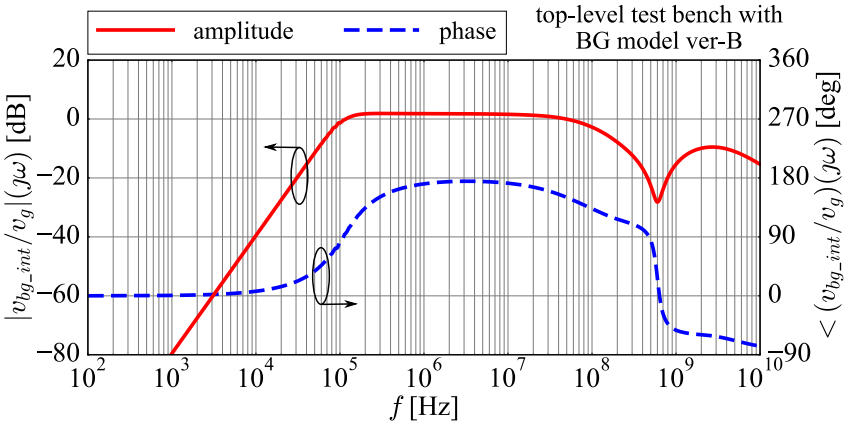
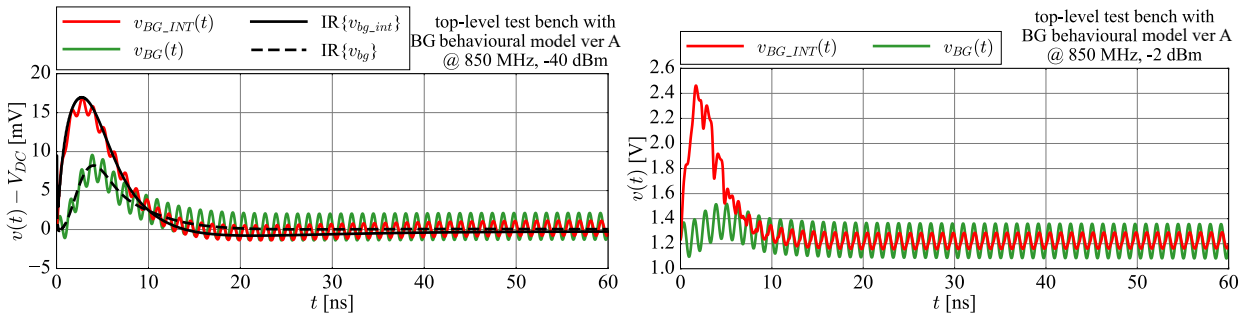


Figure 3.21: Frequency response associated with the closed-form solution of the voltage perturbation v_{bg_int} versus the RF generator v_g in the top-level test bench with the BG behavioural model instance ver-B.

In addition to the influence on the small-signal stability, the artificially large amplitude gain observed in the untrained RF frequency range may also generate artificial voltage overshoots during the initial transient of the TRAN simulation. The influence of the model frequency response in the untrained frequency range on initial transients is analysed next.

3.4.5 Initial transient stability



(a) (b)

Figure 3.22: (a) The initial transients of the voltages $v_{BG\_INT}(t)$ and $v_{BG}(t)$ in the TRAN simulation of the top-level test bench with the BG behavioural model instance ver-A at P_{RF} = -40 dBm compared to the impulse responses (IR) of the voltage perturbations v_{bg_int} and v_{bg}, (b) the initial large-signal transients at P_{RF} = -2 dBm [38].

Fig.3.22apresents the TRAN simulation of the top-level test bench in Fig.3.6, where the transistor-level BG circuit is replaced by the BG behavioural model instance ver-A presented in Section3.4.4, under an RF interference injection at 850 MHz with a low RF forward power level of -40 dBm.

The initial transients of the BG output voltage $v_{BG\_INT}(t)$ and the BUF output voltage $v_{BG}(t)$ are shown, starting from the stable DC operating point Q defined in the DC simulation that precedes the TRAN simulation. A large overshoot of the $v_{BG\_INT}(t)$ voltage transient is observed, with the peak of 17 mV at $t \approx 3$ ns, which is 8.7 times higher than the steady-state amplitude of 1.95 mV.

It is observed that the shape of both v_{BG_INT} and v_{BG} transients is consistent with the impulse responses (IR) that are calculated as the inverse fast Fourier transforms (IFFT) of the frequency responses associated with the perturbation voltage v_{bg_int} in Fig.3.20, and with the perturbation voltage v_{bg}. The same RF voltages in the TRAN simulation of the transistor-level REF circuit tend towards the steady-state with a lower mean value due to the RF-induced DC-shift, and their envelopes have an exponentially decaying shape without voltage overshoots.

Qualitatively similar voltage transients are observed under a higher RF forward power level of -2 dBm, as shown in Fig.3.22b. The peak of the BG output voltage $v_{BG\_INT}(t)$ transient increases to 2.46 V, which is 19 times higher than the steady-state amplitude of 129.3 mV, indicating that the level of the transient overshoot increases with the RF forward power level P_{RF}.

The voltage v_{BG_INT} also exhibits strong RF harmonic distortion during the overshoot period that is attributed to the nonlinearities of the transistor-level subcircuits triggered by the voltage overshoot. The initial transients of the large-signal voltages

in the TRAN simulation are linked to the impulse response that is defined by the full bandwidth of the small-signal frequency response of the associated voltage perturbations. The initial transients v_{BG_INT} and v_{BG} shown in Fig.3.22are therefore defined by the frequency responses $BG_{mod\_ij}(\jmath\omega)$ of the BG behavioural model outside of the trained RF frequency range.

The overshooting impulse response of v_{BG_INT} is associated with the artificially high low-frequency gain of 30.2 dB in the transfer function $BG_{mod\_21}(s)$ of the BG model ver-A shown in Fig.3.19, and it is linked to the large coefficients, up to 175, observed in the output weight matrix of the BG behavioural model instance, as follows. Since the BG output signals i_{DD_BG} and v_{BG_INT} are modelled using both BG input signals v_{BG_P1} and i_{BG_P2} simultaneously according to Eq. (3.7), the individual transfer functions $BG_{mod\_ij}(\jmath\omega)$ of each modelled signal against each individual input signal may not correspond to the physical transfer functions $BG_{ij}(\jmath\omega)$ of the transistor-level BG circuit, even at the trained RF frequency. According to [13], [34], this may result in "over-trained" ESN sub-model instances that are characterized by large output layer coefficients that attempt to "over-fit" the modelled output signals to the two available input signals, generating the large gain values in the behavioural model small-signal transfer functions.

Since it is not guaranteed that the behavioural model will recover to the correct steady-state after the untrained nonlinear dynamics of the transistor-level circuits are triggered by the transient overshoots, this large-signal aspect of the behavioural model stability is referred to as the initial transient stability.

The transient stability is improved by adjusting the ESN hyper-parameters to obtain output layer coefficients with values between -10 and 10. Fig.3.23presents the initial transient of the BG model ver-B, associated with the frequency response presented in Fig.3.21, with a lower gain of 1.9 dB, and output coefficients between -7.8 and 9.2.

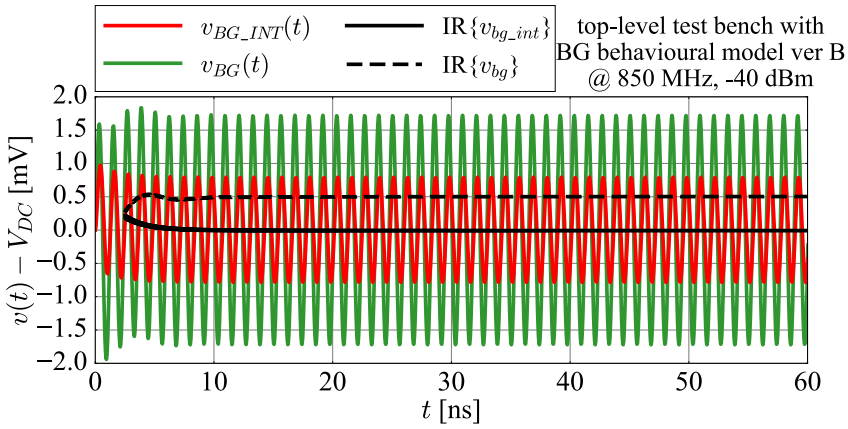


Figure 3.23: The initial transients of the voltages $v_{BG\_INT}(t)$ and $v_{BG}(t)$ in the TRAN simulation of the top-level test bench with the BG behavioural model instance ver-B at P_{RF} = -40 dBm compared to the impulse responses (IR) of the voltage perturbations v_{bg_int} and v_{bg}.

3.5 Behavioural modelling results

3.5.1 Test case 1: Behavioural model of the bandgap circuit

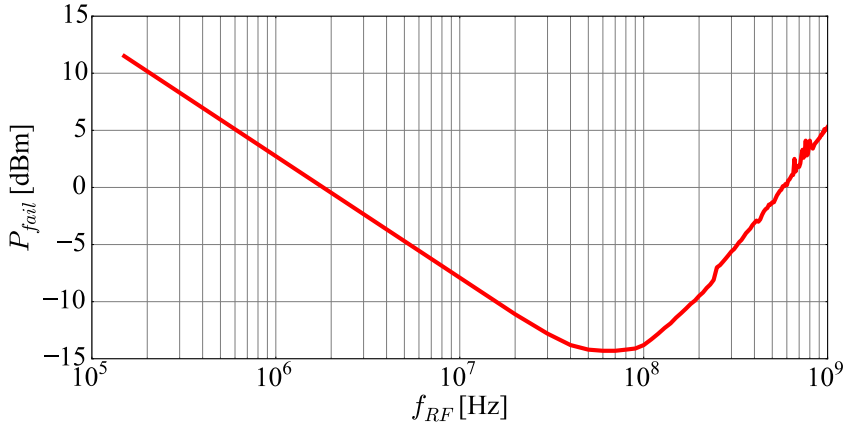


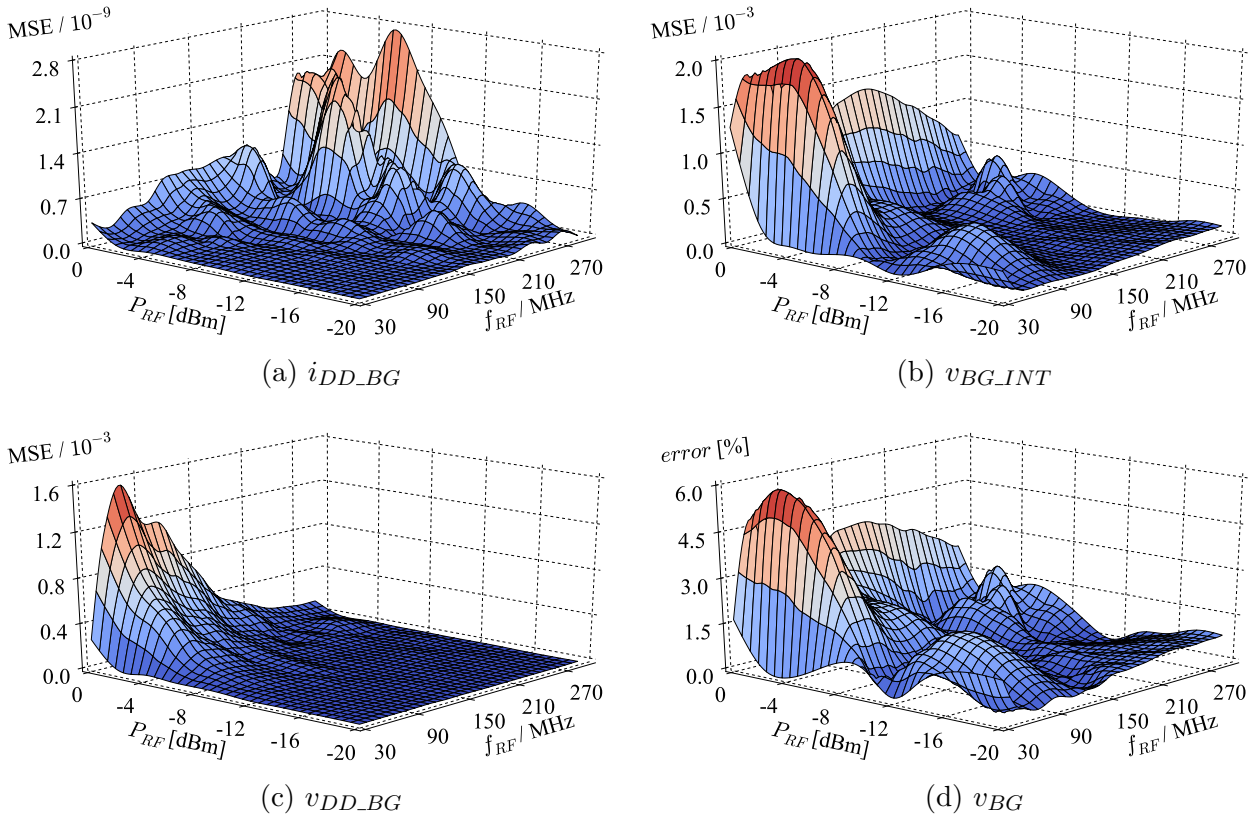
Figure 3.24: The DPI characteristic of the transistor-level REF circuit obtained by PSS simulations. The circuit fails if the RF-induced DC-shift of the output voltage v_{BG} exceeds ±10% of its nominal value of 1.234 V. The RF frequency step is 10 MHz, and the RF forward power resolution is 0.1 dB [36].

A behavioural model for the BG subcircuit in the REF circuit shown in Fig.3.6is built for DPI simulations of the REF circuit.

Fig.3.24presents the DPI characteristic of the transistor-level REF circuit obtained by PSS simulations in the Cadence® Spectre® circuit simulator, using the DPI algorithm presented in Section3.3.4. The failure criterion is defined as a pass if the mean value of the steady-state waveform of the output voltage v_{BG} is within ±10% of the nominal value V_{BG} of 1.234 V. The frequency is swept between 150 kHz and 1 GHz using 10 MHz steps, and the RF forward power resolution is 0.1 dB. The RF forward power level $P_{fail}\,(f)$ represents the lowest RF forward power level P_{RF} at which the circuit fails the failure criterion. The obtained DPI characteristic indicates the highest conducted susceptibility in the middle frequency range that improves with increasing RF frequency as the parasitic capacitances towards ground shunt the RF power away from the REF circuit.

In order to build wideband behavioural models, the frequency range is often divided into multiple frequency bands, such as in [22], with separate models for each frequency band. In this test case, the RF frequency range between 30 MHz and 300 MHz, and the forward power range between -20 dBm and 0 dBm is chosen. These operating conditions present the most critical area for the DPI simulations of the DUT according to Fig.3.24.

Referring to Fig.3.6, the training dataset consists of the time-domain signals $v_{DD\_BG}\,(t)$, $i_{DD\_BG}\,(t)$, $v_{BG\_INT}\,(t)$ in the steady-state. The waveforms are obtained using the PSS simulations of the transistor-level circuit that are extended to 50 periods and interpolated to a uniform sampling time T_s of 200 ps.



(a) i_{DD_BG} (b) v_{BG_INT}

(c) v_{DD_BG} (d) v_{BG}

Figure 3.25: The MSE accuracy of the BG behavioural model in the (f_{RF}, P_{RF}) design space [36].

The BG behavioural model is built using the basic "uni-directional" model architecture presented in Fig.3.1, where the VCCS and the VCVS are implemented using ESN models. The derivative of the model input voltage $v_{DD\_BG}(t)$ in Fig.3.6is used as an additional model input, as in [22]. The VCCS that models the nonlinear input impedance seen looking into port P_1 of the BG circuit is implemented using an ESN with 20 neurons.

The input and output signals are rescaled to the interval $[-1, 1]$ and a bias-term of value 0.1 is used. The neuron leaking rate is 0.03, and a white noise term with $1{\cdot}10^{-3}$ variance is used. Ridge regression with the regularisation coefficient $\beta = 1{\cdot}10^{-8}$ is used to perform linear regression.

The VCVS that models the nonlinear transfer function from port P_1 to port P_2 of the BG circuit is implemented using an ESN with 35 neurons. The input and output signals are rescaled to the interval $[-1, 1]$. A bias-term of value 0.1 is added used. The neuron leaking rate is 0.03, and a white noise term with a $1{\cdot}10^{-3}$ variance is used in training. Ridge regression with the regularisation coefficient $\beta = 1{\cdot}10^{-5}$ is used. The activation function is the hyperbolic tangent: $f(x) = \tanh(4x)$.

The ESN model parameters are chosen in a short trial-and-error process. The training dataset consists of approximately $2 \cdot 10^6$ data points, and the required training time is in the order of 40 seconds using a machine with an Intel® Core™ i5-4460 CPU @ 3.2 GHz

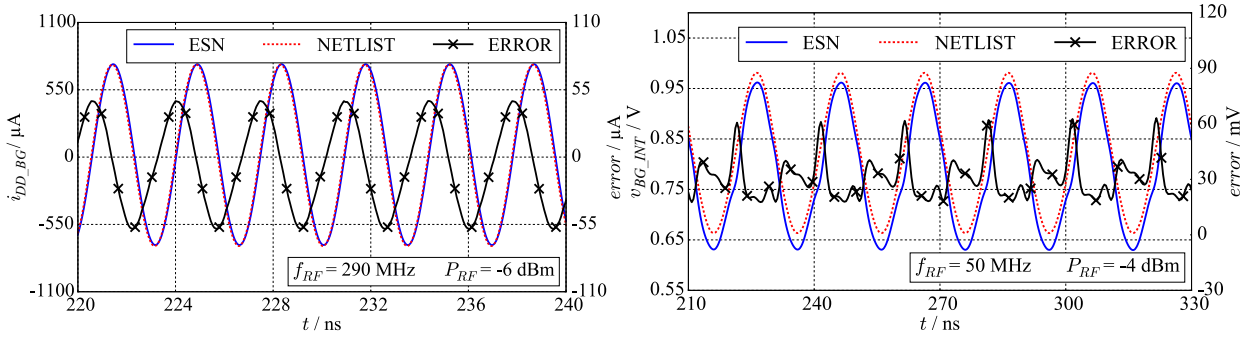


Figure 3.26: The reference and modelled time-domain waveforms of the modelled BG subcircuit and the instantaneous model error, taken at the worst-case MSE points: (a) input current model, (b) output voltage model [36].

and 8 GB of RAM.

The trained ESN models correctly capture the DC behaviour of the transistor-level BG circuit without using the model architecture with separate DC and RF sub-models, as the time-domain waveforms in the training dataset that correspond to the low RF forward power condition of -20 dBm across the wideband RF frequency range capture the DC behaviour of the modelled circuit.

The BG circuit in the top-level test bench in Fig.3.6is replaced by its behavioural model, and the resulting circuit is simulated in the time-domain using TRAN solver of the same circuit simulator used to build the training dataset. The TRAN simulation is run starting from the DC operating point, and the steady-state is reached after approximately 10 periods.

Fig.3.25presents the accuracy of the BG behavioural model in the top-level test bench over the design space defined by the RF frequency f_{RF} and RF forward power P_{RF} of the RF disturbance, evaluated for the top-level RF voltages and RF currents related to the BG subcircuit using the mean square error (MSE), as it is defined in Chapter2. The MSE of the modelled input current $i_{DD\_BG}(t)$ is shown in Fig.3.25a, and varies between $3.79{\cdot}10^{-13}$ and $2.73{\cdot}10^{-9}$. The MSE of the modelled output voltage $v_{BG\_INT}(t)$ is shown in Fig.3.25b, and varies between $1.75 \cdot 10^{-6}$ and $1.98{\cdot}10^{-3}$.

Fig.3.26presents the comparison between the modelled and desired signals in the time-domain for the (f_{RF}, P_{RF}) points with the worst-case MSE performance. The BG supply voltage $v_{DD\_BG}(t)$ is defined by the interaction between the transistor-level BSW circuit and the BG behavioural model. Its MSE is shown in Fig.3.25c, and varies between $9.83{\cdot}10^{-8}$ and $1.53{\cdot}10^{-3}$. The relative error of the mean value of the output voltage v_{BG} of the full circuit is shown in Fig.3.25d, and it varies between 0.017% and 5.64%.

The top-level test bench with the BG behavioural model is simulated to find the DPI characteristic with the same failure criterion. Fig.3.27presents the comparison between the DPI characteristic of the REF circuit compared to the transistor-level circuit shown in Fig.3.24, in the modelled RF frequency range. The modelled DPI characteristic is within 1.1 dB of the actual DPI characteristic in the entire frequency range of the model (30 MHz to 300 MHz).

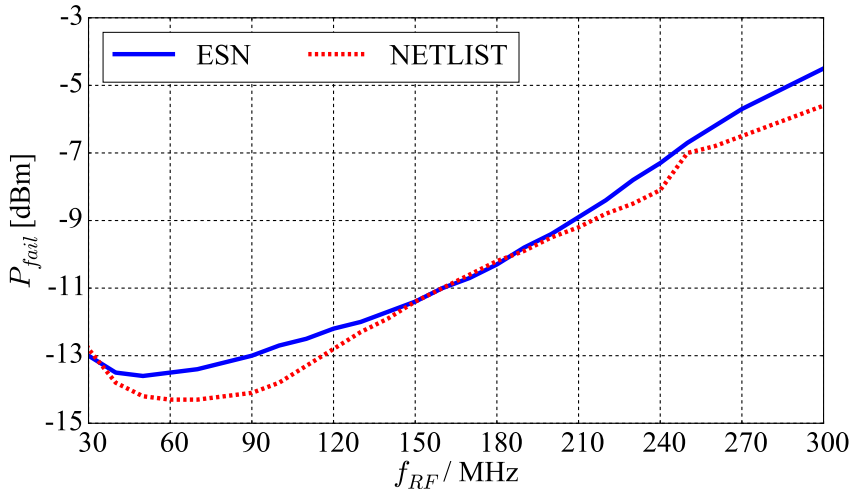


Figure 3.27: The comparison between the DPI characteristics of the DUT obtained using the time-domain simulations of the behavioural model (dotted line) and the transistor-level model (solid line) of the BG circuit [36].

The simulation speed-up results are presented in Table3.1. The speed-up achieved for the BG circuit by itself is determined by directly driving the BG circuit using the ideal signal $v_{IN,BG}(t)$ from file. The simulation times for the case with the behavioural model and for the case with the transistor-level model are denoted as T_{mod_BG} and T_{ref_BG}, and the simulation times of the complete REF circuit shown in Fig.3.6are denoted as T_{ref_DUT} for the transistor-level model, and T_{mod_DUT} for the test bench with the BG behavioural model. The simulation speed-up observed for the BG circuit has a limited influence on the simulation speed-up of the overall REF circuit, as the BG circuit does not contribute significantly to the complexity of the modelled circuit, compared to the BSW and BUF circuits. The simulation speed-up comparison of all subcircuits is given in Section3.5.3.

Table 3.1: The simulation times required for simulating 100 periods. Columns $T_{ref,BG}$ and $T_{ref,DUT}$ are the simulation times obtained using the transistor-level models of the BG circuit and of the entire DUT, respectively. Columns $T_{mod,BG}$ and $T_{mod,DUT}$ are the corresponding simulation times obtained using the behavioural model of the BG circuit [36].

f_{RF} [MHz]	P_{RF} [dBm]	T_{ref_BG} [s]	T_{mod_BG} [s]	T_{ref_DUT} [s]	T_{mod_DUT} [s]
	-20	6.0	1.9	12.7	11.5
30	-10	17.0	2.5	20.1	14.5
	0	37.5	3.1	27.7	24.7
	-20	7.1	2.2	16.3	11.8
100	-10	13.8	2.8	22.6	15.0
	0	28.3	2.8	27.2	23.3
	-20	6.0	2.9	14.2	11.8
300	-10	9.5	2.1	19.3	13.9
	0	16.0	4.5	27.0	24.2

3.5.2 Test case 2: Models of buffered voltage reference subcircuits

Interchangeable behavioural models of the BSW, BG, and BUF subcircuits are built that capture the narrow-band RF behaviour of the top-level REF circuit at 850 MHz in the RF forward power range from -40 dBm to -2 dBm. The model captures the soft harmonic distortion and the pronounced RF-induced DC-shift observed, as presented in Section3.3.2. The behavioural models are built using the extended model architecture with separate DC and RF sub-models, presented in Section3.2.2. The ESN training dataset is constructed using a subset of the steady-state time-domain RF voltages and RF currents obtained using PSS simulations of the top-level test bench in Fig.3.6.

The REF circuit is modelled using a total of seven ESN models in the three behavioural models that are trained using the ESN training procedure outlined in Chapter2. Each output signal i_{DD_BSW}, v_{DD_BG}, i_{DD_BG}, v_{BG_INT}, i_{BG_INT}, i_{DD_BUF}, v_{BG} is modelled using an ESN model with up to 10 leaky integrator neurons, as a function of the ESN input signals indicated by the inward-oriented solid arrows in Fig.3.7.

The time-domain waveforms are interpolated to a constant sampling time $T_s = 10$ ps that corresponds to the Nyquist frequency of 50 GHz, ensuring at least 50 time-domain samples per RF signal period at the highest DPI test frequency of 1 GHz. In order to achieve approximately equal weighting between the training signals for each ESN input and output signal in the ESN training dataset, the single steady-state period of the interpolated discrete-time waveform is extended to between 20 and 100 periods in the time-domain, where the number of periods is inversely proportional to the modelled signal amplitude.

The best performing behavioural model instances for each of the BSW, BG, and BUF subcircuits are evaluated using the methodology presented in Section3.3.3. Three top-level test benches are defined where one of the transistor-level subcircuits in Fig.3.6 is replaced by its behavioural model, and a total of nine RF voltages and RF currents are observed as a function of RF forward power level P_{RF} in each test bench.

The case with the test benches where two or three behavioural models are used is presented in Section3.5.3.

The verification dataset for evaluating the behavioural model accuracy includes RF forward power levels that are not contained in the training dataset, in order to evaluate the interpolation properties of the behavioural models at the trained narrow-band RF frequency. Table3.2summarizes the amplitude error bound $|\Delta|$ relative to the fundamental tone amplitude $|A_0|$, the absolute phase error $\angle\Delta$, and the error bound of the RF-induced DC-shift $\overline{\Delta}$ relative to the DC operating point value. These figures of merit are evaluated for each of the nine observed RF voltages and RF currents in the three test benches with the behavioural model replacing one subcircuit.

Table 3.2: Error bounds of the BSW, BG, BUF behavioural models in the top-level test bench with one behavioural model at 850 MHz from -40 dBm to -2 dBm in the TRAN simulation starting from the PSS initial condition [38].

	TOP transistor-level			TOP + BSW model			TOP + BG model			TOP + BUF model		
signal	$\lvert A_0\rvert$	DC OP	HD_n	$\left\lvert\frac{\Delta}{A_0}\right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$	$\left\lvert\frac{\Delta}{A_0}\right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$	$\left\lvert\frac{\Delta}{A_0}\right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$
v_{DD}	317.3 mV	3.30 V	-52 dBc	0.8%	0.0°	0.03%	0.05%	0.0°	0.02%	0.9%	0.0°	0.06%
i_{DD}	4.7 mA	577 µA	-49 dBc	1.8%	2.0°	0.08%	0.1%	1.2°	1.4%	0.5%	1.1°	0.9%
i_{DD_BSW}	3.2 mA	17.8 µA	-38 dBc	1.8%	4.5°	5.0%	0.9%	0.1°	50%	0.9%	0.0°	4.0%
v_{DD_BG}	88.4 mV	3.299 V	-47 dBc	1.8%	4.5°	0.02%	0.1%	2.7°	0.05%	0.9%	0.1°	0.03%
i_{DD_BG}	1.8 mA	7.32 µA	-38 dBc	1.7%	3.5°	4.0%	1.1%	1.2°	120%	0.9%	0.0°	10.0%
v_{BG_INT}	61.8 mV	1.234 V	-36 dBc	0.9%	0.5°	0.05%	0.4%	0.5°	0.03%	2.0%	6.5°	0.06%
i_{BG_INT}	85.7 µA	0.0 A	-35 dBc	2.0%	0.1°	N/A	0.2%	0.0°	N/A	4.0%	0.0°	N/A
i_{DD_BUF}	2.4 mA	559 µA	-37 dBc	1.8%	0.1°	0.08%	0.2%	0.0°	0.02%	0.5%	2.5°	1.0%
v_{BG}	135.4 mV	1.234 V	-54 dBc	0.9%	0.1°	0.05%	0.2%	0.2°	0.1%	1.0%	3.0°	0.1%

The DC operating point stability of the top-level test bench is verified using the methodology described in Section3.4.1. The small-signal and transient stability of the models in the top-level test bench are verified using the methodology described in Sections3.4.4and3.4.5. All behavioural model instances presented in this section have stable and unique DC operating points, and stable LHP poles associated with each small-signal perturbation signal in the top-level test bench.

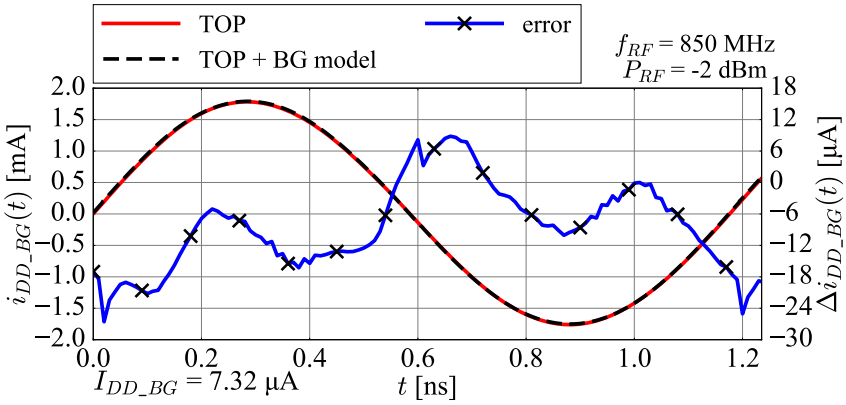


Figure 3.28: Comparison of time-domain waveforms of the BG supply current $i_{DD\_BG}(t)$ at P_{RF} = -2 dBm in the top-level test bench with the BG behavioural model, where the highest relative mean value error of 120% is observed. The amplitude of 1.8 mA is 245 times higher than the reference DC value I_{DD_BG} of 7.32 µA, and small errors of the time-domain samples near the peak result in a large relative error of the mean value [38].

The reference values $|A_0|$ and DC to calculate the relative values in percentage are given under the TOP transistor-level column. The amplitude accuracy of 1% corresponds to a signal-to-noise ratio (SNR) of 40 dB. The highest relative amplitude error $|\Delta/A_0|$ is observed for i_{BG_INT}, for which the reference amplitude $|A_0|$ is about 30 times lower compared to the remaining RF current signals in the test bench.

The worst-case error of the mean-value shift $\overline{\Delta}$ in Table3.2is observed for the RF current i_{DD_BG} in the top-level test bench with the BG behavioural model. Fig.3.28shows the corresponding time-domain waveforms and the instantaneous error in the time-domain. Since the fundamental tone amplitude of i_{DD_BG} is approximately 245 times larger than its mean value, the small instantaneous model errors in the time-domain samples around the waveform peak generate small relative percentage errors of the fundamental tone amplitude compared to the reference amplitude $|A_0|$ of 1.8 mA, and large relative percentage errors of the signal mean value when compared to the DC reference value of 7.32 µA. Similar observations are made for the remaining RF currents in the test bench.

The RF-induced DC-shift of the RF voltages v_{BG_INT} and v_{BG} is the most pronounced nonlinear effect in the modelled test bench, and it modelled within 0.1%, which corresponds to an equivalent signal-to-noise ratio (SNR) of 60 dB.

3.5.3 Test case 3: Connecting multiple behavioural models

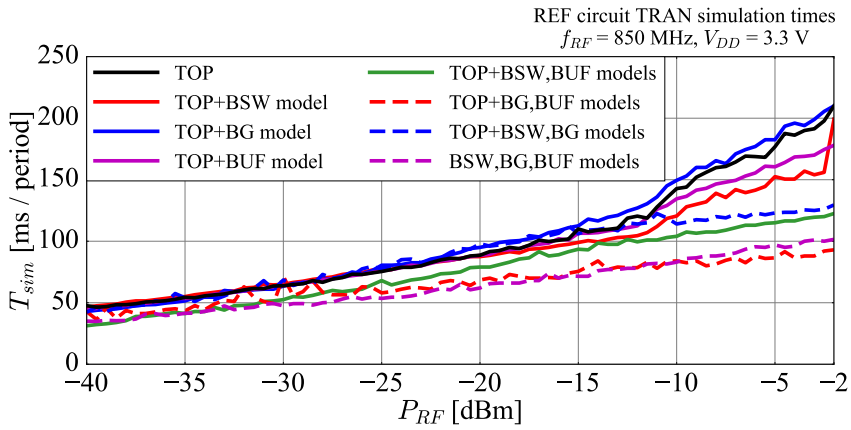


Figure 3.29: The comparison of TRAN simulation times per period for the seven top-level test benches of the REF circuit.

The three behavioural models presented in Section3.2are able to correctly load the connected transistor-level subcircuits. The model architecture in Fig.3.2also enables connecting two behavioural models that use the opposite dual nonlinear impedance models. The node shared between port P_2 of the BSW subcircuit and port P_1 of the BG subcircuit is associated with the RF voltage v_{DD_BG} and the RF current i_{DD_BG}. According to the flow-diagram in Fig.3.7, the selected nonlinear impedance model of BSW port P_2 is a controlled voltage source, and a controlled current source is used for BG port P_1.

The parallel combination of a voltage source and current source that control each other, that is driven by the pin voltage at port P_1 of the BSW circuit, defines both the RF voltage v_{DD_BG} and the RF current i_{DD_BG}. Using the same model architecture for both BSW port P_2 and BG port P_1 is not permitted, as a parallel combination of unequal voltage sources, or a series combination of unequal current sources is not defined.

Three additional model test benches are defined using the same behavioural model instances presented in Section3.5.2that model the three subcircuits in the REF circuit in Fig.3.6, where two subcircuits are replaced by their behavioural models, and the third one is a transistor-level circuit. In the final test bench, all three subcircuits are replaced by the behavioural models. Table3.3summarizes the model accuracy in these four test benches containing two or three behavioural models.

The simulation times of the seven conducted immunity test benches with one, two, or three behavioural models of the subcircuits in the REF circuit are compared in Fig.3.29. The maximum simulation speed-up factor of 2 is observed for the test case where the BG and the BUF subcircuits are replaced by the behavioural models. Note that the modelled transistor-level subcircuits in this test case do not include layout parasitic elements.

Table 3.3: Error bounds of the BSW, BG, BUF behavioural models in the top-level test bench with two or three behavioural model at 850 MHz from -40 dBm to -2 dBm in the TRAN simulation starting from the DC operating point Q.

	TOP transistor-level			BUF circuit + BSW,BG models			BG circuit + BSW,BUF models			BSW circuit + BG,BUF models			BSW,BG,BUF models		
signal	$\lvert A_0 \rvert$	DC OP	HD$_n$	$\left\lvert \frac{\Delta}{A_0} \right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$	$\left\lvert \frac{\Delta}{A_0} \right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$	$\left\lvert \frac{\Delta}{A_0} \right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$	$\left\lvert \frac{\Delta}{A_0} \right\rvert$	$\angle\Delta$	$\left[\frac{\overline{\Delta}}{\mathrm{DC}}\right]$
v_{DD}	317.3 mV	3.30 V	-52 dBc	1.0%	0.0°	0.01%	0.5%	0.0°	0.05%	1.6%	0.0°	2.2°	0.9%	0.0°	0.2%
i_{DD}	4.7 mA	577 µA	-49 dBc	3.2%	4.4°	0.8%	1.0%	3.2°	2.0%	0.5%	2.1°	65%	1.8%	5.6°	14%
i_{DD_BSW}	3.2 mA	17.8 µA	-38 dBc	2.8%	11.8°	28%	2.5%	4.1°	11%	2.5%	0.9°	120%	2.9%	9.6°	160%
v_{DD_BG}	88.4 mV	3.299 V	-47 dBc	2.0%	6.8°	0.02%	2.1%	4.5°	0.02%	4.1%	4.5°	3.3%	1.9%	6.1°	0.07%
i_{DD_BG}	1.8 mA	7.32 µA	-38 dBc	2.0%	9.6°	33%	2.0%	3.2°	20%	1.7%	5.0°	150%	2.2%	6.5°	177%
v_{BG_INT}	61.8 mV	1.234 V	-36 dBc	1.8%	9.3°	0.01%	3.1%	12.0°	1.7%	6.5%	10.5°	1.6%	1.8%	8.4°	0.04%
i_{BG_INT}	85.7 µA	0.0 A	-35 dBc	2.0%	0.4°	N/A	5.0%	2.7°	N/A	14.0%	12.6°	N/A	2.0%	0.5°	N/A
i_{DD_BUF}	2.4 mA	559 µA	-37 dBc	1.3%	0.1°	0.1%	1.8%	2.5°	2.3%	1.8%	5.0°	3.5%	1.3%	3.2°	10%
v_{BG}	135.4 mV	1.234 V	-54 dBc	0.9%	0.1°	0.03%	1.5%	3.3°	2.2%	4.0%	6.0°	3.7%	2.2%	1.9°	1.1%

3.6 Discussion

The merits and limitations of the proposed behavioural modelling methodology are discussed in terms of the application, model building complexity, accuracy, stability, and scalability of the presented behavioural models. The dual nonlinear impedance model architecture enables building interchangeable behavioural models of integrated circuits using echo state networks and controlled sources that define feedback loops between the time-domain voltages and currents associated with the modelled pins. The models are built with the goal of achieving simulation speed-up with reasonable model accuracy. Since the behavioural models contain no information about the physical structure of the modelled circuits, the models may also be used as an alternative to the encrypted transistor-level models for protecting the intellectual property of the modelled circuit.

The presented modelling approach is applied to an industrial test case, demonstrating that the behavioural models can properly load the connected transistor-level circuits and other behavioural models under a range of RF frequencies and RF forward power levels in the conducted immunity simulation environment. The models are able to interpolate between the trained RF frequency and RF forward power levels, making them indistinguishable from transistor-level circuit models in the TRAN simulations of the top-level test bench within the trained RF design space. This is suitable for RF simulation requirements from industrial practice, where the EMC simulations of the circuit under development are run at a particular worst-case RF frequency defined by the target system for the device for root cause analysis, or within a subset of the bandwidth defined by the DPI standard.

The nonlinear element in the behavioural model architecture can also be implemented using other artificial neural networks, such as the feedforward neural network with multiple hidden layers, or the nonlinear autoregressive neural network. The main benefit of using the echo state network is the fast and computationally efficient training procedure based on linear regression that enables fast iterative model re-building in order to achieve good model accuracy and stability. Separating the DC and RF sub-models further simplifies the model building process, as the ESN model does not need to be trained in a wide range of DC conditions of the modelled circuit.

Evaluating the accuracy of a given behavioural model in the circuit simulator is a multi-dimensional problem, as the model is built to cover a wide range of RF conditions, and multiple RF voltage and RF current waveforms in the time-domain are compared to the reference test bench. The accuracy of the presented wideband (the frequency span covering one decade) behavioural model of the BG subcircuit is evaluated using the mean square error measure over a wide RF design space, and it is comparable to the results of similar test cases in literature [11].

The test domain of the narrow-band behavioural models of the three subcircuits in the REF circuit includes a wide range of RF amplitudes across the nine RF voltages and RF currents in the top-level test bench. The proposed approach for defining the amplitude and phase error bounds enables: (i) a concise overview of the behavioural model accuracy over the design space, (ii) detecting which time-domain signal property exhibits the worst model performance, and at which RF forward power levels each error component starts increasing, (iii) iterative building of model instances to achieve the required accuracy for a particular RF simulation application requirement, by identifying the RF frequencies and RF forward power levels at which the model accuracy is lower, and (iv) identifying artificially added harmonic components that indicate "overtrained" models that fit the training data with poor interpolation properties.

The simulation speed-up enabled by the behavioural models is attributed to two main causes. The block-level results in Table3.1indicate that the simulation time of transistor-level BG circuit increases with increasing RF forward power level, as the transistors are driven into the nonlinear operating region, while the simulation time of the BG behavioural model is almost independent of the RF forward power level. The second consideration is the long simulation time required for the transistor-level circuits to reach the steady-state in the transient analysis due to the internal time constants of the circuit. As the behavioural models are derived directly from the steady-state signals, the steady-state is reached within approximately 10 periods, making the behavioural models very practical for use in the transient analysis.

The simulation times of the REF circuit with one or more behavioural models against the RF forward power level in Fig.3.29demonstrate that the transistor-level circuits enter the nonlinear region for RF forward power levels above -12 dBm, while the test benches with two or three behavioural models have a constant slope of simulation time for all RF forward power levels.

Behavioural models of similar complexity would be able to capture the behaviour of the REF circuit with included layout parasitics, enabling larger simulation speed-up factors.

The stability of the ESN models in the RF sub-model is achieved by guaranteeing the echo state property using the procedures outlined in Chapter2. The stability of the behavioural model in the top-level test bench, including the DC operating point stability (meta-stability), the small-signal stability, and the initial transient stability, depends on the DC and RF characteristics of the behavioural model outside of the trained DC and RF operating conditions, that are uniquely defined by the randomly generated coefficients in the input and hidden layers, and the trained output layer coefficients. As a result, the ESN models that are iteratively rebuilt using the same training dataset generate RF sub-models of similar RF accuracy with widely different DC and RF characteristics

outside of the trained range.

Since the echo state network is defined with a fixed sampling time, extending the training dataset to RF frequencies that are several decades below the target RF frequency range increases the number of time-domain samples per period in the training dataset, resulting in a scaling issue that would increase the computational complexity of the ESN training procedure.

This scaling issue leads to the conclusion that any increase in the behavioural model bandwidth and complexity should be motivated by the final use-case of the behavioural models. The RF sub-model is iteratively rebuilt until the untrained characteristics result in a stable model. This approach is enabled by the fast training procedure of the echo state network, compared to other artificial neural networks.

The theoretical conclusions presented in Section3.4enable linking the discrete-time properties of the echo state network to its behaviour in the circuit simulator. The framework based on the zero-order-hold element and the piecewise-constant continuous-time waveforms is useful for developing the stability analysis methodology. In the practical implementation of the echo state network in Verilog A presented in Chapter2and AppendixA, the ESN is defined using the delay operator, allowing the ESN output to change in between two discrete-time samples. This opens the possibilities for additional effects that influence the model stability in the circuit simulator, that are not detected in the presented test cases.

The presented behavioural models use up to two input signals for each ESN model. This is appropriate for an unloaded REF circuit, where the internal subcircuits load each other. The modelling of a loaded REF circuit would be enabled by adding the dependence of the internal RF signals on the RF load current that senses the nonlinear load impedance as a third input to the ESN in the output buffer behavioural model. While the presented nonlinear impedance model architecture is scalable to multiple inputs, it is recognized that the case with three or more input signals increases the complexity of the training dataset, and of the behavioural model stability analysis through a larger number of frequency responses and transfer functions that have to be considered.

In the presented test case, the functional signals are constant DC signals in the time-domain, and all time-varying signals in the top-level test bench are resulting from the RF interference injection into the supply pin of the circuit under test. This class of circuits is appropriate for the feasibility study into the interchangeable behavioural modelling of integrated circuits for conducted immunity simulations. The behavioural modelling of circuits that have time-varying functional signals in addition to the RF disturbance signals in the conducted immunity test bench, such as analog-to-digital converters (ADC), require further research into the scaling of the proposed methodology.

3.7 Summary

The nonlinear impedance model architecture based on controlled sources is introduced, and the implementation with echo state networks is presented that enables building behavioural models of integrated circuits which can replace transistor-level models, thus the name interchangeable models. The methodology for analysing the signal flow of a generic circuit is proposed, where the voltages and currents associated with each port of the modelled circuit are split into ESN input and output signals. The properties of the commercial circuit simulator solvers are evaluated for conducted immunity simulations, with focus on reaching the RF steady-state using the transient solver.

The behavioural model architecture is extended to enable modelling the DC and RF behaviour of the modelled circuit independently, in order to simplify the training requirements of the ESN model. The DC monitor block is introduced that enables separation of the DC and RF components of the monitored voltage signals in the time-domain, including the implementation in the hardware description language Verilog A that enables using the behavioural model in the DC simulations and in the transient simulations that start from an initial condition defined by a state file.

The conducted immunity simulation environment is introduced on the case of an industrial buffered voltage reference integrated circuit that contains three subcircuits. The relationships between the RF voltages and RF currents observed in the top-level simulation test bench are described by the flow-diagrams of each modelled subcircuit.

Two main nonlinear effects are observed: (i) RF harmonic distortion, and (ii) RF-induced DC-shift. The methodology for evaluating the behavioural model accuracy based on comparing the frequency domain properties of the time-domain waveforms is introduced. The methodology enables benchmarking the test bench where one or more subcircuits are replaced by the corresponding behavioural models as a function of the RF design space over multiple pin voltages and branch currents in a concise, tabulated form. An algorithm for running simulations according to the Direct RF Power Injection (DPI) standard, that minimises the number of required simulation runs using binary search, is introduced.

The stability of the behavioural models in the conducted immunity simulations of the top-level test bench is analysed in terms of the DC operating point stability, the small-signal stability, and the initial transient stability. The DC operating point stability, or “meta-stability”, is linked to the DC characteristics of the ESN model in the RF sub-model outside of the trained DC range, and a sufficient condition for the meta-stability of a given behavioural model is derived. The RF current balance requirement is introduced, and an effect based on implicit substrate connections that may introduce model stability issues is described.

A framework for analysing the interaction between the discrete-time echo state network and the continuous-time transistor-level circuits is developed, and the methodology for deriving the small-signal characteristics of the behavioural models is presented.

The closed-form solutions that define the small-signal frequency response of the buffered voltage reference circuit are derived using the block-level frequency responses of each subcircuit. The behavioural model stability in the top-level test bench is linked to the model properties outside of the trained RF frequency range. The initial transients of the behavioural models before reaching the steady-state are linked to the impulse response of each perturbation voltage in the top-level test bench, and to the properties of the trained coefficients in the ESN output weight matrix.

A behavioural model instance of the output buffer circuit is presented that is stable as a standalone element, but introduces unstable poles into the top-level test bench that contains other transistor-level circuits, resulting in a divergent transient simulation. The link between the model frequency responses and the unstable poles of the perturbation signals in the top-level test bench is derived.

A behavioural model instance of the bandgap circuit is presented that is stable both as a standalone element, and in the top-level test bench, but exhibits significant voltage overshoots that may trigger untrained behaviour of the transistor-level circuits in the test bench. The link between the voltage overshoot shape and the impulse response of the associated small-signal voltage perturbation and the properties of the underlying ESN model is presented.

A behavioural model of the bandgap circuit in the buffered voltage reference for DPI simulations is presented that covers the RF frequency range from 30 MHz to 300 MHz, and the RF forward power range from -20 dBm to 0 dBm. The model accuracy is evaluated using the mean square error, and it is comparable to the results reported in literature.

Compared to the transistor-level circuit, the simulation time of the behavioural model is independent of the RF forward power level. The DPI characteristic of the test bench where the bandgap circuit is replaced by its behavioural model is within 1 dB of the DPI characteristic of the transistor-level test bench. The interchangeable behavioural models of all three subcircuits at the narrow-band RF frequency of 850 MHz are built to cover the RF forward power range from -40 dBm to -2 dBm. The models are evaluated using the proposed model accuracy evaluation method. All three behavioural models are able to correctly load the connected transistor-level circuits. The behavioural model architecture enables connecting two behavioural models that use dual nonlinear impedance model topologies, and all three behavioural models are able to load the connected behavioural models in the top-level test bench. The simulation speed-up factors up to 2 are observed, with good model accuracy.

Chapter 4

Behavioural modelling in ESD and EMC applications

4.1 Motivation

The behavioural modelling principles are also applied to modelling applications in the areas of electrostatic discharge (ESD) and electromagnetic compatibility (EMC).

In the ESD area, the I-V characteristics of ESD protection devices are measured using the transmission line pulsing (TLP) method. The TLP method enables non-destructive I-V measurements up to very high values of voltage and current. The modelled ESD protection device exhibits the snapback effect, which is not included in most standard circuit library models. Behavioural models that contain the snapback effect enable simulating the TLP setup for root cause analysis. The model of the TLP setup combines the circuit model of the passive network with the behavioural model of the ESD device.

In the EMC area, the re-radiation of an RF disturbance picked up by a fully EMC-compliant IC in one RF band back into the system in another RF band may cause the de-sensing of other modules in the wireless system. The RF re-radiation effect is caused by the nonlinear IC pin impedance that generates RF harmonic distortion. Behavioural models enable simulations of RF re-radiation during the design phase of product development.

The chapter is organized as follows. Section4.2presents the behavioural model of an ESD protection device that exhibits snapback for use in the TLP simulations. The model is derived from the measured I-V characteristics, and it is correlated to the time-domain waveforms measured in the TLP setup. Section4.3presents the behavioural model of an I2C pad of an industrial IC for simulations of the RF re-radiation in a magnetically coupled wireless system due to RF harmonic distortion. The model is derived from circuit simulations, and it is correlated to RF harmonic distortion measurements. Section4.4 summarizes the chapter. The research from this chapter is presented in [44], [45].

4.2 Transmission line pulse modelling

Electrostatic discharge (ESD) events are an important consideration for all integrated circuits (IC). The voltages applied to an IC during an ESD event exceed the supply voltage by several orders of magnitude [56]. In order to protect the IC from ESD events, ESD protection devices such as silicon-controlled rectifiers (SCR) [57] are implemented in the IC design. The standard ESD tests include the human body model (HBM) test [58], the transmission line pulsing (TLP) test [59], and the machine model (MM) test [60].

An important parameter of the ESD protection devices is the I-V characteristic of the device-under-test (DUT) for high values of the voltage and current. In order to avoid the systematic thermal breakdown of the DUT caused by the high DC current values, the I-V characteristic is measured using the TLP measurement method, in which a series of pulses having the duration of 100 ns is applied to the DUT. The I-V pairs are extracted from the quasi-DC steady-state of the pulse. The pulses are generated by discharging a coaxial cable pre-charged to a DC voltage that defines the pulse energy.

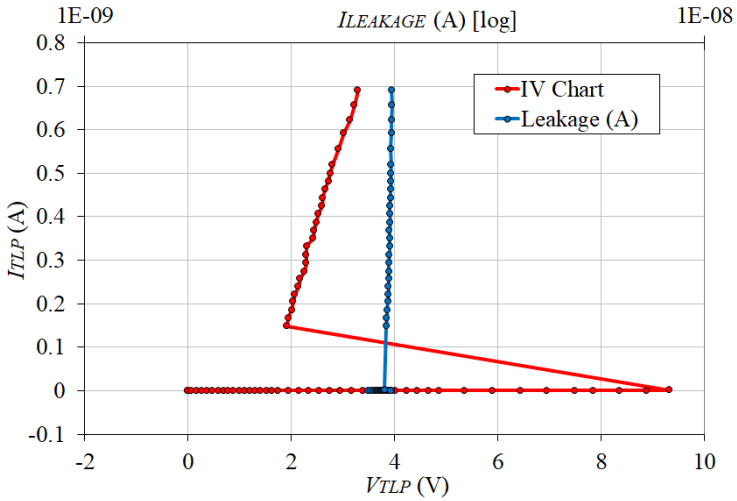


Figure 4.1: Measured TLP characteristic of a gate-coupled NMOS silicon-controlled rectifier ESD protection device [44].

Fig.4.1shows the I-V characteristic of a gate-coupled NMOS silicon-controlled rectifier (GCNSCR) obtained by TLP measurements. Each point in the I-V characteristic represents the settled voltage and current values in the quasi-DC steady-state of the pulse measured using a high-speed oscilloscope. The DC leakage current of the DUT is measured after each applied pulse and it is plotted in the upper x-axis to detect if the measurement was destructive or non-destructive.

The GCNSCR exhibits the snapback effect for values of V_{IN} above approximately 9 V, at which the device starts conducting current, and the voltage across the device decreases to approximately 2 V, generating a negative dynamic resistance. The snapback effect is described in more detail in [44].

4.2.1 TLP simulation environment

Table 4.1: The model parameters of the lumped-distributed TLP generator model [44].

parameter	value	parameter	value
K	2.3	R_{A3} [Ω]	20
R_G [MΩ]	10	t_{d2} [ns]	2
Z_0 [Ω]	50	C_1 [pF]	18
t_{d1} [ns]	50	R_1 [Ω]	0.9
R_{S1} [Ω]	2.5	L_1 [nH]	5
t_r [ns]	6	C_2 [pF]	10
R_{A1} [Ω]	20	L_2 [nH]	180
R_{A2} [Ω]	56		

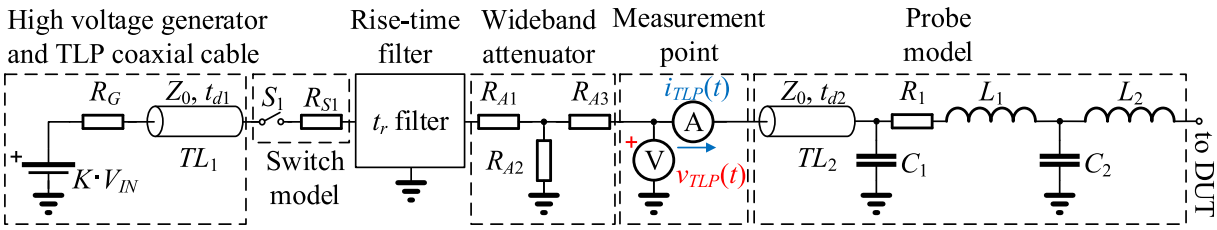


Figure 4.2: Mixed lumped-distributed model of the TLP generator [44].

The mixed lumped-distributed model of the TLP measurement system is presented in Fig.4.2with the model parameters summarized in Table4.1. The model topology is built and tuned using the measured TLP current and voltage waveforms of the open, short, and match loads (not shown here, available in [44]). The coaxial cable is modelled as a lossless transmission line defined by the characteristic impedance $Z_0 = 50\ \Omega$ and by the propagation delay $t_{d1} = 50$ ns. The DC voltage source $K \cdot V_{IN}$ charges the transmission line TL_1 while the switch S_1 is in the open position. The energy accumulated in TL_1 is discharged through the series resistance R_{S1} of the switch S_1 when the switch is closed, generating a rectangular pulse of $2t_{d1} = 100$ ns in duration.

The rising and falling edges of the resulting rectangular pulse are shaped by the 6 ns rise-time filter, which is modelled using the 9th order lumped model presented in [61]. The resistive T-network consisting of the resistances R_{A1}, R_{A2}, R_{A3} defines a wideband attenuator with the attenuation factor $K = 2.3$. The attenuator is optimized to minimize the waves reflected from unmatched loads in order to achieve approximately the correct voltage value in the open load case, and the correct current value in the short load case after the 100 ns pulse. It should be noted that the modelled voltage in the open load case and the modelled current in the short load case both tend towards zero after 400 ns.

The DC voltage of the power supply model is increased by the attenuation factor K in order to compensate for the attenuator. The TLP voltage and current waveforms $v_{TLP}(t)$ and $i_{TLP}(t)$ are measured using a high-speed oscilloscope at the output of the attenuator. The pulse is applied to the DUT using a probe modelled by the lossless 50 Ω transmission line TL_2 defined by the propagation delay $t_{d2} = 2$ ns, analogously to [59]. The probe tip is modelled by two CL networks consisting of C_1, L_1, C_2, L_2, and the series resistance $R_1 = 0.9$ Ω.

4.2.2 Test case: Behavioural model of a GCNSCR exhibiting snapback

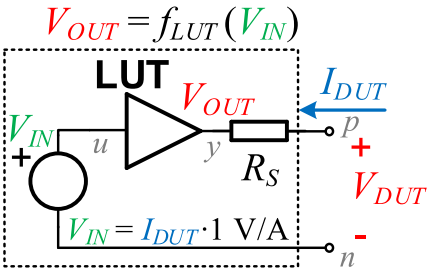


Figure 4.3: Architecture of the behavioural model of the ESD protection device TLP characteristic based on [62]. The look-up table (LUT) is built from the TLP measurement data [44].

The behavioural model of the GCNSCR device is built using the model architecture in Fig.4.3according to the methodology presented in [62] based on a current-controlled voltage source (CCVS). The current I_{DUT} flowing into the device is converted to an internal voltage V_{IN}, and it is applied to the look-up table (LUT) that generates the voltage V_{DUT} at the device pin p. The look-up table contains the (I_{DUT}, V_{DUT}) pairs obtained from the TLP measurement data. The model is implemented in Verilog A and it is simulated in Cadence® Spectre® with the TLP generator model in Fig.4.2.

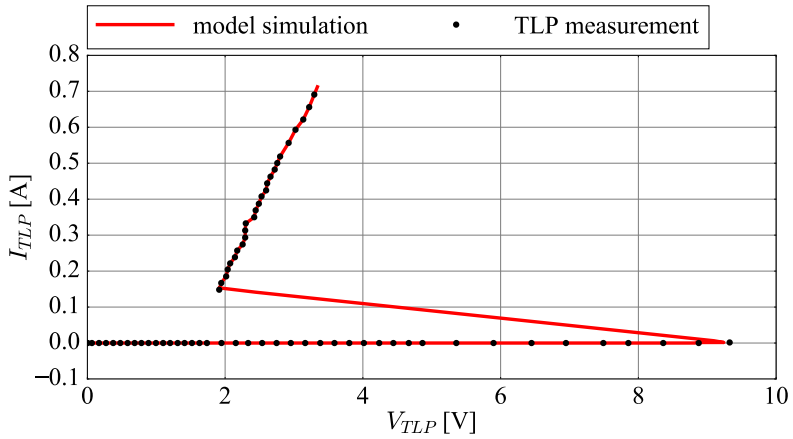


Figure 4.4: Comparison between the measured and modelled TLP characteristic of the GCNSCR device. The voltage V_{IN} is swept from 0.1 V to 40 V in 100 mV steps [44].

Fig.4.4presents the comparison between the simulated TLP characteristic of the behavioural model and the measured TLP data. Examples of simulated time-domain waveforms in the off-state and on-state are shown in Fig.4.5. The I-V characteristic in Fig.4.4is obtained by sampling the voltage and current waveforms at $t = 100$ ns.

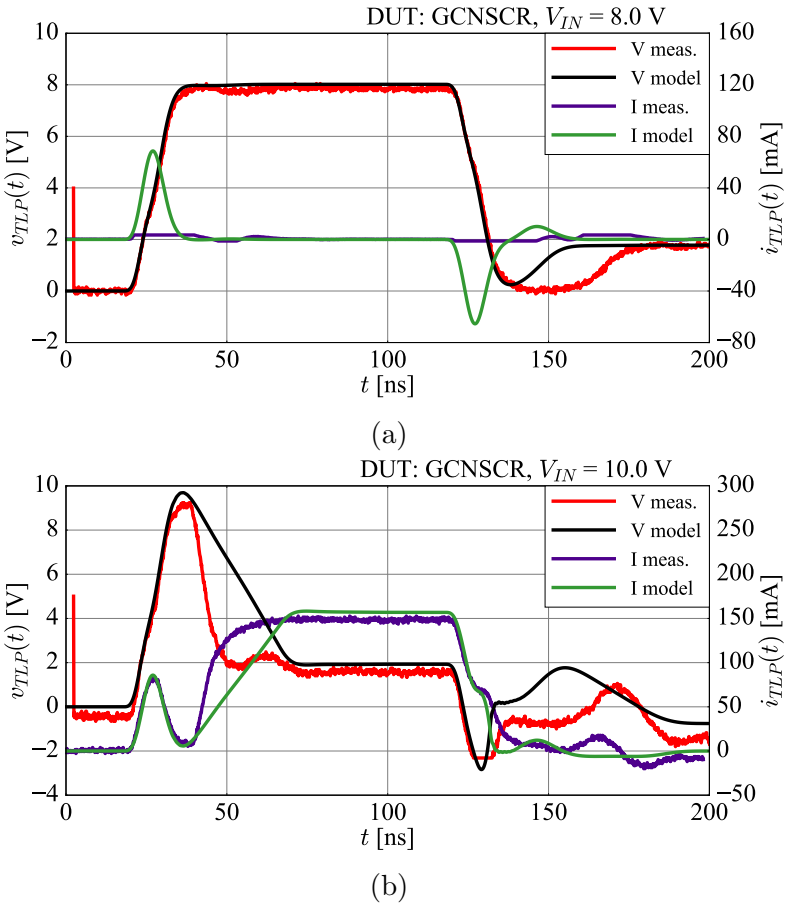


Figure 4.5: Comparison between the measured and modelled TLP voltage and current waveforms of the GCNSCR device in the time-domain: (a) in the off-state, (b) in the on-state [44].

The rising edge of the voltage overshoot waveform in the on-state observed in Fig.4.5b from 20 ns to 40 ns, and the corresponding current waveform, are correctly predicted by the model because these transients are defined by the reactive elements in the model of the probe tip in the TLP generator model in Fig.4.2.

The falling edge of the voltage overshoot from 40 ns to 70 ns represents the turn-on time of the GCNSCR. Since these transients are defined by the device parasitics that are not included in the simulation model, the circuit simulator tends towards the settled quasi-DC steady-state voltage and current values using the observed ramp waveforms.

The modelling approach based on a combination of a circuit model and LUT model demonstrates that the snapback effect can be reproduced in simulations. The I-V characteristic and the time-domain overshoots are modelled accurately, except during the turn-on period, which is defined by the ESD device parasitics not included in the model.

4.3 RF harmonic distortion modelling

Modern consumer electronics devices include an increasing number of antennas operating in a wide range of radio-frequency (RF) bands in close proximity to an increasing number of integrated circuits (IC) [63]. As a result, antenna structures and IC interconnects are mutually coupled by their reactive near fields. An emerging EMC topic in such environments is the RF interference between an aggressor operating in one band and a victim operating in another band, through a third element: an IC that picks up the RF disturbance at its input-output (IO) pins. Due to the nonlinear input impedance of the IO pins, the IC re-radiates the RF disturbance at the second or third harmonic frequency back into the system [63], [64].

In [63], a digital interface signal (HDMI) is the aggressor that generates harmonics interfering with a WiFi antenna in the 2.4 GHz and 5 GHz bands. In [64], the re-radiation of an electronic circuit illuminated by a radiated EM field is characterized using a proposed non-standard characterization setup. The EMC standards for radiated and conducted emissions of ICs do not cover the re-radiation effect because the re-radiated RF disturbance originates from the IC pins, but it is not generated in the IC [64].

Characterizing the nonlinearity of ICs by harmonic distortion measurements requires achieving sufficiently high dynamic range to detect the harmonics in the presence of a fundamental tone that is often larger by several orders of magnitude. This can be achieved using specialized instrumentation, such as the nonlinear vector network analyzer (NVNA) [65]. Alternative methods to separate the large fundamental tone from the harmonics are based on the diplexer, as presented in [66], [67]. The general mathematical framework for nonlinear device characterization and modelling are the X-parameters [65]. The X-parameter models capture the full nonlinear behaviour of the modelled devices [65], [68]. Alternatively, a simplified model based on the voltage-dependent capacitance can be used according to [69–71], which captures only the RF harmonic distortion behaviour of the IC.

In this section, the nonlinearity of an IC pin is characterized by measurements using the adapted methodology based on the diplexer [66], [67]. The measurements are correlated with the simulations that include the IC, the test board, and the diplexer model. The circuit simulations of the IC are used to build a behavioural model of the nonlinear IC pin impedance based on the voltage-dependent capacitance and dynamic resistance [69–71]. The model is used to improve the simulation time in a wireless system test case.

4.3.1 Voltage-dependent RC elements

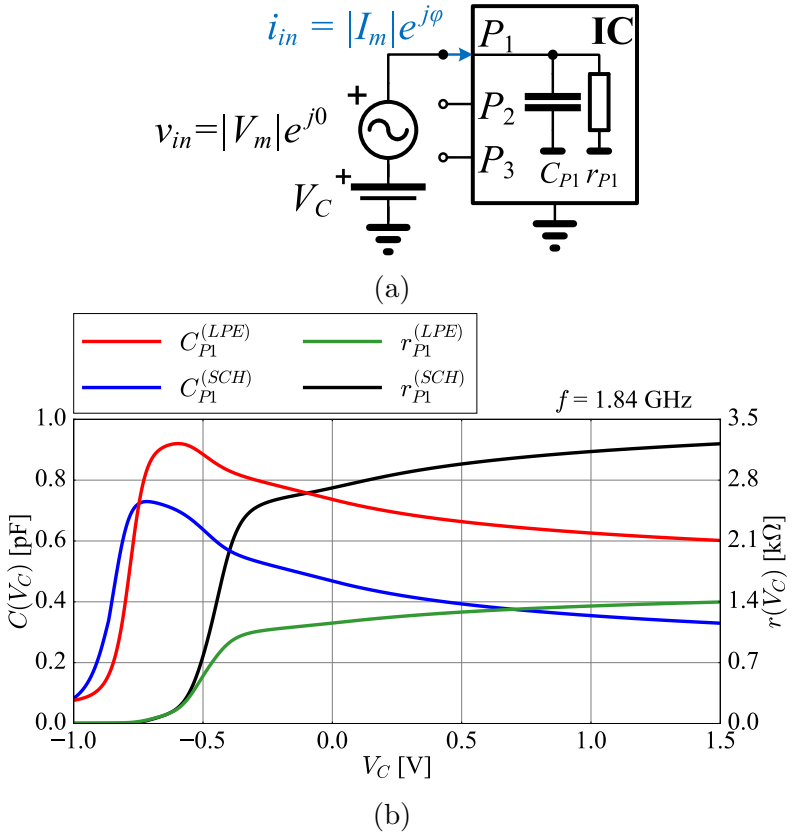


Figure 4.6: (a) Simulation testbench used for extracting the values of the capacitance C_{P1} and dynamic resistance r_{P1} as a function of the bias voltage V_C, according to [69], (b) voltage-dependent RC term values of the IC pin P_1, extracted from simulations of the schematic netlist (SCH), and the netlist including layout parasitic elements (LPE) [45].

The pads of all ICs contain various devices for protection against ESD, such as a silicon-controlled rectifier (SCR) [72]. These normally-off devices turn on during ESD events in order to provide a low-ohmic path from the pad to ground, and present a voltage-dependent capacitive load in parallel to the pad during the normal circuit operation conditions. Such devices cause nonlinear harmonic distortion due to their nonlinear I-V characteristics [64]. The interference of more than one fundamental tone, i.e. nonlinear intermodulation distortion, is not considered in the scope of this work.

The I-V characteristic of a voltage-dependent capacitor $C = C\left(V_C\right)$ is given by Eq. (4.1) according to [71], and it follows directly from the definition of the capacitance as the derivative of charge with respect to voltage [71].

$$C\left(V_C\right) \triangleq \frac{\mathrm{d}q\left(v\right)}{\mathrm{d}v}|_{v=V_C} \implies i\left(t\right) = C\left(v\left(t\right)\right) \cdot \frac{\mathrm{d}v\left(t\right)}{\mathrm{d}t} \tag{4.1}$$

To illustrate how the voltage-dependent capacitance causes harmonic distortion, the capacitance function $C(V_C)$ is expanded according to the Maclaurin series in Eq. (4.2):

$$C(V_C) = \sum_{k=0}^{N} C_k V_C^k \implies i(t) = \sum_{k=0}^{N} C_k \cdot \big(v(t)\big)^k \cdot \frac{\mathrm{d}v(t)}{\mathrm{d}t} \tag{4.2}$$

The repeated multiplication operation (exponentiation) of the voltage $v(t)$ generates higher order harmonics. In the special case of a voltage-independent capacitor $C = C_0$, no higher order harmonics are generated because the terms involving voltage multiplication are removed. The coefficients C_k in Eq. (4.2) mathematically define the harmonic distortion, however they do not have physical meaning. Knowing the capacitance value as a function of voltage using a look-up table (LUT) as the ideal interpolation method [71], is sufficient to model the harmonic distortion.

The simulation testbench for extracting the voltage-dependent capacitance value according to [69] is given in Fig.4.6. The IC pin-under-test is modelled according to [68] as a parallel combination of the voltage-controlled capacitor C_{P1} defined by Eq. (4.1), and the dynamic resistance r_{P1} defined by Eq. (4.3):

$$r(V_C) \triangleq \frac{\mathrm{d}v}{\mathrm{d}i}\Big|_{v=V_C} \implies i(t) = \int_0^t \frac{1}{r\big(v(t')\big)} \frac{\mathrm{d}v(t')}{\mathrm{d}t'} \mathrm{d}t' \tag{4.3}$$

Since both the capacitance C_{P1} and the resistance r_{P1} in Fig.4.6are time-derivatives of the IC pin voltage $v(t)$ taken in the bias point V_C, the DC current does not flow into the IC pin.

The phasor $i_{in} = |I_m| e^{\jmath\varphi}$ of the AC current flowing into the IC pin P_1 is simulated as a function of the DC voltage bias V_C and the AC voltage phasor $v_{in} = |V_m| e^{\jmath 0}$ at the fundamental radial frequency ω_0. The resulting current i_{in} is divided into the real part i_r flowing into the voltage-dependent dynamic resistance r_{P1}, and the imaginary part i_c flowing into the voltage-dependent capacitance C_{P1} according to Eq. (4.4).

$$\begin{aligned} i_{in} = i_r + i_c \implies i_r &\triangleq \mathrm{Re}\{i_{in}\} = \frac{1}{r_{P1}(V_C)} \cdot v_{in} \\ i_c &\triangleq \jmath\,\mathrm{Im}\{i_{in}\} = \jmath\omega_0 C_{P1}(V_C) \cdot v_{in} \end{aligned} \tag{4.4}$$

The extracted values of $r_{P1}(V_C)$ and $C_{P1}(V_C)$ are shown in Fig.4.6b, based on the simulation of the schematic netlist (SCH), and based on the netlist that includes the layout parasitic elements (LPE). The bias voltage V_C is swept from -1 V to +1.5 V, and the RF frequency is set to 1.84 GHz. The model Eqs. (4.1) and (4.3) are implemented in Verilog A using the time-derivative ddt, time integral idt, and look-up tables.

4.3.2 RF harmonic distortion simulation environment

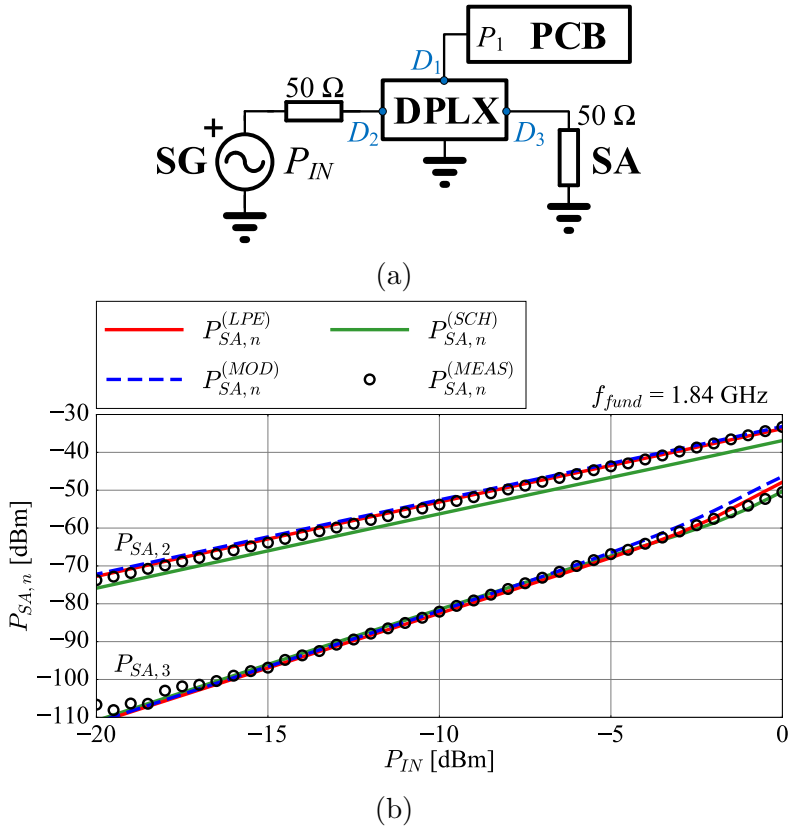


Figure 4.7: (a) Measurement setup for IC pin nonlinearity characterization based on the diplexer (DPLX) [66], [67], including the RF signal generator (SG), spectrum analyzer (SA), and test board (PCB), (b) comparison between measurement and behavioural model simulation of the power at second harmonic $P_{SA,2}$ and third harmonic $P_{SA,3}$ in the diplexer setup at 1.84 GHz [45].

The IC nonlinearity is characterized using the adapted approach presented in [66], [67] based on the diplexer. The diplexer is a 3-port component that separates the incident fundamental tone injected into the IC pin from the higher-order harmonics reflected to the spectrum analyzer, that can be several orders of magnitude lower than the fundamental tone [66]. The diplexer setup is shown in Fig.4.7a.

The IC is wire-bonded on the test board (PCB), and routed towards SMA connectors using 50 Ω transmission lines (TL) implemented on a high-frequency substrate.

The IC nonlinearity is characterized by sweeping the input power P_{IN} of the fundamental tone in Fig.4.7afrom -20 dBm to 0 dBm at 1.84 GHz, and plotting the power levels of the second and third harmonic measured using the spectrum analyzer (SA).

A detailed description of the diplexer measurement setup is given in [45].

The comparison between measurements and simulations is shown in Fig.4.7b. The measurement setup is recreated in the simulation environment as follows. The diplexer is modelled using the measured 3-port S-parameters as its behavioural model. The test board is modelled using the S-parameters obtained from the full-3D FEM simulation of the test board, including the bondwires. The nonlinear IC is included in the simulation in three variants: (i) using the transistor-level circuit schematic (SCH), (ii) using the transistor-level circuit including the layout parasitic elements (LPE), and (iii) using the Verilog A model built from the LPE-variant of the circuit. The steady-state waveforms of the node voltages are obtained using the periodic steady-state (PSS) solver.

The slopes of the second and third order harmonics are 2 dB/dB and 3 dB/dB, as expected according to the theoretical analysis given in [65]. The LPE-variant of the transistor-level circuit is in better agreement with measurements than the SCH-variant because the parasitic capacitance values are non-negligible compared to the voltage-dependent capacitances that generate the harmonics.

Table 4.2: Comparison of simulation times for different simulation variants of the diplexer setup [45].

variant	simulation time at -20 dBm [min]	simulation time at 0 dBm [min]
(i) transistor-level SCH	1	4
(ii) transistor-level LPE	20	80
(iii) Verilog A model	0.1	0.7

The simulation times are summarized in Table4.2. The simulation time increases for higher power levels because the transistor models in the circuit enter more nonlinear regime. The Verilog A model provides a simulation speed-up factor of 100 at the power level of 0 dBm compared to the LPE-variant of the circuit.

4.3.3 Test case: Re-radiation in a magnetically coupled wireless system

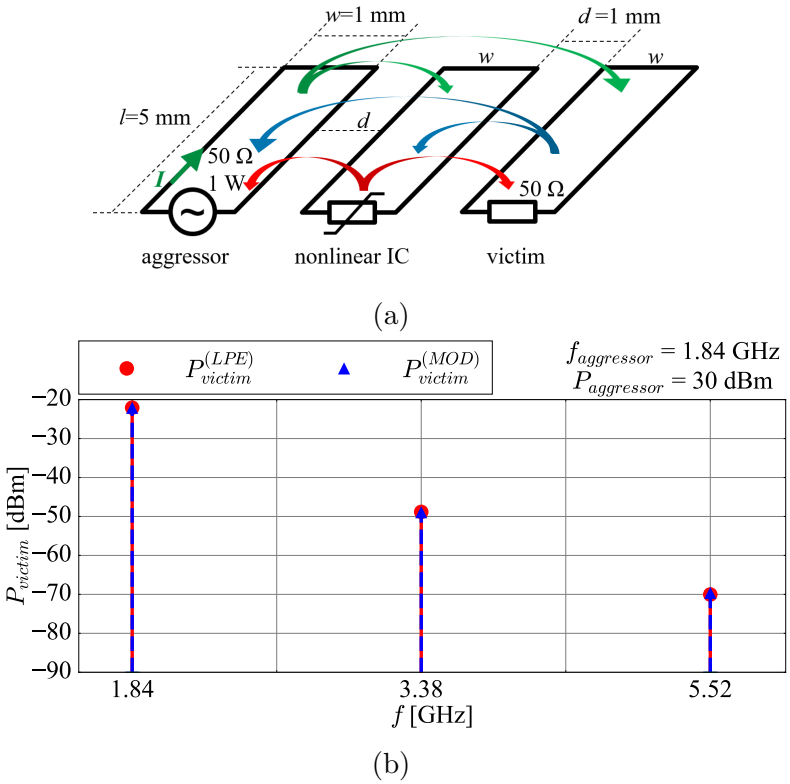


Figure 4.8: (a) Measurement setup for IC pin nonlinearity characterization based on the diplexer (DPLX) [66], [67], including the RF signal generator (SG), spectrum analyzer (SA), and test board (PCB), (b) PSS simulation of the wireless system test case where the aggressor operates at 1.84 GHz and the available power of 1 W = 30 dBm [45].

Magnetic near field coupling is the dominant coupling mechanism in many applications where bondwires or bended transmission lines of flexible PCBs have small wire cross-sections, and form relatively large mutually coupled current loops. The geometries of such structures are very complex, however the underlying principle of the studied EMC effect can be demonstrated on a simplified test case using three rectangular wire loops shown in Fig.4.8a. The length of each wire loop is l=5 mm and the width is w=1 mm. The wire cross-section is 25 µm by 25 µm. The distance between the rectangular loops is 1 mm edge-to-edge.

The left loop represents the aggressor, e.g. an active feedline of a GSM antenna, or parts of the antenna structure. The center loop represents a transmission line connected to an IC pin. The right loop represents the victim structure, e.g. a feedline or an antenna structure of a WiFi module terminated in 50 Ω. The aggressor operates in the LTE band 3 at 1.84 GHz at the maximum allowed forward power of 1 W = 30 dBm. Due to the nonlinear distortion of the IC pin, the third order harmonic is generated at 5.52 GHz, i.e. in the ISM band of standard WiFi applications.

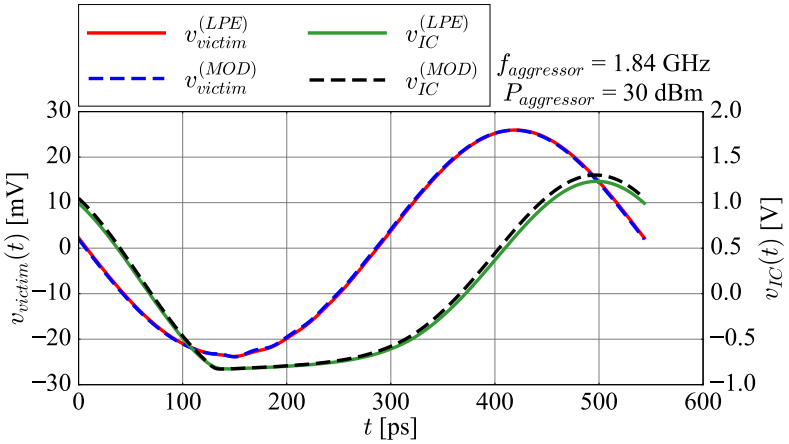


Figure 4.9: Time-domain output of the PSS simulation of the wireless system test case [45].

The 3D-FEM simulation of the presented wireless system is used to obtain 3-port S-parameters that define the mutual coupling between the aggressor, the nonlinear IC, and the victim. The simulation environment similar to the setup in Fig.4.7is used to simulate the large-signal behaviour of the wireless system, where the diplexer is replaced by the 3-port S-parameter model of the wireless system.

Fig.4.8bshows the PSS simulation results of the signals picked up by the victim loop. The minimum receiver sensitivity of a WiFi module must be better than -82 dBm for 6 MB/s data rate. To ensure headroom, datasheets of typical WiFi receivers indicate up to 10 dB better sensitivity specification of -92 dBm. The presented simulation results show that the disturbance at 5.52 GHz picked up by the victim loop is -70 dBm, or 12 dB above the minimum sensitivity, and 22 dB above the typical sensitivity of a standard WiFi receiver.

The simulation is run using the LPE-variant of the transistor-level circuit, and using the Verilog A implementation of the model presented in Section4.3.1. In the time-domain, Fig.4.9shows that the behavioural model reproduces the large-signal behaviour of the LPE-variant. The simulation time is 20 min for the circuit LPE-variant, and 10 s for the Verilog A behavioural model variant.

The presented wireless test case demonstrates that place and route of standard mixed signal ICs and its interconnects is crucial for the overall performance of wireless communication systems.

By providing simple and accurate nonlinear models of the IO-terminals of integrated circuits to the RF system designer, the nonlinear distortion effects can be taken into consideration when laying out the system design and defining the EMC strategy of the product.

4.4 Summary

The transmission line pulsing measurement method is presented, and a mixed lumped-distributed model of the TLP generator is derived. The behavioural model of a gate-coupled NMOS silicon-controlled rectifier device is built using TLP measurement data. The modelled device exhibits the snapback effect that is not included in most model libraries. The model is implemented in Verilog A and enables running TLP simulations in the time-domain in the circuit simulator. The off-state and on-state of the modelled device are modelled correctly in the quasi-DC steady-state during the TLP pulse. The behavioural model enables fast and accurate modelling of the ESD device that exhibits the snapback effect into the TLP simulation environment.

The RF re-radiation due to RF harmonic distortion of nonlinear integrated circuits in wireless systems is presented. The root cause of the RF harmonic distortion is linked to the voltage-dependent RC elements in I2C pins. A method for extracting the voltage-dependent values using AC simulations is presented, and a behavioural model for RF harmonic distortion simulations is built using the extracted characteristics. The behavioural model is validated by comparison to measurements in the diplexer setup. Simulation speed-up factors up to 115 are achieved when using the behavioural model compared to the transistor-level circuit with the extracted layout parasitic elements.

The RF re-radiation effect is demonstrated on a magnetically coupled wireless system consisting of an aggressor antenna operating at 1.84 GHz, a victim antenna operating in the 5 GHz WiFi band, and a nonlinear integrated circuit. The aggressor RF disturbance signal is picked up by the IC and the third harmonic frequency is generated due to nonlinear distortion at the IC pad, and it is re-radiated to the victim. The behavioural model enables the inclusion of the nonlinear IC into the RF simulation environment.

Chapter 5

Conclusion

The thesis presents modelling of integrated circuit nonlinearities by echo state networks in combination with look-up tables and S-parameters. The models accurately represent input and output impedance nonlinearities and because of that they correctly load the circuits to which the model is connected. The models have been proven to be accurate for a wide range of power levels, i.e. they correctly reproduce DC-shifts and higher order harmonics. Depending on the model and application, the speed-ups of only 2 times up to 100 times have been obtained while maintaining a good accuracy.

The echo state network is introduced as the building block for modelling large-signal behaviour of nonlinear integrated circuits. The formal mathematical definition of the echo state network is given with the procedure for guaranteeing bounded-input bounded-output (BIBO) stability. The procedures for the training and the verification of an echo state network with randomly generated recurrent connections in the hidden layer are presented for time-series modelling. The proposed method for modelling the nonlinear circuit behaviour defines the modifications to the generic ESN training procedure for time-series modelling required for modelling the time-domain waveforms obtained by simulations of integrated circuits. An iterative method for manually selecting the ESN hyper-parameters is given, with a set of guidelines that describe the influence of each ESN hyper-parameter on the properties of the iteratively generated ESN instances.

An adaptive algorithm for sampling the nonlinear circuit behaviour in the design space is presented that enables building the ESN training dataset with more samples placed in the design space regions with higher nonlinearity expressed as total harmonic distortion of the modelled waveforms, while avoiding the under-sampling of linear regions. Two stopping criteria for the adaptive sampling algorithm are presented, based on a fixed maximum number of samples, and on Spearman correlation between consecutive 2D interpolators of the user-selected scalar function above a defined design space.

The implementation of the echo state network in the hardware description language Verilog A is given. The Verilog A implementation enables the use of the ESN model in commercial circuit simulators. The proposed modelling methodology is applied to five industrial test cases: a voltage follower, a DC-DC driver IC, a LIN interface, an analytical oscillator with a feedback connection, and an RF mixer. The presented modelling results demonstrate the feasibility of using the echo state network to model a wide range of nonlinear behaviour observed in integrated circuit simulations, including the memory effects with delays between the input and output signals of up to 1000 samples, and the behaviour associated with circuits that have two widely separated time-constants.

The ESN model is benchmarked against the reference recurrent neural network model, and it is shown to enable obtaining comparable accuracy expressed as mean square error using a faster and simpler training procedure with guaranteed BIBO stability. The generalization properties of the ESN model are limited to interpolation within a trained design space, and to the ability to react to input signals with additive white noise. Simulation speed-up factors up to 77 are observed compared to the transistor-level circuits with included layout parasitic elements. The execution time of the ESN model is less dependent on the total harmonic distortion of the modelled time-domain waveforms observed in the integrated circuit.

The nonlinear impedance model architecture based on controlled sources is introduced, and the implementation with echo state networks is presented that enables building behavioural models of integrated circuits which can replace transistor-level models, thus the name interchangeable models. The methodology for analysing the signal flow of a generic circuit is proposed, where the voltages and currents associated with each port of the modelled circuit are split into ESN input and output signals. The properties of the commercial circuit simulator solvers are evaluated for conducted immunity simulations, with focus on reaching the RF steady-state using the transient solver.

The behavioural model architecture is extended to enable modelling the DC and RF behaviour of the modelled circuit independently, in order to simplify the training requirements of the ESN model. The DC monitor block is introduced that enables separation of the DC and RF components of the monitored voltage signals in the time-domain, including the implementation in the hardware description language Verilog A that enables using the behavioural model in the DC simulations and in the transient simulations that start from an initial condition defined by a state file.

The conducted immunity simulation environment is introduced on the case of an industrial buffered voltage reference integrated circuit that contains three subcircuits. The relationships between the RF voltages and RF currents observed in the top-level simulation test bench are described by the flow-diagrams of each modelled subcircuit.

Two main nonlinear effects are observed: (i) RF harmonic distortion, and (ii) RF-induced DC-shift. The methodology for evaluating the behavioural model accuracy based on comparing the frequency domain properties of the time-domain waveforms is introduced. The methodology enables benchmarking the test bench where one or more subcircuits are replaced by the corresponding behavioural models as a function of the RF design space over multiple pin voltages and branch currents in a concise, tabulated form. An algorithm for running simulations according to the Direct RF Power Injection (DPI) standard, that minimises the number of required simulation runs using binary search, is introduced.

The stability of the behavioural models in the conducted immunity simulations of the top-level test bench is analysed in terms of the DC operating point stability, the small-signal stability, and the initial transient stability. The DC operating point stability, or "meta-stability", is linked to the DC characteristics of the ESN model in the RF sub-model outside of the trained DC range, and a sufficient condition for the meta-stability of a given behavioural model is derived. The RF current balance requirement is introduced, and an effect based on implicit substrate connections that may introduce model stability issues is described.

A framework for analysing the interaction between the discrete-time echo state network and the continuous-time transistor-level circuits is developed, and the methodology for deriving the small-signal characteristics of the behavioural models is presented.

The closed-form solutions that define the small-signal frequency response of the buffered voltage reference circuit are derived using the block-level frequency responses of each subcircuit. The behavioural model stability in the top-level test bench is linked to the model properties outside of the trained RF frequency range. The initial transients of the behavioural models before reaching the steady-state are linked to the impulse response of each perturbation voltage in the top-level test bench, and to the properties of the trained coefficients in the ESN output weight matrix.

A behavioural model instance of the output buffer circuit is presented that is stable as a standalone element, but introduces unstable poles into the top-level test bench that contains other transistor-level circuits, resulting in a divergent transient simulation. The link between the model frequency responses and the unstable poles of the perturbation signals in the top-level test bench is derived.

A behavioural model instance of the bandgap circuit is presented that is stable both as a standalone element, and in the top-level test bench, but exhibits significant voltage overshoots that may trigger untrained behaviour of the transistor-level circuits in the test bench. The link between the voltage overshoot shape and the impulse response of the associated small-signal voltage perturbation and the properties of the underlying ESN model is presented.

A behavioural model of the bandgap circuit in the buffered voltage reference for DPI simulations is presented that covers the RF frequency range from 30 MHz to 300 MHz, and the RF forward power range from -20 dBm to 0 dBm. The model accuracy is evaluated using the mean square error measure, and it is comparable to the results reported in literature.

Compared to the transistor-level circuit, the simulation time of the behavioural model is independent of the RF forward power level. The DPI characteristic of the test bench where the bandgap circuit is replaced by its behavioural model is within 1 dB of the DPI characteristic of the transistor-level test bench. The interchangeable behavioural models of all three subcircuits at the narrow-band RF frequency of 850 MHz are built to cover the RF forward power range from -40 dBm to -2 dBm. The models are evaluated using the proposed model accuracy evaluation method. All three behavioural models are able to correctly load the connected transistor-level circuits. The behavioural model architecture enables connecting two behavioural models that use dual nonlinear impedance model topologies, and all three behavioural models are able to load the connected behavioural models in the top-level test bench. The simulation speed-up factors up to 2 are observed, with good model accuracy.

The guidelines for further research into the behavioural modelling are given, including the modelling of a loaded buffered voltage reference circuit that requires scaling the behavioural models to more than two input signals, and the modelling of integrated circuits that have time-varying functional signals in addition to the signals generated by the injected RF interference.

The transmission line pulsing measurement method is presented, and a lumped-distributed model of the TLP generator is derived. The behavioural model of a gate-coupled NMOS silicon-controlled rectifier device is built using TLP measurement data. The modelled device exhibits the snapback effect that is not included in most model libraries. The model is implemented in Verilog A and enables running TLP simulations in the time-domain in the circuit simulator. The off-state and on-state of the modelled device are modelled correctly in the quasi-DC steady-state during the TLP pulse. The behavioural model enables fast and accurate modelling of the ESD device that exhibits the snapback effect into the TLP simulation environment.

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List of abbreviations

ADC analog-to-digital converter

ANN artificial neural network

BIBO bounded-input bounded-output

CCVS current-controlled voltage source

CIF Cauchy integral formula

DPI direct power injection

DPLX diplexer

DUT device-under-test

EMC electromagnetic compatibility

EMI electromagnetic interference

ESD electrostatic discharge

ESN echo state network

ESP echo state property

FFNN feed-forward neural network

FFT fast Fourier transform

FRD frequency response data

GaN gallium nitride

GCD greatest common divisor

GCNSCR gate-coupled NMOS silicon-controlled rectifier

HBM human body model

HDL hardware description language

HDMI high-definition multimedia interface

I2C inter-integrated circuit

IBIS I/O buffer information specification

IC integrated circuit

IDTFT inverse discrete-time Fourier transform

IEC International Electrotechnical Commission

IF intermediate frequency

IFFT inverse fast Fourier transform

IO input-output

IR impulse response

LHP left half-plane

LIN local interconnect network

LNA low noise amplifier

LO local oscillator

LOLA local linear approximation

LUT look-up table

MLP multilayer perceptron

MM machine model

MOR model order reduction

MPC model predictive control

MSE mean square error

NARX nonlinear autoregressive neural network

NMOS n-channel metal-oxide-semiconductor transistor

NVNA nonlinear vector network analyzer

PCB printed circuit board

PMOS p-channel metal-oxide-semiconductor transistor

PSS periodic steady-state

PWL piecewise linear

QP quadratic programming

RF radio-frequency

RHP right half-plane

RMSE root mean square error

RNN recurrent neural network

SA spectrum analyzer

SAPF shunt active power filter

SCR silicon-controlled rectifier

SDN simplified dual neural network

SG signal generator

SLFN single-layer feedforward neural network

SNR signal-to-noise ratio

SQL structured query language

SVM support vector machine

THD total harmonic distortion

TL transmission line

TLP transmission line pulsing

TRAN transient

VCCS voltage-controlled current source

VCVS voltage-controlled voltage source

ZOH zero-order hold

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Appendix A

Behavioural model architecture in the hardware description language Verilog A

This chapter presents the implementation of the behavioural model architecture presented in Chapter3in the hardware description language Verilog A. The hierarchical approach is used, where the top-level code for the behavioural model instantiates the DC and RF sub-models, and the ESN rescaling blocks, that are implemented as separate modules. The presented code is compatible with the Verilog A and Verilog AMS standards, and it is tested in the Cadence® Spectre® circuit simulator.

The chapter is organized as follows. SectionA.1presents the schematic and the Verilog A code of the interchangeable behavioural model of a generic 2-port circuit block BLK, consisting of the DC and RF sub-models, and the corresponding rescaling blocks. The two pins of the modelled block use both dual nonlinear impedance models presented in Chapter3, based on the voltage-controlled voltage source and on the current-controlled voltage source. SectionA.2presents the implementation of the look-up table sub-model in Verilog A, and the implementation of the echo state network sub-model and the rescaling block are given in SectionsA.3andA.4.

A.1 Interchangeable behavioural model in Verilog A

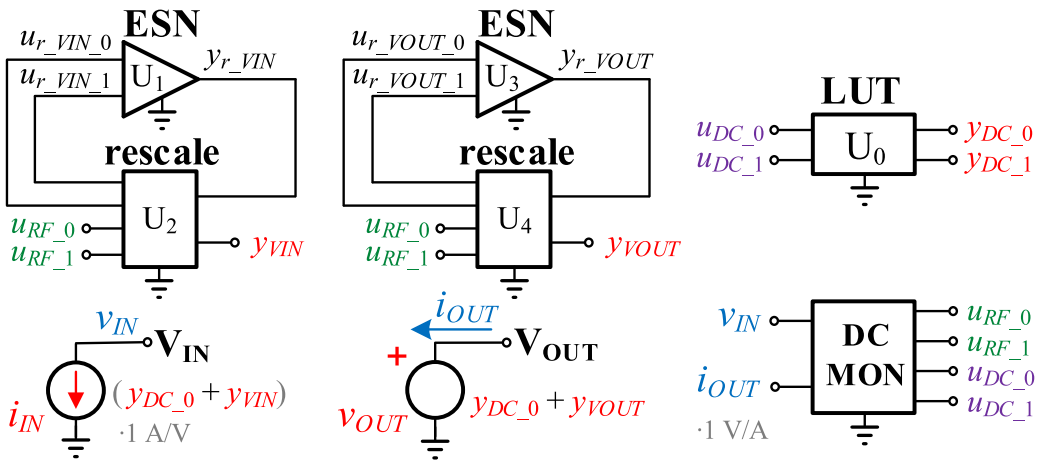


Figure A.1: The behavioural model of a generic 2-port circuit block. The input current i_{IN} and output voltage v_{OUT} are modelled as functions of the input voltage v_{IN} and output current i_{OUT}.

Fig.A.1shows interchangeable behavioural model schematic of a generic 2-port circuit BLK in the circuit simulator, according to the model architecture presented in Chapter3. The model implementation in the hardware description language Verilog A is given in ListingA.1. The presented code implements the DC monitor block, and instantiates the LUT and ESN sub-models, and the ESN rescaling blocks. The implementations of the instantiated blocks are given in SectionsA.2,A.3,A.4.

Listing A.1: Verilog A implementation of the interchangeable behavioural model of a generic 2-port circuit block BLK.

```
module BLK(VIN, VOUT, gnd);
inout VIN, VOUT, gnd;
electrical VIN, VOUT, gnd;
real VIN_mon_dc_val, VOUT_mon_dc_val, initCond;

electrical [0:1] u_DC, y_DC, u_RF, ur_VIN, ur_VOUT; // 2-element vectors
electrical y_VIN, yr_VIN, y_VOUT, yr_VOUT;          // scalars
electrical VIN_IC, VOUT_IC;                    // initial condition nodes

// instantiate DC and RF sub-models
BLK_lut U0 (u_DC,y_DC,gnd);              // DC sub-model for VIN and VOUT
BLK_VIN_esn U1 (ur_VIN,yr_VIN,gnd);      // RF sub-model for VIN
BLK_VIN_rescale U2 (u_RF,ur_VIN,y_VIN,yr_VIN,gnd);      // VIN rescale
BLK_VOUT_esn U3 (ur_VOUT,yr_VOUT,gnd); // RF sub-model for VOUT
BLK_VOUT_rescale U4 (u_RF,ur_VOUT,y_VOUT,yr_VOUT,gnd);  // VOUT rescale

// analog block below
```

```
analog begin
 // DC monitor begin
 @ (initial_step) begin
  if (analysis("dc")||((V(VIN_IC,gnd)==0)&&(V(VOUT_IC,gnd)==0))) begin
   VIN_mon_dc_val = V(VIN,gnd);
   VOUT_mon_dc_val = -I(VOUT,gnd);
   initCond = 0;
  end
  else begin
   VIN_mon_dc_val = V(VIN_IC,gnd);
   VOUT_mon_dc_val = V(VOUT_IC,gnd);
   initCond = 1;
  end
 end
 if (analysis("dc")) begin
  V(u_DC[0],gnd) = V(VIN,gnd);
  V(u_DC[1],gnd) = -I(VOUT,gnd);
  V(VIN_IC,gnd) <+ 0.0;
  V(VOUT_IC,gnd) <+ 0.0;
 end
 else begin
  V(u_DC[0],gnd) <+ VIN_mon_dc_val;
  V(u_DC[1],gnd) <+ VOUT_mon_dc_val;
  if (($abstime==0.0) && (initCond==0)) begin
   V(VIN_IC,gnd) <+ 0.0;
   V(VOUT_IC,gnd) <+ 0.0;
  end
  else if ($abstime > 0.0) begin
   V(VIN_IC,gnd) <+ V(u_DC[0],gnd);
   V(VOUT_IC,gnd) <+ V(u_DC[1],gnd);
  end
 end
 V(u_RF[0],gnd) <+ V(VIN,gnd) - V(u_DC[0],gnd);
 V(u_RF[1],gnd) <+ -I(VOUT,gnd) - V(u_DC[1],gnd);
 // DC monitor end

 I(VIN,gnd) <+ V(y_DC[0],gnd);
 I(VIN,gnd) <+ V(y_VIN,gnd);
 V(VOUT,gnd) <+ V(y_DC[1],gnd);
 V(VIN,gnd) <+ V(y_VOUT,gnd);
end
endmodule
```

A.2 Look-up table sub-model in Verilog A

The Verilog A implementation of the look-up table sub-model is given in ListingA.2.

Listing A.2: Verilog A implementation of the look-up table sub-model.

```
module BLK_lut(u1, u2, y1, y2, gnd);
inout u1, u2, y1, y2, gnd;       // u1=VIN_dc, u2=IOUT_dc
electrical u1, u2, y1, y2, gnd; // y1=IIN_dc, y2=VOUT_dc

localparam real f_u1[0:5306] = '{ // DC table input data VIN
 };
localparam real f_u2[0:5306] = '{ // DC table input data IOUT
 };
localparam real f_y1[0:5306] = '{ // DC table output data IIN
 };
localparam real f_y2[0:5306] = '{ // DC table output data VOUT
 };
analog begin
 V(y1,gnd)<+ $table_model(V(u1,gnd),V(u2,gnd),f_u1,f_u2,f_y1,"1CC,1CC");
 V(y2,gnd)<+ $table_model(V(u1,gnd),V(u2,gnd),f_u1,f_u2,f_y2,"1CC,1CC");
end
endmodule
```

The two-dimensional look-up tables with 87-by-61 input DC variables that contain the DC characteristics for each of the two output DC variables are sorted, such that the second input changes through all values for each value of the first input, and flattened to four one-dimensional vectors with 5307 elements for each input and output DC variable.

A.3 Echo state network sub-model in Verilog A

The Verilog A implementation of the echo state network sub-model is given in ListingA.3.

Listing A.3: Verilog A implementation of the echo state network sub-model.

```
module BLK_VIN_esn(u1, u2, y1, gnd);
inout u1, u2, y1, gnd;          // u1=VIN_rf, u2=IOUT_rf
electrical u1, u2, y1, gnd;     // y1=IIN_rf

localparam real Win[0:18] = '{  // Win coeffs - 2 input units+bias
 };
localparam real W[0:35] = '{    // W coeffs - 6 internal units
 };
localparam real Wout[0:8] = '{  // Wout coeffs - 1 output unit
 };
localparam real a = 0.1;        // leaking rate
localparam real Ts = 1e-11;     // sampling time
electrical u0;                  // bias-term
electrical [1:6] x, x_tilde;    // internal unit activations
electrical [1:1] y_tilde;       // output unit activation
genvar i, j;                    // for-loop variables
analog begin
 V(u0, gnd) <+ 0.1;
 for(i = 0; i < 6; i = i + 1) begin
  V(x_tilda[i + 1],gnd) <+ Win[i * 3 + 0] * V(u0,gnd);
  V(x_tilde[i + 1],gnd) <+ Win[i * 3 + 1] * V(u1,gnd);
  V(x_tilde[i + 1],gnd) <+ Win[i * 3 + 2] * V(u2,gnd);
  for (j = 0; j < 6; j = j + 1) begin
   V(x_tilde[i + 1],gnd) <+ W[i * 6 + j] * absdelay(V(x[j + 1],gnd),Ts);
  end
  V(x[i + 1],gnd) <+ a * tanh(V(x_tilde[i + 1],gnd));
  V(x[i + 1],gnd) <+ (1 - a) * absdelay(V(x[i + 1],gnd),Ts);
 end
 for (i = 0; i < 1; i = i + 1) begin
  V(y_tilde[i + 1],gnd) <+ Wout[i * 9 + 0] * V(u1,gnd);
  V(y_tilde[i + 1],gnd) <+ Wout[i * 9 + 1] * V(u1,gnd);
  V(y_tilde[i + 1],gnd) <+ Wout[i * 9 + 2] * V(u2,gnd);
  for (j = 0; j < 6; j = j + 1) begin
   V(y_tilde[i + 1],gnd) <+ Wout[i * 9 + j + 3] * V(x[j + 1],gnd);
  end
 end
 V(y1,gnd) <+ V(y_tilde[1],gnd);
end
endmodule
```

A.4 Rescaling block in Verilog A

The Verilog A implementation of the rescaling block is given in ListingA.4.

Listing A.4: Verilog A implementation of the ESN rescaling block.

```
module BLK_VIN_rescale(u1, u2, ur1, ur2, y1, yr1, gnd);
inout u1, u2, ur1, ur2, y1, yr1, gnd;           // u1=VIN_rf, u2=IOUT_rf
electrical u1, u2, ur1, ur2, y1, yr1, gnd;      // y1=IIN_rf

localparam real u_min[1:2] = '{ // input minimum values
};
localparam real u_max[1:2] = '{ // input maximum values
};
localparam real ur_min[1:2] = '{ // rescaled input minimum values
};
localparam real ur_max[1:2] = '{ // rescaled input maximum values
};
localparam real y_min[1:1] = '{ // output minimum values
};
localparam real y_max[1:1] = '{ // output maximum values
};
localparam real yr_min[1:1] = '{ // rescaled output minimum values
};
localparam real yr_max[1:1] = '{ // rescaled output maximum values
};
analog begin
 V(ur1,gnd) <+ (V(u1,gnd) - u_min[1]) * (ur_max[1] - ur_min[1]) /
                                  (u_max[1] - u_min[1]) + ur_min[1];
 V(ur2,gnd) <+ (V(u2,gnd) - u_min[2]) * (ur_max[2] - ur_min[2]) /
                                  (u_max[2] - u_min[2]) + ur_min[2];
 V(y1,gnd) <+ (V(yr1,gnd) - yr_min[1]) * (y_max[1] - y_min[1]) /
                                  (yr_max[1] - yr_min[1]) + y_min[1];
end
endmodule
```

Appendix B

Buffered voltage reference small-signal modelling

This chapter presents the small-signal analysis of the transistor-level buffered voltage reference based on the transfer function convention presented in SectionB.1. The transfer functions of the transistor-level bulk switch (BSW), bandgap (BG), output buffer (BUF), and bias-tee (BT) are given in SectionsB.2,B.3,B.4,B.5, and the closed-form solutions for the perturbation signals in the top-level test bench are derived in SectionB.6.

B.1 Small-signal transfer function convention

The small-signal transfer functions $BLK_{ij}(s)$ of each transistor-level circuit or behavioural model BLK are modelled by fitting poles and zeroes to the frequency responses $BLK_{ij}(\jmath\omega)$ which are obtained using PSS or TRAN simulations of the BLK circuit. The analytical expression for a generic transfer function in the s-domain is given in Eq. (B.1):

$$f(s) = G \cdot \frac{\prod_{j=1}^{m}\left(1+\frac{s}{2\pi z_j}\right)}{\prod_{i=1}^{n}\left(1+\frac{s}{2\pi p_i}\right)} \tag{B.1}$$

where $s = 2\pi\sigma \pm \jmath\omega$ is the complex frequency in rad/s, G is the low-frequency gain, z_j are the m zeroes, and p_i are the n poles in Hz. Under this convention, the poles and zeroes with positive real parts are in the left half-plane (LHP), and the zeroes with negative real parts are in the right half-plane (RHP) of the complex s-domain. In order to enable linking the positions of the poles and zeroes in the pole-zero diagrams to the frequency response plots with a logarithmic frequency axis in Hz, the real part σ of the complex variable s is plotted as an absolute value in Hz.

B.2 Small-signal model of the transistor-level bulk switch circuit

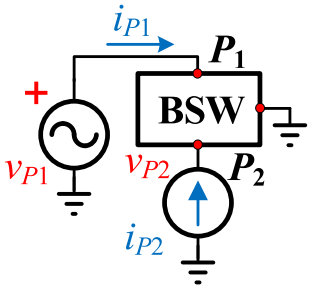


Figure B.1: AC test bench for simulating the small-signal behaviour of the bulk-switch.

The bulk switch is a 2-port circuit, and its small-signal transfer functions $BSW_{ij}(\jmath\omega)$ are simulated using the AC test bench shown in Fig.B.1. Port P_1 is the supply pin with the associated pin voltage v_{P1}, and port P_2 is the output pin that is connected to the load circuit, with the associated load current i_{P2}. The supply current i_{P1} flowing into port P_1 and the output voltage v_{P2} at port P_2 are defined as functions of v_{P1} and i_{P2} according to Eq. (B.2):

$$\begin{aligned} i_{P1} &= i_{BSW\_P1}(v_{P1}, i_{P2}) \\ v_{P2} &= v_{BSW\_P2}(v_{P1}, i_{P2}) \end{aligned} \tag{B.2}$$

Eq. (B.3) presents the linearized form of the relationships in the small-signal conditions around the operating point Q:

$$\begin{aligned} i_{p1} &= \left.\frac{\partial i_{BSW\_P1}}{\partial v_{BSW\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_{BSW\_P1}}{\partial i_{BSW\_P2}}\right|_Q \cdot i_{p2} = BSW_{11} \cdot v_{p1} + BSW_{12} \cdot i_{p2} \\ v_{p2} &= \left.\frac{\partial v_{BSW\_P2}}{\partial v_{BSW\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial v_{BSW\_P2}}{\partial i_{BSW\_P2}}\right|_Q \cdot i_{p2} = BSW_{21} \cdot v_{p1} + BSW_{22} \cdot i_{p2} \end{aligned} \tag{B.3}$$

Fig.B.2shows the frequency responses $BSW_{ij}(\jmath\omega)$ of the transistor-level bulk switch obtained using PSS simulations of the AC test bench shown in Fig.B.1, around the DC operating point Q defined in TableB.1. The associated transfer functions $BSW_{ij}(s)$ in the s-domain are obtained by manually fitting poles and zeroes of the transfer functions to the frequency responses $BSW_{ij}(\jmath\omega)$ (solid lines) obtained by simulations. The values of the low-frequency gain G, the zeroes z_j, and the poles p_i are summarized in TableB.2.

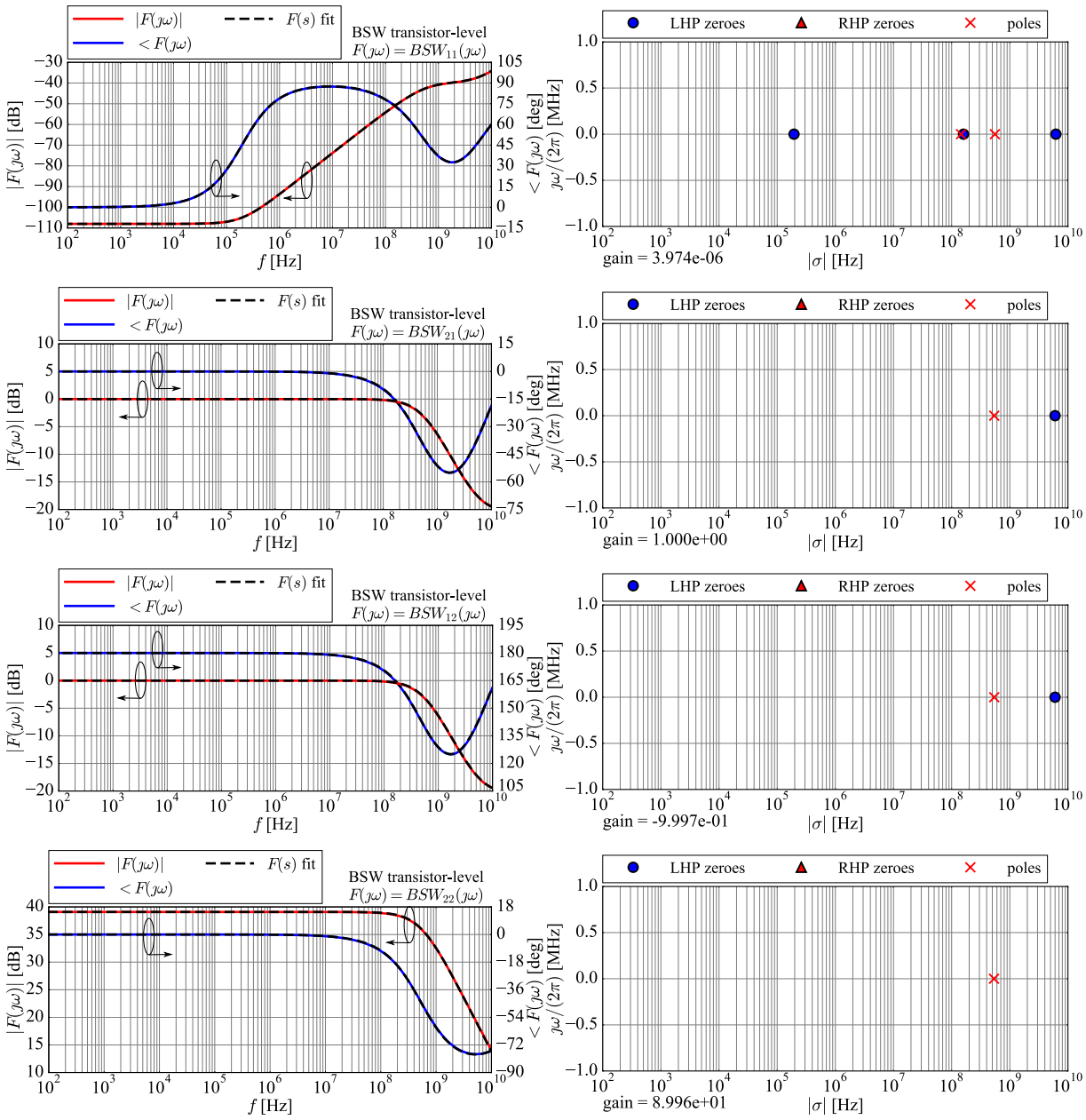


Figure B.2: Frequency responses $BSW_{ij}(j\omega)$ of the transistor-level bulk switch (solid lines), with the associated transfer functions $BSW_{ij}(s)$ in the s-domain, where $s = 2\pi\sigma \pm j\omega$.

Table B.1: DC operating point Q of the transistor-level bulk switch for small-signal PSS simulations.

signal	DC value
V_{BSW_P1}	3.3000 V
I_{BSW_P1}	17.7585 µA
V_{BSW_P2}	3.2989 V
I_{BSW_P2}	7.3212 µA

Table B.2: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $BSW_{ij}(s)$ of the transistor-level bulk switch.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$BSW_{11}(s) = \frac{\partial i_{BSW\_P1}}{\partial v_{BSW\_P1}}\Big\|_Q$	$3.974{\cdot}10^{-6}$	194.5k, 160M, 6.2G, -430G	145M, 555M
$BSW_{21}(s) = \frac{\partial v_{BSW\_P2}}{\partial v_{BSW\_P1}}\Big\|_Q$	$1.000{\cdot}10^{0}$	6G, 60G	540M
$BSW_{12}(s) = \frac{\partial i_{BSW\_P1}}{\partial i_{BSW\_P2}}\Big\|_Q$	$-9.997{\cdot}10^{-1}$	6G, 60G	540M
$BSW_{22}(s) = \frac{\partial v_{BSW\_P2}}{\partial i_{BSW\_P2}}\Big\|_Q$	$8.996{\cdot}10^{1}$	50G	535M

B.3 Small-signal model of the transistor-level output buffer

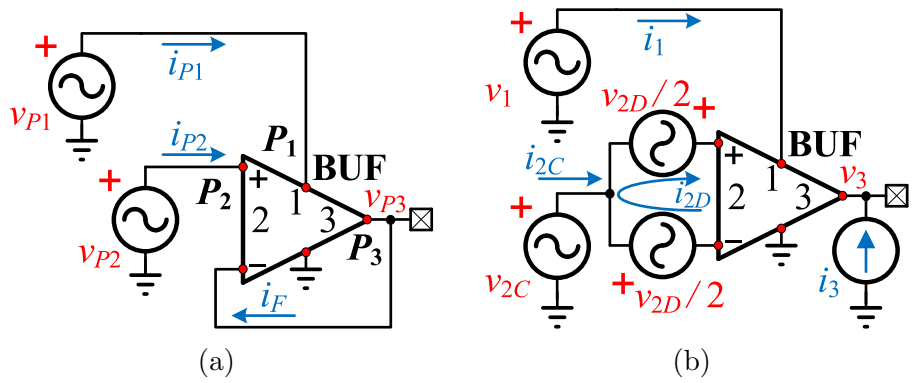


Figure B.3: AC test bench for simulating the small-signal behaviour of the output buffer: (a) as a voltage follower with a unity gain feedback connection, (b) in the open loop configuration.

The output buffer is a voltage follower implemented using an operational amplifier with a unity gain feedback connection, and its small-signal transfer functions are simulated using the AC test bench shown in Fig.B.3a. Port P_1 is the supply pin with the associated pin voltage v_{P1}, port P_2 is the input pin with the associated input voltage v_{P2}, and port P_3 is the output pin with the associated output voltage v_{P3}. The supply current i_{P1} flowing into port P_1, the input current i_{P2} flowing into port P_2, the output voltage v_{P3} at port P_3, and the current i_F flowing through the feedback connection are defined as functions of v_{P1} and v_{P2} according to Eq. (B.4):

$$\begin{aligned} i_{P1} &= i_{BUF\_P1}\left(v_{P1}, v_{P2}\right) \\ i_{P2} &= i_{BUF\_P2}\left(v_{P1}, v_{P2}\right) \\ v_{P3} &= v_{BUF\_P3}\left(v_{P1}, v_{P2}\right) \\ i_F &= i_F\left(v_{P1}, v_{P2}\right) \end{aligned} \tag{B.4}$$

Eq. (B.5) presents the linearized form of the relationships in the small-signal conditions around the operating point Q:

$$\begin{aligned} i_{p1} &= \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{p2} = BUF_{11} \cdot v_{p1} + BUF_{12} \cdot v_{p2} \\ i_{p2} &= \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{p2} = BUF_{21} \cdot v_{p1} + BUF_{22} \cdot v_{p2} \\ v_{p3} &= \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{p2} = BUF_{31} \cdot v_{p1} + BUF_{32} \cdot v_{p2} \\ i_F &= \left.\frac{\partial i_F}{\partial v_{BUF\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_F}{\partial v_{BUF\_P2}}\right|_Q \cdot v_{p2} = BUF_{41} \cdot v_{p1} + BUF_{42} \cdot v_{p2} \end{aligned} \tag{B.5}$$

The small-signal model of the output buffer is derived in the open loop configuration shown in Fig.B.3b, where port 1 is the supply pin with the associated pin voltage v_1 and current i_1 flowing into the buffer, port 2 is the differential input port driven using the common-mode voltage v_{2C} and differential-mode voltage v_{2D}, with the associated common-mode current i_{2C} and differential-mode current i_{2D}, and port 3 is the output pin with the associated pin voltage v_3 and current i_3 flowing into the buffer. The common- and differential-mode voltages v_{2C}, v_{2D} and currents i_{2C}, i_{2D} at port 2 are related to the single-ended voltage v_{2P} and current i_{2P} associated with the positive input pin of port 2, and to the single-ended voltage v_{2N} and current i_{2N} associated with the negative input pin of port 2 according to the expressions given in Eq. (B.6):

$$\begin{aligned} v_{2P} &= v_{2C} + \frac{v_{2D}}{2} \qquad & i_{2P} &= \frac{i_{2C}}{2} + i_{2D} \\ v_{2N} &= v_{2C} - \frac{v_{2D}}{2} \qquad & i_{2N} &= \frac{i_{2C}}{2} - i_{2D} \end{aligned} \tag{B.6}$$

The relationships between the voltages and currents in the voltage follower and the open loop configurations shown in Fig.B.3are derived using the relationships in Eq. (B.6), and are presented in Eq. (B.7):

$$\begin{aligned} v_1 &= v_{P1} & i_1 &= i_{P1} \\ v_{2C} &= \frac{v_{P2} + v_{P3}}{2} & i_{2C} &= i_{P2} + i_F \\ v_{2D} &= v_{P2} - v_{P3} & i_{2D} &= \frac{i_{P2} - i_F}{2} \\ v_3 &= v_{P3} & i_3 &= -i_F \end{aligned} \tag{B.7}$$

In the open loop, the supply current i_1, the common-mode input current i_{2C}, the differential-mode input current i_{2D}, and the output voltage v_3 are modelled as functions of the supply voltage v_1, the common-mode input voltage v_{2C}, the differential-mode input voltage v_{2D}, and the output current i_3. The output current i_3 is used as an input signal because: (i) a non-zero AC current i_f flows through the feedback branch of the buffer in the voltage follower configuration, and (ii) to set the equal DC values of the output voltage V_3 and the input voltage V_{2C} in the open loop that is maintained by the unity gain feedback connection in the closed loop. These relationships are summarized in Eq. (B.8):

$$\begin{aligned} i_1 &= i_1\left(v_1, v_{2C}, v_{2D}, i_3\right) \\ i_{2C} &= i_{2C}\left(v_1, v_{2C}, v_{2D}, i_3\right) \\ i_{2D} &= i_{2D}\left(v_1, v_{2C}, v_{2D}, i_3\right) \\ v_3 &= v_3\left(v_1, v_{2C}, v_{2D}, i_3\right) \end{aligned} \tag{B.8}$$

Eq. (B.9) presents the linearized form of the relationships in the small-signal conditions around the operating point Q:

$$\begin{aligned} i_1 &= \left.\frac{\partial i_1}{\partial v_1}\right|_Q \cdot v_1 + \left.\frac{\partial i_1}{\partial v_{2C}}\right|_Q \cdot v_{2c} + \left.\frac{\partial i_1}{\partial v_{2D}}\right|_Q \cdot v_{2d} + \left.\frac{\partial i_1}{\partial i_3}\right|_Q \cdot i_3 \\ i_{2c} &= \left.\frac{\partial i_{2C}}{\partial v_1}\right|_Q \cdot v_1 + \left.\frac{\partial i_{2C}}{\partial v_{2C}}\right|_Q \cdot v_{2c} + \left.\frac{\partial i_{2C}}{\partial v_{2D}}\right|_Q \cdot v_{2d} + \left.\frac{\partial i_{2C}}{\partial i_3}\right|_Q \cdot i_3 \\ i_{2d} &= \left.\frac{\partial i_{2D}}{\partial v_1}\right|_Q \cdot v_1 + \left.\frac{\partial i_{2D}}{\partial v_{2C}}\right|_Q \cdot v_{2c} + \left.\frac{\partial i_{2D}}{\partial v_{2D}}\right|_Q \cdot v_{2d} + \left.\frac{\partial i_{2D}}{\partial i_3}\right|_Q \cdot i_3 \\ v_3 &= \left.\frac{\partial v_3}{\partial v_1}\right|_Q \cdot v_1 + \left.\frac{\partial v_3}{\partial v_{2C}}\right|_Q \cdot v_{2c} + \left.\frac{\partial v_3}{\partial v_{2D}}\right|_Q \cdot v_{2d} + \left.\frac{\partial v_3}{\partial i_3}\right|_Q \cdot i_3 \end{aligned} \tag{B.9}$$

The sixteen partial derivatives in Eq. (B.9) are labelled using the small-signal transfer functions A_{ij} for brevity, according to Eq. (B.10):

$$\begin{aligned} i_1 &= A_{11} \cdot v_1 + A_{12} \cdot v_{2c} + A_{13} \cdot v_{2d} + A_{14} \cdot i_3 \\ i_{2c} &= A_{21} \cdot v_1 + A_{22} \cdot v_{2c} + A_{23} \cdot v_{2d} + A_{24} \cdot i_3 \\ i_{2d} &= A_{31} \cdot v_1 + A_{32} \cdot v_{2c} + A_{33} \cdot v_{2d} + A_{34} \cdot i_3 \\ v_3 &= A_{41} \cdot v_1 + A_{42} \cdot v_{2c} + A_{43} \cdot v_{2d} + A_{44} \cdot i_3 \end{aligned} \tag{B.10}$$

Figs.B.4,B.5,B.6,B.7show the frequency responses $A_{ij}\left(\jmath\omega\right)$ of the transistor-level output buffer in the open loop obtained using PSS simulations of the AC test bench shown in Fig.B.3b, around the DC operating point Q defined in TableB.3. The associated transfer functions $A_{ij}\left(s\right)$ in the s-domain are obtained by manually fitting poles and zeroes to the simulated frequency responses $A_{ij}\left(\jmath\omega\right)$ (solid lines). The values of the low-frequency gain G, the zeroes z_j, and the poles p_i according to the transfer function expression in Eq. (B.1) are summarized in TablesB.4,B.5,B.6,B.7.

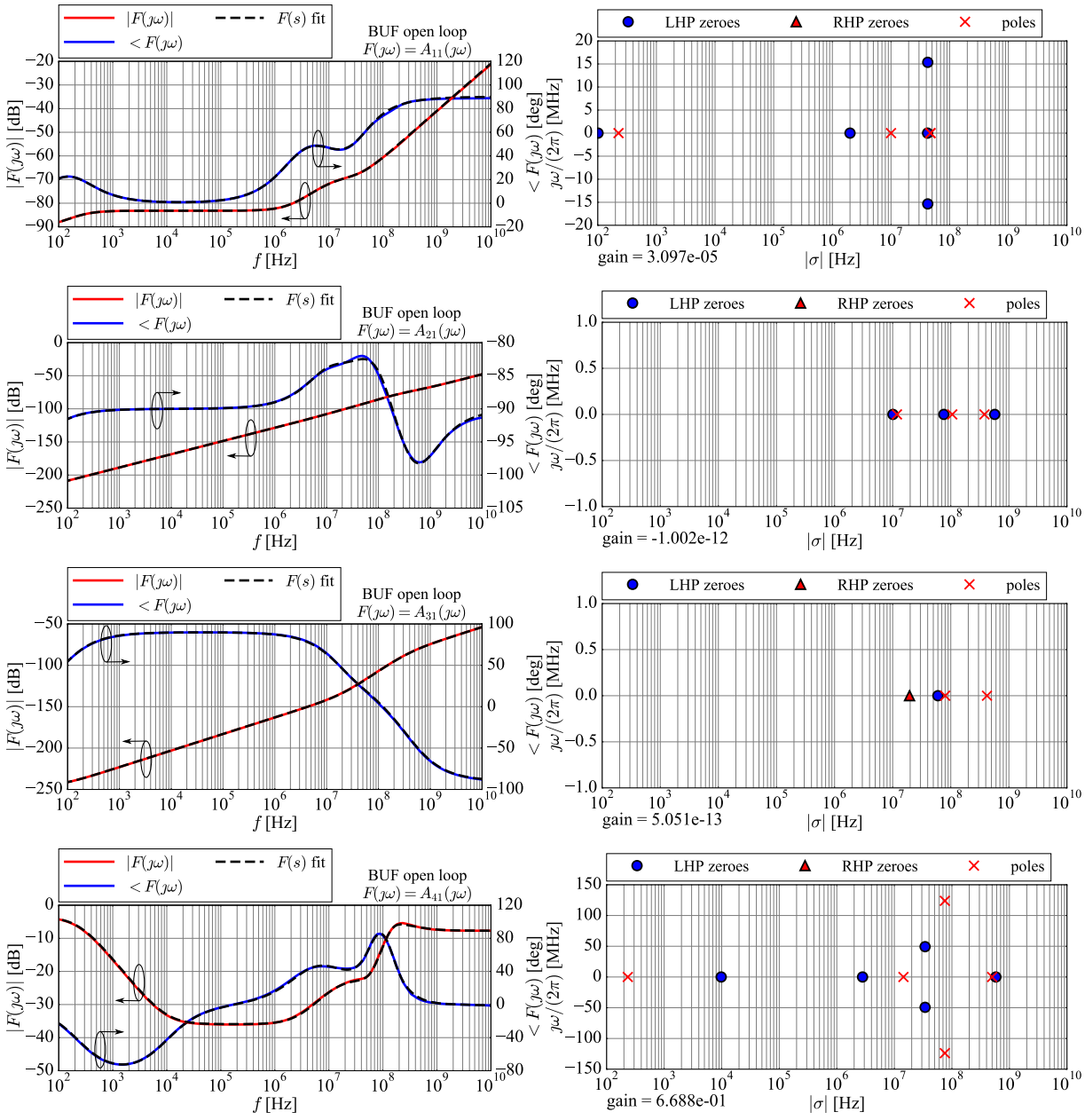


Figure B.4: Frequency responses $A_{i1}(j\omega)$ of the transistor-level output buffer in the open loop (solid lines), with the associated transfer functions $A_{i1}(s)$ in the s-domain against the input voltage v_1, where $s = 2\pi\sigma \pm j\omega$.

Table B.3: DC operating point Q of the transistor-level output buffer in the open loop for small-signal PSS simulations.

signal	DC value
V_{BUF_P1}	3.3000 V
I_{BUF_P1}	559.5431 µA
V_{BUF_P2}	1.23382 V
I_{BUF_P2}	0.0000 A
V_{BUF_P3}	1.23398 V
I_{BUF_P3}	272.869105 µA

Table B.4: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $A_{i1}(s)$ transistor-level output buffer in the open loop against the supply voltage v_1.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$A_{11}(s) = \frac{\partial i_1}{\partial v_1}\Big\vert_Q$	3.097·10^{-5}	101, 2M, 42M, 42.3M ± $\jmath$15.35M	226, 10M, 47M, 47M
$A_{21}(s) = \frac{\partial i_{2C}}{\partial v_1}\Big\vert_Q$	-1.002·10^{-12}	2.7, 10.1M, 76M, 570M	11.85M, 106M, 380M
$A_{31}(s) = \frac{\partial i_{2D}}{\partial v_1}\Big\vert_Q$	5.051·10^{-13}	-19.5M, 71, 60M	80M, 420M
$A_{41}(s) = \frac{\partial v_3}{\partial v_1}\Big\vert_Q$	6.688·10^{-1}	9.8k, 2.8M, 34.2M ± $\jmath$49.3M, 580M	234, 14.4M, 75.4M ± $\jmath$123.9M, 500M, 450G

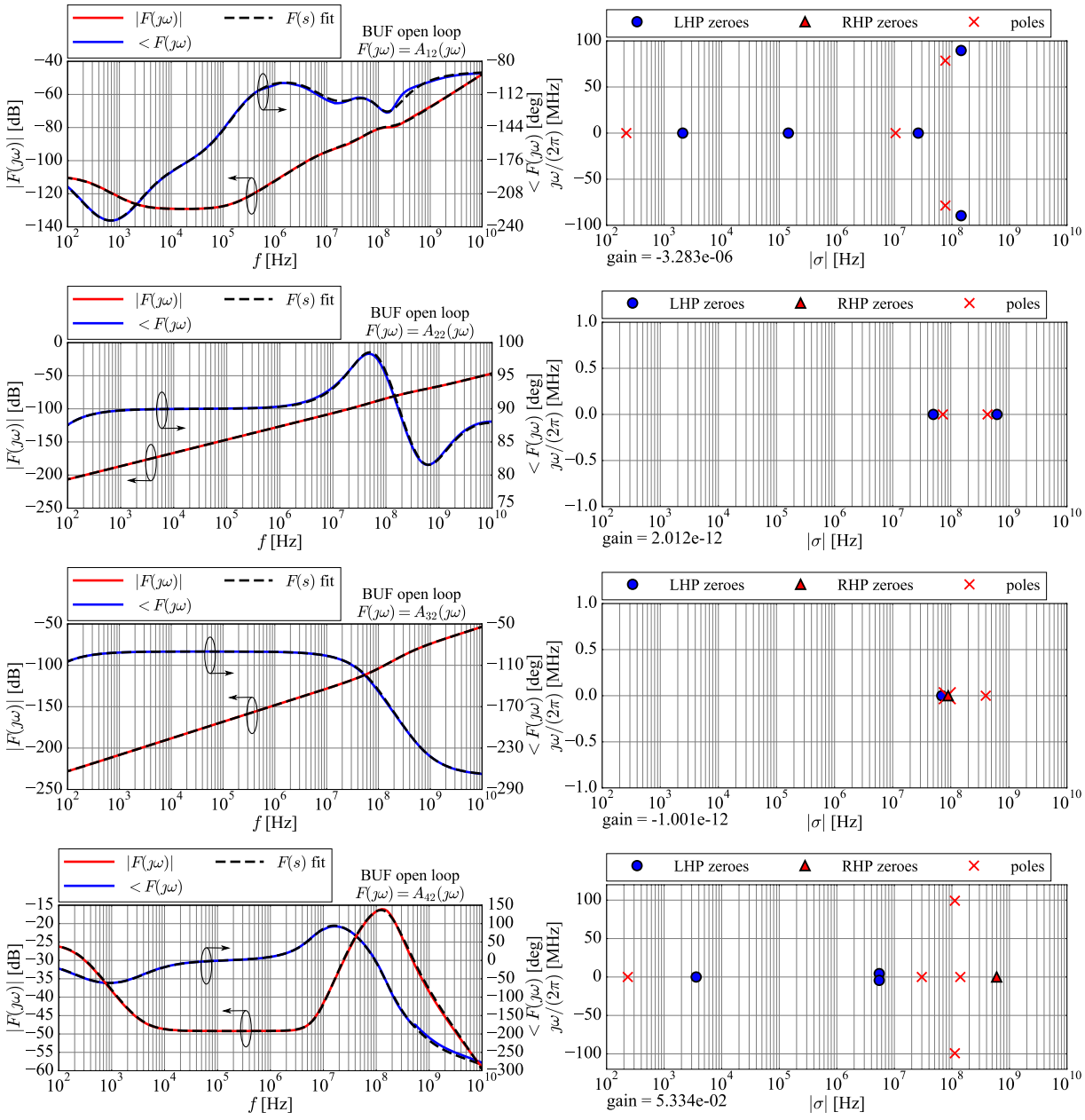


Figure B.5: Frequency responses $A_{i2}(j\omega)$ of the transistor-level output buffer in the open loop (solid lines), with the associated transfer functions $A_{i2}(s)$ in the s-domain against the common-mode input voltage v_{2C}, where $s = 2\pi\sigma \pm j\omega$.

Table B.5: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $A_{i2}(s)$ of transistor-level output buffer in the open loop against the common-mode input voltage v_{2C}.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$A_{12}(s) = \frac{\partial i_1}{\partial v_{2C}}\Big\vert_Q$	-3.283·10^{-6}	2.1k, 143.8k, 26M, 144.5M ± $\jmath$89.55M	220, 10.5M, 77M ± $\jmath$78.56M
$A_{22}(s) = \frac{\partial i_{2C}}{\partial v_{2C}}\Big\vert_Q$	2.012·10^{-12}	4.3, 50M, 625M	73M, 430M, 500G
$A_{32}(s) = \frac{\partial i_{2D}}{\partial v_{2C}}\Big\vert_Q$	-1.001·10^{-12}	26, 70M, -90M	87M, 400M
$A_{42}(s) = \frac{\partial v_3}{\partial v_{2C}}\Big\vert_Q$	5.334·10^{-2}	3.6k, 5.46M ± $\jmath$4.38M, -600M	233, 30M, 112.5M ± $\jmath$99.22M, 140M, 25G

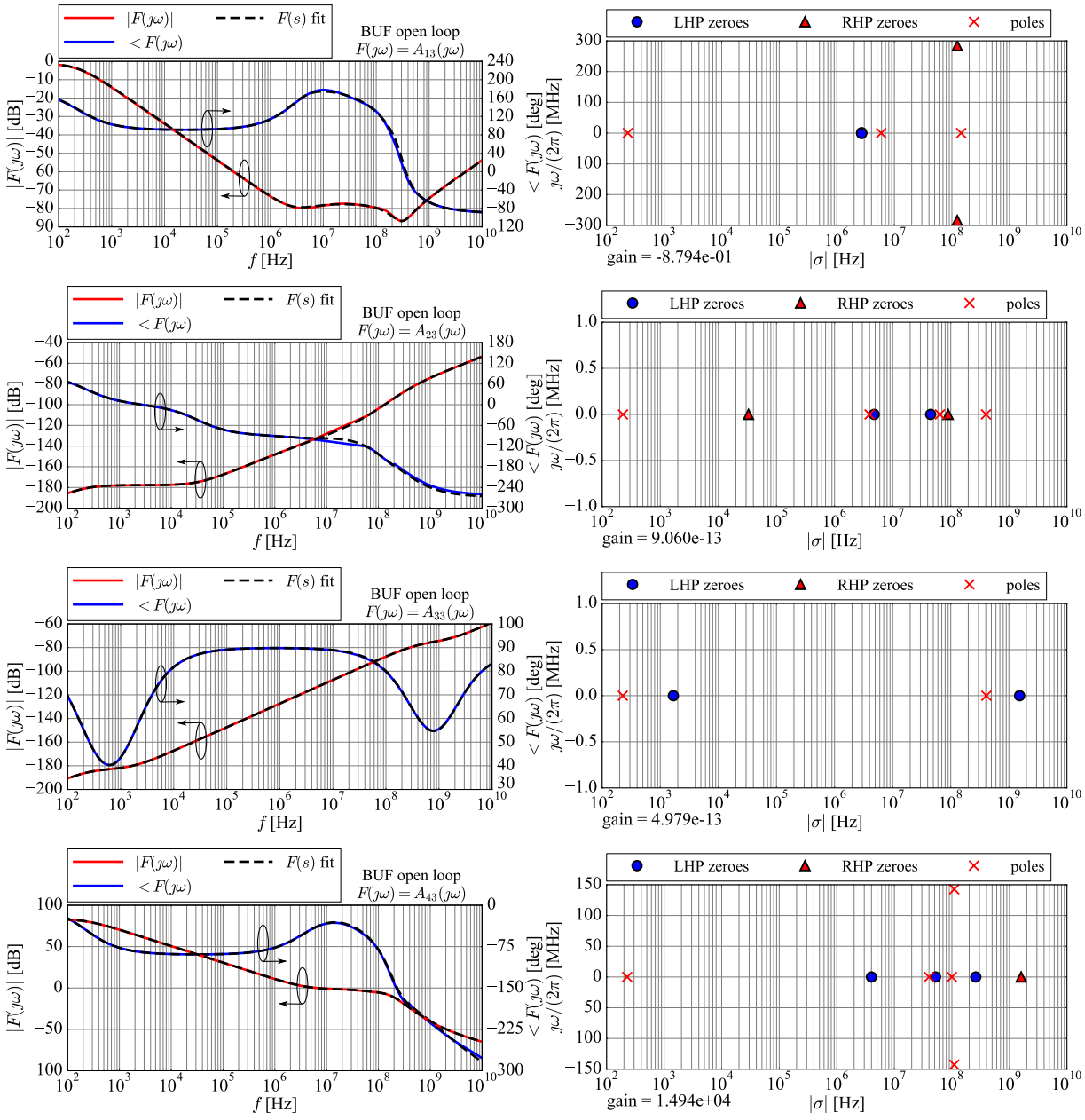


Figure B.6: Frequency responses $A_{i3}(j\omega)$ of the transistor-level output buffer in the open loop (solid lines), with the associated transfer functions $A_{i3}(s)$ in the s-domain against the differential-mode input voltage v_{2D}, where $s = 2\pi\sigma \pm j\omega$.

Table B.6: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $A_{i3}(s)$ transistor-level output buffer in the open loop against the differential-mode input voltage v_{2D}.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$A_{13}(s) = \frac{\partial i_1}{\partial v_{2D}}\Big\vert_Q$	-8.794·10^{-1}	2.7M ± $\jmath$1.3M, -124M ± $\jmath$284.1M	233, 5.9M, 145M
$A_{23}(s) = \frac{\partial i_{2C}}{\partial v_{2D}}\Big\vert_Q$	9.060·10^{-13}	0, -33k, 4.8M, 45M, -90M	228, 4M, 65M, 404M
$A_{33}(s) = \frac{\partial i_{2D}}{\partial v_{2D}}\Big\vert_Q$	4.979·10^{-13}	0.16, 1.68k, 1.53G	226, 410M, 1200G
$A_{43}(s) = \frac{\partial v_3}{\partial v_{2D}}\Big\vert_Q$	1.494·10^{4}	4M, 52M, 260M, -1.6G, -21G	228, 40M, 100M, 109.8M ± $\jmath$142.6M

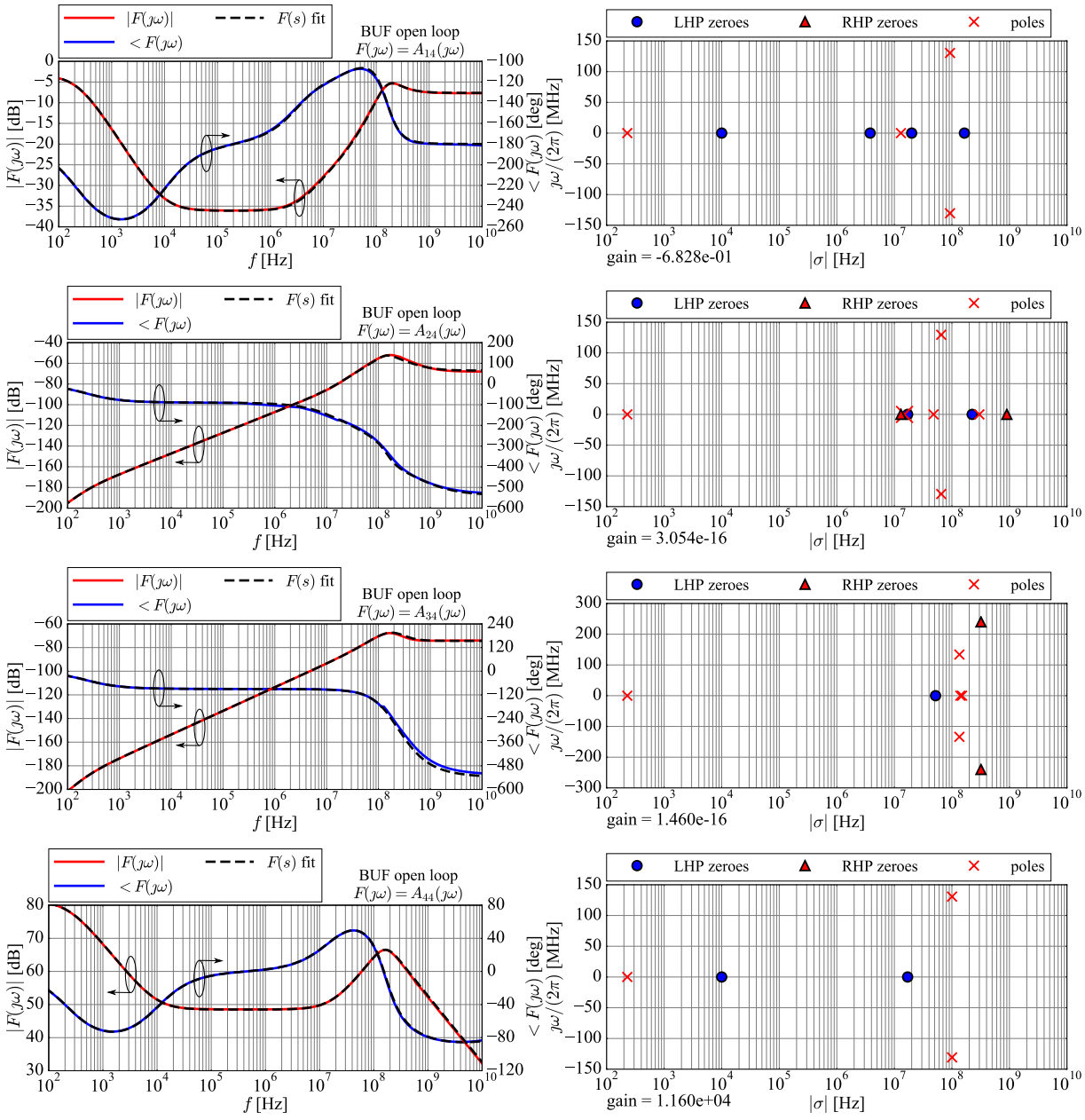


Figure B.7: Frequency responses $A_{i4}(j\omega)$ of the transistor-level output buffer in the open loop (solid lines), with the associated transfer functions $A_{i4}(s)$ in the s-domain against the output current i_3, where $s = 2\pi\sigma \pm j\omega$.

Table B.7: The low-frequency gain G, zeroes z_j, and poles p_i of the loop transfer functions $A_{i4}(s)$ transistor-level output buffer in the open against the output current i_3.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$A_{14}(s) = \frac{\partial i_1}{\partial i_3}\Big\vert_Q$	-6.828·10^{-1}	10k, 3.8M, 20M, 165M	229, 13M, 92.8M ± $\jmath$130.3M
$A_{24}(s) = \frac{\partial i_{2C}}{\partial i_3}\Big\vert_Q$	3.054·10^{-16}	0, -0.1, -13M, 17M, 225M, -900M	229, 15M, 48M, 300M, 65.2M ± $\jmath$129.5M
$A_{34}(s) = \frac{\partial i_{2D}}{\partial i_3}\Big\vert_Q$	1.460·10^{-16}	0, -0.1, 52M, -320M ± $\jmath$240M	229, 140M, 150M, 134.9M ± $\jmath$133.8M
$A_{44}(s) = \frac{\partial v_3}{\partial i_3}\Big\vert_Q$	1.160·10^{4}	0.01, 17M, 120G	229, 100.6M ± $\jmath$130.7M

The small-signal transfer functions $BUF_{ij}(s)$ of the output buffer in the voltage follower configuration shown in Fig.B.3aare obtained analytically using the known sixteen small-signal transfer functions $A_{ij}(s)$ in the open loop as follows. After substituting Eq. (B.10) into Eq. (B.7), the small-signal output voltage v_{p3} and the small-signal feedback current i_f form a system of two equations in two variables given in Eq. (B.11):

$$\begin{aligned} v_{P3} \cdot f_1 &= A_{41} \cdot v_{P1} + f_2 \cdot v_{P2} - A_{44} \cdot i_f \\ i_f \cdot f_3 &= f_4 \cdot v_{P1} + f_5 \cdot v_{P2} + f_6 \cdot v_{P3} \end{aligned} \tag{B.11}$$

where f_i are the helper functions defined in Eq. (B.12):

$$\begin{aligned} f_1 &= 1 + A_{43} - \frac{A_{42}}{2} & f_4 &= \frac{A_{21}}{2} - A_{31} \\ f_2 &= A_{43} + \frac{A_{42}}{2} & f_5 &= \frac{A_{22}}{4} - \frac{A_{32}}{2} + \frac{A_{23}}{2} - A_{33} \\ f_3 &= 1 + \frac{A_{24}}{2} - A_{34} & f_6 &= \frac{A_{22}}{4} - \frac{A_{32}}{2} - \frac{A_{23}}{2} + A_{33} \end{aligned} \tag{B.12}$$

The solution of the above equation system is given in Eq. (B.13):

$$\begin{aligned} v_{P3} \cdot f_7 &= f_8 \cdot v_{P1} + f_9 \cdot v_{P2} \\ i_f \cdot f_7 &= f_{10} \cdot v_{P1} + f_{11} \cdot v_{P2} \end{aligned} \tag{B.13}$$

where f_i are the additional helper functions defined in Eq. (B.14):

$$\begin{aligned} f_7 &= f_1 f_3 + A_{44} f_6 & f_{10} &= f_1 f_4 + A_{41} f_6 \\ f_8 &= A_{41} f_3 - A_{44} f_4 & f_{11} &= f_1 f_5 + f_2 f_6 \\ f_9 &= f_2 f_3 - A_{44} f_5 \end{aligned} \tag{B.14}$$

The solutions for the remaining output variables i_{P1} and i_{P2} are obtained by substituting Eq. (B.13) into Eqs. (B.7), (B.10), and are presented in Eq. (B.15):

$$\begin{aligned} i_{P1} \cdot f_7 &= f_{12} \cdot v_{P1} + f_{13} \cdot v_{P2} \\ i_{P2} \cdot f_7 &= f_{16} \cdot v_{P1} + f_{17} \cdot v_{P2} \end{aligned} \tag{B.15}$$

where the additional helper functions f_i are defined in Eq. (B.16):

$$
\begin{aligned}
f_{12} &= A_{11} f_7 + \left(\frac{A_{12}}{2} - A_{13}\right) f_8 - A_{14} f_{10} \\
f_{13} &= \left(\frac{A_{12}}{2} + A_{13}\right) f_7 + \left(\frac{A_{12}}{2} - A_{13}\right) f_9 - A_{14} f_{11} \\
f_{14} &= \frac{A_{22}}{4} + \frac{A_{32}}{2} + \frac{A_{23}}{2} + A_{33} \\
f_{15} &= \frac{A_{22}}{4} + \frac{A_{32}}{2} - \frac{A_{23}}{2} - A_{33} \\
f_{16} &= \left(\frac{A_{21}}{2} + A_{31}\right) f_7 + f_8 f_{15} - \left(\frac{A_{24}}{2} + A_{34}\right) f_{10} \\
f_{17} &= f_7 f_{14} + f_9 f_{15} - \left(\frac{A_{24}}{2} + A_{34}\right) f_{11}
\end{aligned}
\tag{B.16}
$$

The analytical expressions for the output buffer transfer functions are obtained from the small-signal relationships given in Eqs. (B.13) and (B.15), and are given in Eq. (B.17):

$$
\begin{aligned}
BUF_{11}(s) &= \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P1}}\right|_Q = \frac{f_{12}}{f_7}, & BUF_{12}(s) &= \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P2}}\right|_Q = \frac{f_{13}}{f_7} \\
BUF_{21}(s) &= \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P1}}\right|_Q = \frac{f_{16}}{f_7}, & BUF_{22}(s) &= \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P2}}\right|_Q = \frac{f_{17}}{f_7} \\
BUF_{31}(s) &= \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P1}}\right|_Q = \frac{f_8}{f_7}, & BUF_{32}(s) &= \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P2}}\right|_Q = \frac{f_9}{f_7} \\
BUF_{41}(s) &= \left.\frac{\partial i_F}{\partial v_{BUF\_P1}}\right|_Q = \frac{f_{10}}{f_7}, & BUF_{42}(s) &= \left.\frac{\partial i_F}{\partial v_{BUF\_P2}}\right|_Q = \frac{f_{11}}{f_7}
\end{aligned}
\tag{B.17}
$$

where the helper functions f_i are linked to the known open loop transfer functions $A_{ij}(s)$ through Eqs. (B.12), (B.14), (B.16). The analytical expressions for the output buffer transfer functions $BUF_{ij}(s)$ consisting of polynomial numerators and denominators in the complex variable s are obtained by substituting the known analytical expressions for $A_{ij}(s)$ into Eq. (B.17) using the Python symbolic library SymPy. For each transfer function $BUF_{ij}(s)$, the poles and zeroes are determined by finding the polynomial roots of the numerator and the denominator using the Python scientific library NumPy. The roots that are common to the numerator and the denominator are identified graphically in the complex s-plane and manually removed, and the final poles and zeroes are manually tuned to improve the matching to the simulated frequency response $BUF_{ij}(\jmath\omega)$. The resulting transfer functions $BUF_{ij}(s)$ are presented in Figs.B.8,B.9, and are compared to the frequency responses $BUF_{ij}(\jmath\omega)$ of the transistor-level output buffer obtained using PSS simulations of the AC test bench shown in Fig.B.3a. The values of the low-frequency gain G, the zeroes z_j, and the poles p_i are summarized in TablesB.8,B.9.

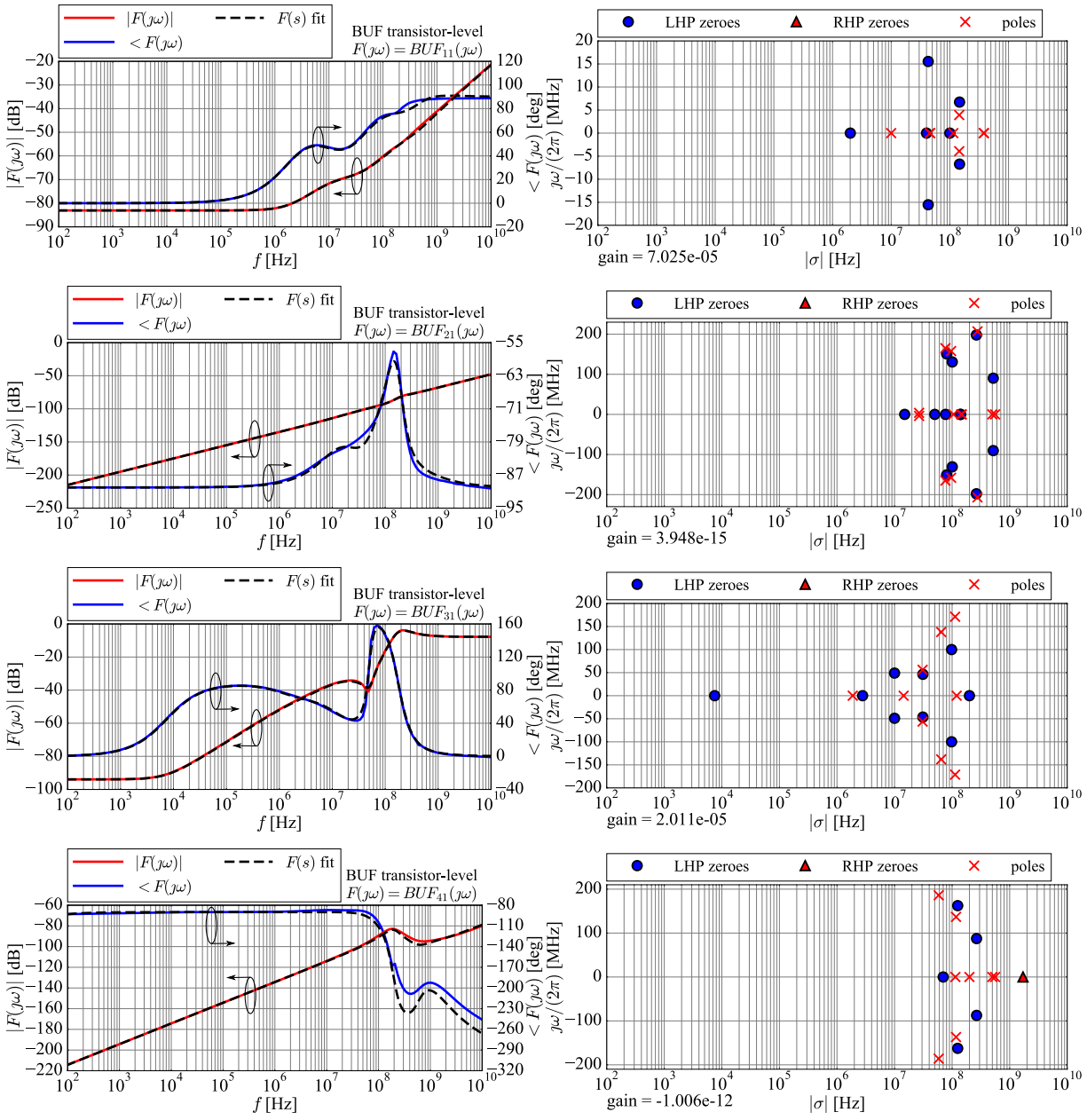


Figure B.8: Frequency responses $BUF_{i1}(j\omega)$ of the transistor-level output buffer in the voltage follower configuration (solid lines), with the associated transfer functions $BUF_{i1}(s)$ in the s-domain against the input voltage v_{P1}, where $s = 2\pi\sigma \pm j\omega$.

Table B.8: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $BUF_{i1}(s)$ of the transistor-level output buffer in the voltage follower configuration against the supply voltage v_{P1}.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$BUF_{11}(s) = \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P1}}\right\|_Q$	$7.025{\cdot}10^{-5}$	2M, 40M, 100M, 42.8M ± $\jmath$15.5M, 146.2M ± $\jmath$6.7M, 352.8M ± $\jmath$218.6M	10M, 46M, 46M, 114.5M, 144.5M ± $\jmath$3.9M, 380M, 380M
$BUF_{21}(s) = \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P1}}\right\|_Q$	$3.948{\cdot}10^{-15}$	0, 15M, 50M, 77.1M, 80.4M ± $\jmath$150.9M, 100.7M ± $\jmath$130.7M, 139.8M, 140.2M, 264M ± $\jmath$198M, 518.7M ± $\jmath$90.3M	26.7M ± $\jmath$3.8M, 76.4M ± $\jmath$165.2M, 96.2M ± $\jmath$158M, 105.7M, 144.5M, 147.3M, 276M ± $\jmath$207M, 499.2M, 558.6M
$BUF_{31}(s) = \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P1}}\right\|_Q$	$2.011{\cdot}10^{-5}$	7.5k, 2.78M, 200M, 10M ± $\jmath$49M, 31M ± $\jmath$46.4M, 98M ± $\jmath$100M	1.9M, 14.4M, 120M, 30.7M ± $\jmath$56.1M, 64.6M ± $\jmath$138M, 112.8M ± $\jmath$171.2M
$BUF_{41}(s) = \left.\frac{\partial i_F}{\partial v_{BUF\_P1}}\right\|_Q$	$-1.006{\cdot}10^{-12}$	5.2, 70M, 125.1M ± $\jmath$162.4M, 266M ± $\jmath$87.4M, 271M ± $\jmath$519.1M, -1.7G, -80G	58.5M ± $\jmath$186M, 117M ± $\jmath$136.8M, 114M, 200M, 500M, 558.6M, 450G, 500G

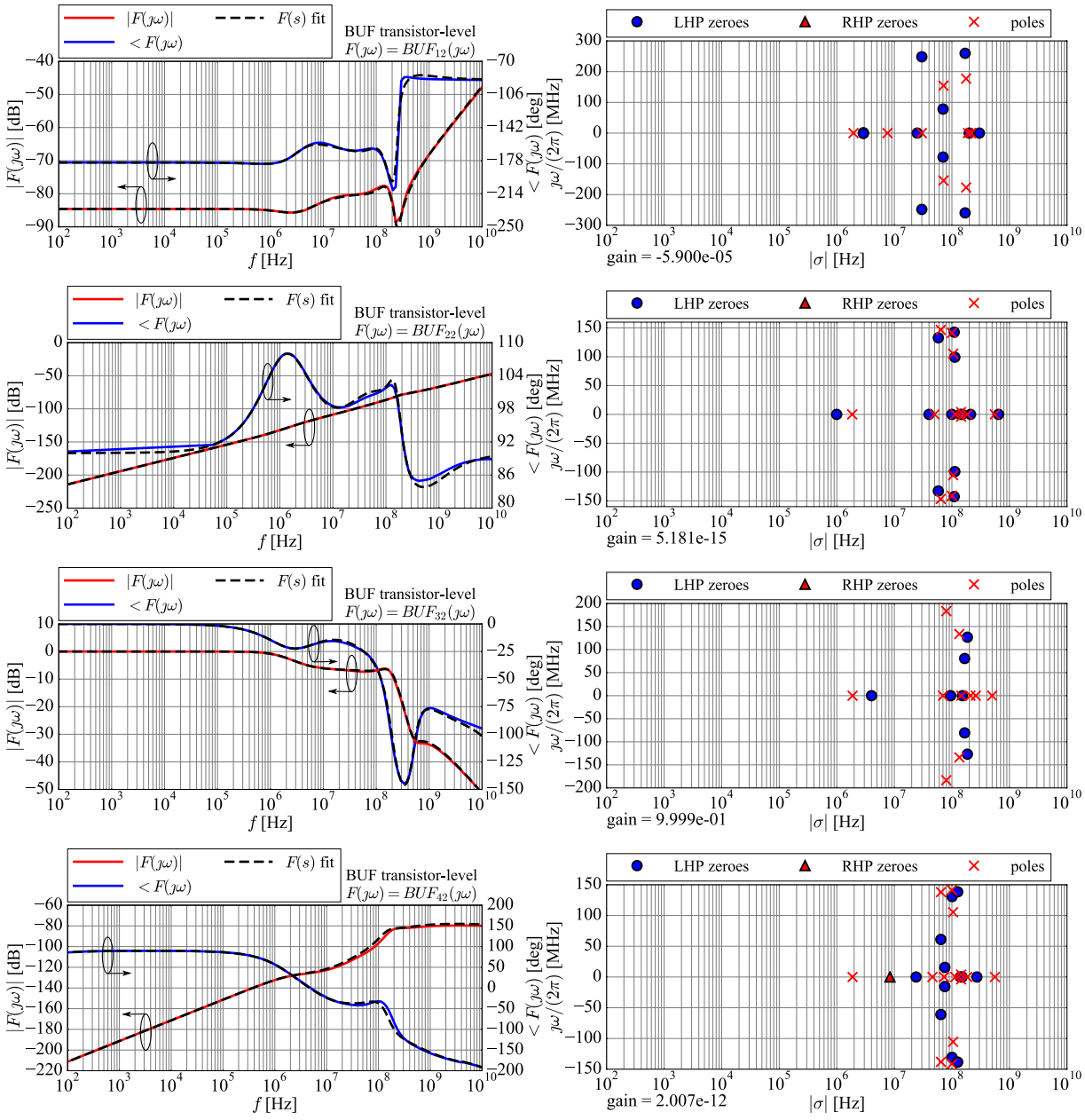


Figure B.9: Frequency responses $BUF_{i2}(j\omega)$ of the transistor-level output buffer in the voltage follower configuration (solid lines), with the associated transfer functions $BUF_{i2}(s)$ in the s-domain against the input voltage v_{P2}, where $s = 2\pi\sigma \pm j\omega$.

Table B.9: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $BUF_{i2}(s)$ of the transistor-level output buffer in the voltage follower configuration against the input voltage v_{P2}.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$BUF_{12}(s) = \left.\frac{\partial i_{BUF\_P1}}{\partial v_{BUF\_P2}}\right\|_Q$	-5.900·10^{-5}	2.9M ± $\jmath$1.2M, 25M, 200M, 300M, 30M ± $\jmath$248.2M, 70.1M ± $\jmath$78M, 169.6M ± $\jmath$259.5M	1.95M, 7.6M, 30M, 71.4M ± $\jmath$154.3M, 176.5M ± $\jmath$177.1M, 190M, 215M, 215M
$BUF_{22}(s) = \left.\frac{\partial i_{BUF\_P2}}{\partial v_{BUF\_P2}}\right\|_Q$	5.180·10^{-15}	0, 995k, 40M, 58M ± $\jmath$132.9M, 100M, 140M, 150M, 109.8M ± $\jmath$142.6M, 112.5M ± $\jmath$99.2M, 210.7M, 645.2M	1.9M, 50M, 114.5M, 64M ± $\jmath$146.6M, 99.9M ± $\jmath$141.3M, 105M ± $\jmath$105.4M, 144.4M ± $\jmath$3.9M, 184.5M, 558.6M
$BUF_{32}(s) = \left.\frac{\partial v_{BUF\_P3}}{\partial v_{BUF\_P2}}\right\|_Q$	9.999·10^{-1}	4M, 95M, 152M, 150M ± $\jmath$477M, 166.5M ± $\jmath$80.6M, 185.9M ± $\jmath$126.8M, -7.3G ± $\jmath$25.6G	1.87M, 70M, 210M, 80M ± $\jmath$183.3M, 134.9M ± $\jmath$133.8M, 145.6M, 260M, 500M
$BUF_{42}(s) = \left.\frac{\partial i_F}{\partial v_{BUF\_P2}}\right\|_Q$	2.007·10^{-12}	7.36, -8.4M, 23.9M, 64.2M ± $\jmath$61M, 75.4M ± $\jmath$15.6M, 100.7M ± $\jmath$130.7M, 126.1M ± $\jmath$138.4M, 139.8M, 150.3M, 271.7M, -9.8G ± $\jmath$26.9G	1.87M, 45.9M, 73M, 64.6M ± $\jmath$138M, 99.9M ± $\jmath$141.3M, 105M ± $\jmath$105.4M, 144.4M ± $\jmath$3.9M, 114.5M, 184.5M, 558.6M, 500G

B.4 Small-signal model of the transistor-level bandgap block

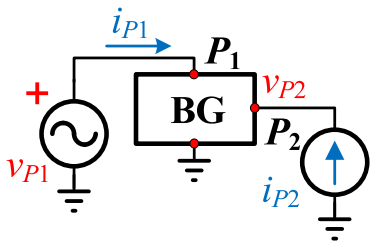


Figure B.10: AC test bench for simulating the small-signal behaviour of the bandgap block.

The bandgap block is a 2-port block, and its small-signal transfer functions are simulated using the AC test bench shown in Fig.B.10. Port P_1 is the supply pin with the associated pin voltage v_{P1}, and port P_2 is the output pin that is connected to the load circuit, with the associated load current i_{P2}. The supply current i_{P1} flowing into port P_1 and the load voltage v_{P2} at port P_2 are defined as functions of v_{P1} and i_{P2} according to Eq. (B.18):

$$\begin{aligned} i_{P1} &= i_{BG\_P1}\left(v_{P1}, i_{P2}\right) \\ v_{P2} &= v_{BG\_P2}\left(v_{P1}, i_{P2}\right) \end{aligned} \tag{B.18}$$

Eq. (B.19) presents the linearized form of the relationships in the small-signal conditions around the operating point Q:

$$\begin{aligned} i_{p1} &= \left.\frac{\partial i_{BG\_P1}}{\partial v_{BG\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_{BG\_P1}}{\partial i_{BG\_P2}}\right|_Q \cdot i_{p2} = BG_{11} \cdot v_{p1} + BG_{12} \cdot i_{p2} \\ v_{p2} &= \left.\frac{\partial v_{BG\_P2}}{\partial v_{BG\_P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial v_{BG\_P2}}{\partial i_{BG\_P2}}\right|_Q \cdot i_{p2} = BG_{21} \cdot v_{p1} + BG_{22} \cdot i_{p2} \end{aligned} \tag{B.19}$$

Fig.B.11shows the frequency responses $BG_{ij}\left(\jmath\omega\right)$ of the transistor-level bandgap block obtained using PSS simulations of the AC test bench shown in Fig.B.10, around the DC operating point Q defined in TableB.10. The associated transfer functions $BG_{ij}\left(s\right)$ in the s-domain are obtained by manually fitting poles and zeroes to the simulated frequency responses $BG_{ij}\left(\jmath\omega\right)$. The values of the low-frequency gain G, the zeroes z_j, and the poles p_i are summarized in TableB.11.

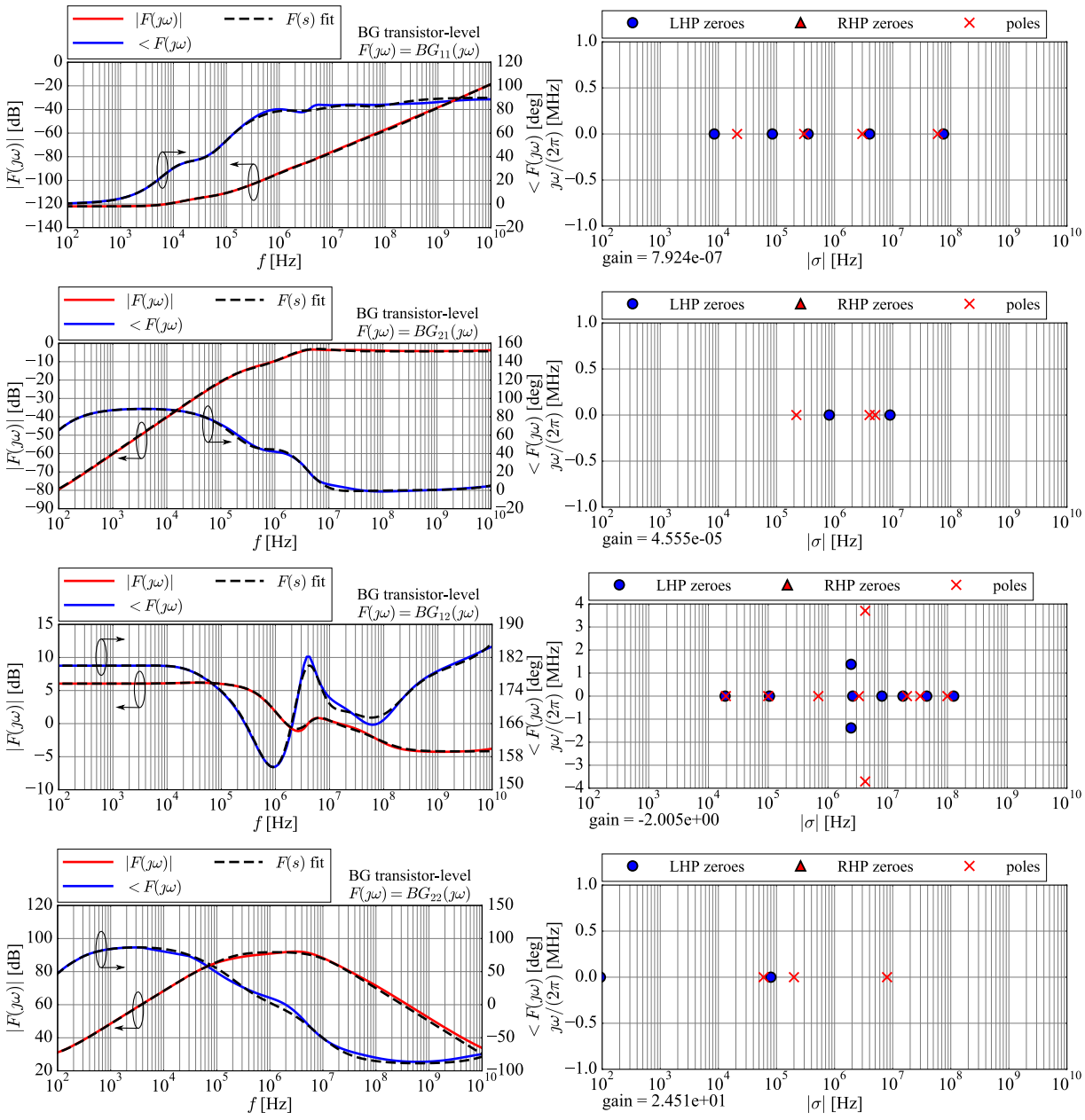


Figure B.11: Frequency responses $BG_{ij}\,(\jmath\omega)$ of the transistor-level bandgap block (solid lines), with the associated transfer functions $BG_{ij}\,(s)$ in the s-domain, where $s = 2\pi\sigma \pm \jmath\omega$.

Table B.10: DC operating point Q of the transistor-level bandgap block for small-signal PSS simulations.

signal	DC value
V_{BG_P1}	3.2989 V
I_{BG_P1}	7.3212 µA
V_{BG_P2}	1.23382 V
I_{BG_P2}	0.0000 µA

Table B.11: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $BG_{ij}(s)$ of the transistor-level bandgap block.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$BG_{11}(s) = \left.\frac{\partial i_{BG\_P1}}{\partial v_{BG\_P1}}\right\|_Q$	7.924·10^{-7}	8.5k, 85k, 350k, 4M, 75M	21k, 299k, 3M, 60M
$BG_{21}(s) = \left.\frac{\partial v_{BG\_P2}}{\partial v_{BG\_P1}}\right\|_Q$	4.555·10^{-5}	45.5, 810k, 9M, 110G	220k, 4M, 5M
$BG_{12}(s) = \left.\frac{\partial i_{BG\_P1}}{\partial i_{BG\_P2}}\right\|_Q$	-2.005·10^{0}	19k, 105k, 2.6M, 8M, 2.4M ± $\jmath$1.4M, 18M, 45M, 127M, 100G	19.6k, 100k, 690k, 3.3M, 4.2M ± $\jmath$3.7M, 21M, 35M, 100M
$BG_{22}(s) = \left.\frac{\partial v_{BG\_P2}}{\partial i_{BG\_P2}}\right\|_Q$	2.451·10^{1}	93, 80k, 50G	60k, 200k, 8M

B.5 Small-signal model of the bias-tee

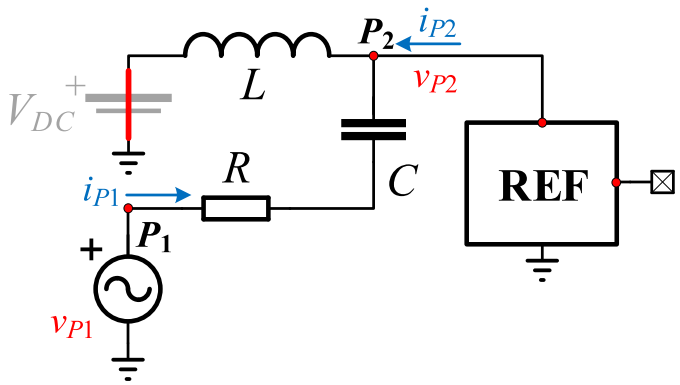


Figure B.12: AC test bench for calculating the small-signal behaviour of the bias-tee network with a 50 Ω RF generator. $V_{DC} = 3.3$ V, $R = 50$ Ω, $L = 430$ µH, $C = 6.8$ nF.

The bias-tee is a linear 2-port block, and its small-signal transfer functions are derived analytically using the AC test bench shown in Fig.B.12. The DC voltage source is shorted to ground for the small-signal analysis, port P_1 is connected to the voltage source of the RF generator that defines the RF open circuit voltage v_{P1}, and port P_2 is connected to the load circuit that defines the load current i_{P2}. The values of the RLC elements are used as known variables. The RF generator current i_{P1} and the load voltage v_{P2} are defined as functions of v_{P1} and i_{P2} according to Eq. (B.20):

$$\begin{aligned} i_{P1} &= i_{P1}\left(v_{P1}, i_{P2}\right) \\ v_{P2} &= v_{P2}\left(v_{P1}, i_{P2}\right) \end{aligned} \tag{B.20}$$

Eq. (B.21) presents the linearized form of these relationships in the small-signal conditions around the operating point Q:

$$\begin{aligned} i_{p1} &= \left.\frac{\partial i_{P1}}{\partial v_{P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial i_{P1}}{\partial i_{P2}}\right|_Q \cdot i_{p2} = BT_{11} \cdot v_{p1} + BT_{12} \cdot i_{p2} \\ v_{p2} &= \left.\frac{\partial v_{P2}}{\partial v_{P1}}\right|_Q \cdot v_{p1} + \left.\frac{\partial v_{P2}}{\partial i_{P2}}\right|_Q \cdot i_{p2} = BT_{21} \cdot v_{p1} + BT_{22} \cdot i_{p2} \end{aligned} \tag{B.21}$$

The four partial derivatives are labelled as $BT_{ij}(s)$, and their analytical expressions are obtained by setting one of the independent variables to zero, as shown in Eq. (B.22):

$$
\begin{aligned}
BT_{11}(s) &= \left.\frac{\partial i_{P1}}{\partial v_{P1}}\right|_Q = \left.\frac{i_{p1}}{v_{p1}}\right|_{i_{p2}=0} = \frac{sC}{1+sRC+s^2LC} \\
BT_{21}(s) &= \left.\frac{\partial v_{P2}}{\partial v_{P1}}\right|_Q = \left.\frac{v_{p2}}{v_{p1}}\right|_{i_{p2}=0} = \frac{s^2LC}{1+sRC+s^2LC} \\
BT_{12}(s) &= \left.\frac{\partial i_{P1}}{\partial i_{P2}}\right|_Q = \left.\frac{i_{p1}}{i_{p2}}\right|_{v_{p1}=0} = \frac{-s^2LC}{1+sRC+s^2LC} \\
BT_{22}(s) &= \left.\frac{\partial v_{P2}}{\partial i_{P2}}\right|_Q = \left.\frac{v_{p2}}{i_{p2}}\right|_{v_{p1}=0} = \frac{sL\cdot(1+sRC)}{1+sRC+s^2LC}
\end{aligned}
\tag{B.22}
$$

The values of the low-frequency gain G, zeroes z_j, and poles p_i are summarized in TableB.12, and Fig.B.13shows the frequency responses $BT_{ij}(\jmath\omega)$ of the bias-tee obtained using PSS simulations that are compared to the analytical expressions for the bias-tee transfer functions $BT_{ij}(s)$ evaluated at $s = \jmath\omega$.

Table B.12: The low-frequency gain G, zeroes z_j, and poles p_i of the transfer functions $BT_{ij}(s)$ of the bias-tee with a 50 Ω RF generator.

$F(s)$	G	z_j [Hz]	p_i [Hz]
$BT_{11}(s) = \left.\frac{\partial i_{P1}}{\partial v_{P1}}\right\|_Q$	$6.800{\cdot}10^{-9}$	0	9.25k ± ȷ92.6k
$BT_{21}(s) = \left.\frac{\partial v_{P2}}{\partial v_{P1}}\right\|_Q$	$2.924{\cdot}10^{-12}$	0, 0	9.25k ± ȷ92.6k
$BT_{12}(s) = \left.\frac{\partial i_{P1}}{\partial i_{P2}}\right\|_Q$	$-2.924{\cdot}10^{-12}$	0, 0	9.25k ± ȷ92.6k
$BT_{22}(s) = \left.\frac{\partial v_{P2}}{\partial i_{P2}}\right\|_Q$	$4.300{\cdot}10^{-4}$	0, 468.1k	9.25k ± ȷ92.6k

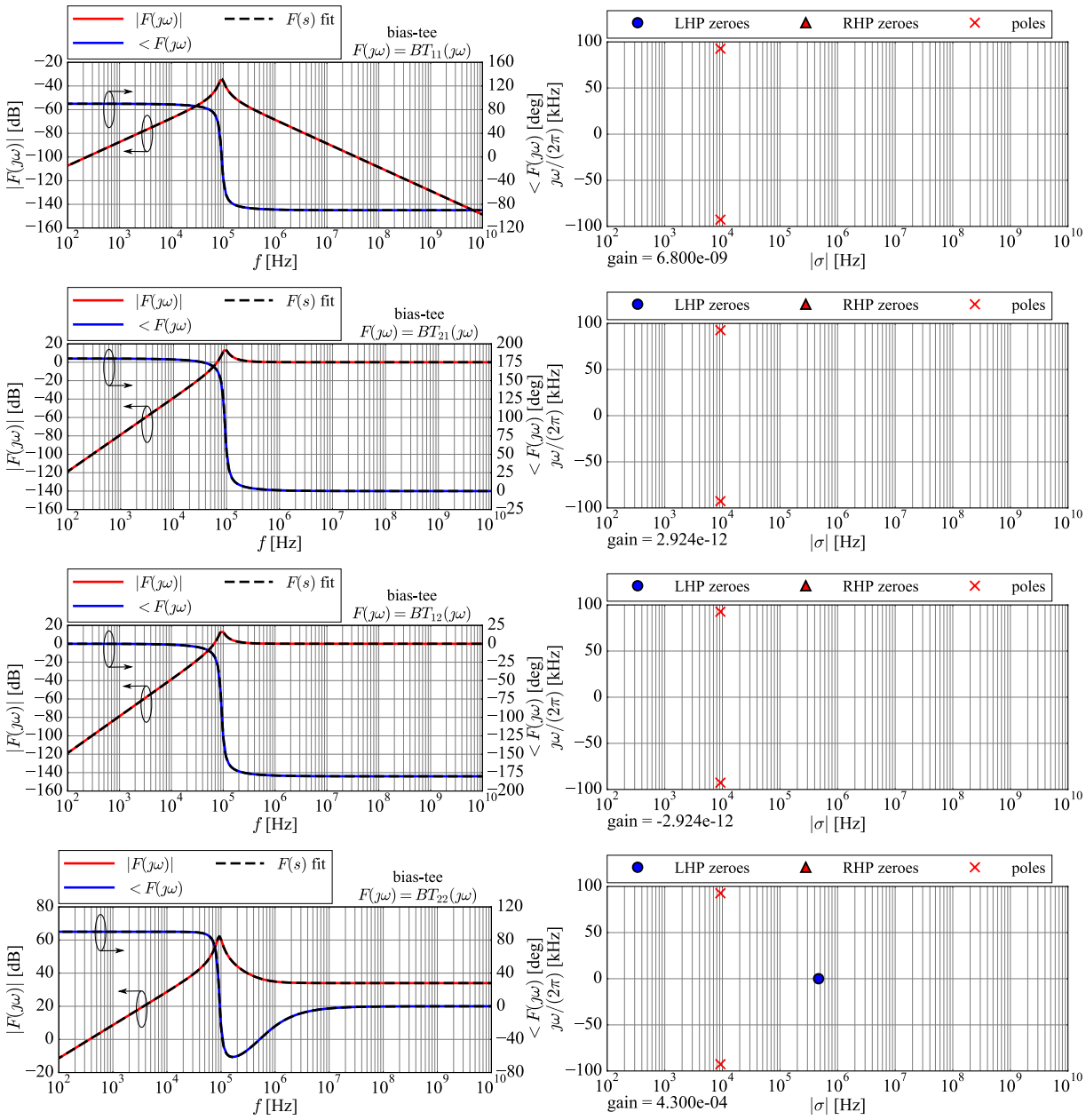


Figure B.13: Frequency responses $BT_{ij}(j\omega)$ of the bias-tee with a 50-Ω RF generator (solid lines), with the associated transfer functions $BT_{ij}(s)$ in the s-domain, where $s = 2\pi\sigma \pm j\omega$.

B.6 Small-signal model of the top-level test bench

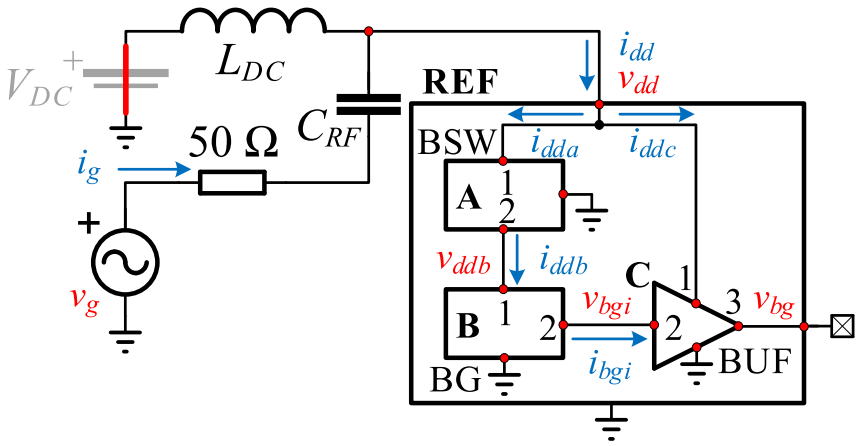


Figure B.14: AC test bench for simulating the small-signal behaviour of the top-level test bench. $V_{DC} = 3.3$ V, $L = 430$ µH, $C = 6.8$ nF.

The small-signal behaviour of the top-level test bench in Fig.B.14around the DC operating point Q is defined by substituting the perturbations of the top-level voltages and currents into the linearized block-level expressions given in Eqs. (B.3), (B.5), (B.19), (B.21). For each block, the small-signal currents that flow outwards from the block are substituted with the negative sign. The resulting expressions are given in Eq. (B.23):

$$\begin{aligned}
i_g &= D_{11} \cdot v_g - D_{12} \cdot i_{dd} & i_{ddb} &= B_{11} \cdot v_{ddb} - B_{12} \cdot i_{bgi} \\
v_{dd} &= D_{21} \cdot v_g - D_{22} \cdot i_{dd} & v_{bgi} &= B_{21} \cdot v_{ddb} - B_{22} \cdot i_{bgi} \\
i_{dd} &= i_{dda} + i_{ddc} & i_{ddc} &= C_{11} \cdot v_{dd} + C_{12} \cdot v_{bgi} \\
i_{dda} &= A_{11} \cdot v_{dd} - A_{12} \cdot i_{ddb} & i_{bgi} &= C_{21} \cdot v_{dd} + C_{22} \cdot v_{bgi} \\
v_{ddb} &= A_{21} \cdot v_{dd} - A_{22} \cdot i_{ddb} & v_{bg} &= C_{31} \cdot v_{dd} + C_{32} \cdot v_{bgi}
\end{aligned} \tag{B.23}$$

where for brevity, the bulk switch transfer functions BSW_{ij} are marked as A_{ij}, the bandgap transfer functions BG_{ij} are marked as B_{ij}, the output buffer transfer functions BUF_{ij} are marked as C_{ij}, and the bias-tee transfer functions BT_{ij} are marked as D_{ij}. The supply current perturbations i_{dd_bsw}, i_{dd_bg}, and i_{dd_buf} are marked as i_{dda}, i_{ddb}, and i_{ddc}. The bandgap output voltage perturbation v_{bg_int} and the buffer input current perturbation i_{bg_int} are marked as v_{bgi} and i_{bgi}.

This system of ten equations in ten unknowns is solved as follows. In the first step, the perturbation voltage v_{dd} is considered as an independent variable, and the expressions for the perturbation signals v_{ddb}, i_{ddb}, v_{bgi}, and i_{bgi} form a closed system of four equations in four unknowns, with the solution given in Eq. (B.24):

$$\begin{aligned} v_{ddb} \cdot f_1 &= A_{21} f_2 \cdot v_{dd} & v_{bgi} \cdot f_1 f_2 &= f_4 \cdot v_{dd} \\ i_{bgi} \cdot f_1 &= C_{21} f_3 \cdot v_{dd} & i_{ddb} \cdot f_1 f_3 &= f_5 \cdot v_{dd} \end{aligned} \tag{B.24}$$

where f_i are the helper transfer functions defined in Eq. (B.25):

$$\begin{aligned} f_1 &= f_2 f_3 - A_{22} B_{12} B_{21} C_{22} & f_4 &= A_{21} B_{21} f_2 - B_{22} C_{21} f_1 \\ f_2 &= 1 + B_{22} C_{22} & f_5 &= A_{21} B_{11} f_1 - B_{12} C_{21} f_3 \\ f_3 &= 1 + A_{22} B_{11} \end{aligned} \tag{B.25}$$

In the second step, the solutions for perturbation signals i_{dda}, i_{ddc}, v_{bg}, and i_{dd} are obtained by substituting Eq. (B.24) into Eq. (B.23):

$$\begin{aligned} i_{dda} \cdot f_1 f_3 &= f_6 \cdot v_{dd} & v_{bg} \cdot f_1 f_2 &= f_8 \cdot v_{dd} \\ i_{ddc} \cdot f_1 f_2 &= f_7 \cdot v_{dd} & i_{dd} \cdot f_1 f_2 f_3 &= f_9 \cdot v_{dd} \end{aligned} \tag{B.26}$$

where f_i are the additional helper functions defined in Eq. (B.27):

$$\begin{aligned} f_6 &= A_{11} f_1 f_3 - A_{12} f_5 & f_8 &= C_{31} f_1 f_2 + C_{32} f_4 \\ f_7 &= C_{11} f_1 f_2 + C_{12} f_4 & f_9 &= f_2 f_6 + f_3 f_7 \end{aligned} \tag{B.27}$$

In the third step, the expression for i_{dd} in Eq. (B.26) is substituted into Eq. (B.23) to find the closed-form solution for the perturbation voltage v_{dd} and the perturbation of the RF generator current i_g as a function of the independent perturbation voltage v_g of the RF generator, given in Eq. (B.28):

$$\begin{aligned} v_{dd} \cdot f_{10} &= D_{21} f_1 f_2 f_3 \cdot v_g \\ i_g \cdot f_{10} &= f_{11} \cdot v_g \end{aligned} \tag{B.28}$$

where the additional helper functions f_i are defined in Eq. (B.29):

$$\begin{aligned} f_{10} &= f_1 f_2 f_3 + D_{22} f_9 \\ f_{11} &= D_{11} f_{10} - D_{12} D_{21} f_9 \end{aligned} \tag{B.29}$$

In the final step, the closed-form solution for v_{dd} in Eq. (B.28) is substituted into

Eqs. (B.24), (B.26) to obtain the closed-form solutions for all perturbation signals in the top-level test bench as a function of the independent perturbation voltage v_g of the RF generator, given in Eq. (B.30):

$$\begin{aligned}
i_g \cdot f_{10} &= f_{11} \cdot v_g \\
v_{dd} \cdot f_{10} &= D_{21} f_1 f_2 f_3 \cdot v_g \\
i_{dd} \cdot f_{10} &= D_{21} f_9 \cdot v_g \\
i_{dda} \cdot f_{10} &= D_{21} f_2 f_6 \cdot v_g \\
v_{ddb} \cdot f_{10} &= A_{21} D_{21} f_2^2 f_3 \cdot v_g \\
i_{ddb} \cdot f_{10} &= D_{21} f_2 f_5 \cdot v_g \\
v_{bgi} \cdot f_{10} &= D_{21} f_3 f_4 \cdot v_g \\
i_{ddc} \cdot f_{10} &= D_{21} f_3 f_7 \cdot v_g \\
i_{bgi} \cdot f_{10} &= C_{21} D_{21} f_2 f_3^2 \cdot v_g \\
v_{bg} \cdot f_{10} &= D_{21} f_3 f_8 \cdot v_g
\end{aligned} \tag{B.30}$$

The closed-form solutions in Eq. (B.30) enable calculating the poles and zeroes of each perturbation signal in the top-level test bench analytically based on the known transfer functions A_{ij}, B_{ij}, C_{ij}, D_{ij} of each sub-block, in any combination of transistor-level blocks and behavioural models, using the methodology presented in SectionB.3.

Appendix C

Simulations of the DPI injection into the output pin of an amplifier

One particular effect of the nonlinear output impedance shown in [65] is investigated from an EMC perspective. The DPI performance of an operational amplifier (op-amp) in the non-inverting configuration is evaluated by injecting the RF disturbance into the output pin, while the input pin is driven by a low-frequency functional signal. The RF-induced DC-shift of the output voltage is observed as the failure criterion of the DPI test.

It is shown in [65] that the output impedance of the amplifier, i.e. the output reflection coefficient, depends on the initial phase of the signal applied to the output under certain conditions of the large-signal drive at the amplifier input. Since in general the initial phase of the RF generator is not controlled in the DPI measurement setup, and the output impedance determines the RF power delivered to the circuit under test, there exists a possibility of random (spurious) changes in the measured DPI characteristic that may cause measurement repeatability problems.

The chapter is organized as follows. SectionC.1presents the methodology for calculating the output reflection coefficient using TRAN simulations. SectionC.2presents the functional simulation results of the op-amp, including the open- and closed-loop frequency response, the large-signal parameters, and the output reflection coefficient simulations. The influence of the phase relationship between the RF disturbance and the functional signal on the output reflection coefficient is presented in SectionC.3, and the influence on the simulated DPI characteristics is given in SectionC.4. The results are discussed in SectionC.5. The research from this chapter is presented in [35].

C.1 Output reflection coefficient in the time-domain

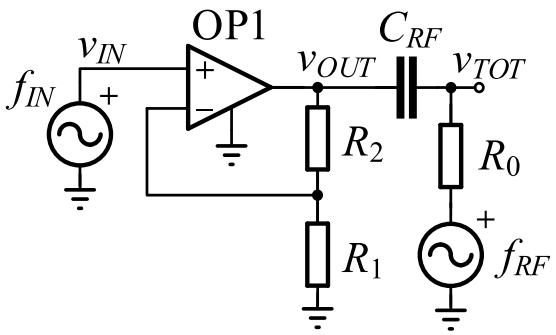


Figure C.1: Testbench for DPI simulations of the modelled amplifier with RF disturbance applied to the output pin [35].

The testbench for the DPI simulations is shown in Fig.C.1. The op-amp is connected in the non-inverting configuration with low-frequency gain of 20 dB using the feedback network defined by $R_1 = 1$ MΩ and $R_2 = 9$ MΩ. The RF disturbance is injected into the output pin of the amplifier through the decoupling capacitor $C_{RF} = 6.8$ nF. Two nodes are observed: the amplifier output node v_{OUT} and the RF generator output node v_{TOT}. The output impedance of the amplifier is observed in the node v_{TOT} because this is the relevant node that loads the RF generator. The output reflection coefficient Γ_{out} seen from the node v_{TOT} looking into the amplifier is defined as:

$$\Gamma_{out}(f) = \frac{V_{refl}(f)}{V_{fwd}(f)} \tag{C.1}$$

where $V_{fwd}(f)$ is the forward voltage wave at the frequency f applied to the node v_{TOT}, and $V_{refl}(f)$ is the voltage wave at the frequency f reflected from the node v_{TOT} in Fig.C.1. In case of linear circuits the reflected voltage wave $v_{REFL}(t)$ contains only the forward voltage wave frequency f_{RF}, therefore Γ_{out} becomes equivalent to the parameter S_{22}. The total voltage at the output node of the amplifier is equal to:

$$V_{tot}(f) = V_{fwd}(f) + V_{refl}(f) + V_{func}(f) \tag{C.2}$$

The component $v_{FUNC}(f)$ is the contribution of the functional input signal.

In the case of nonlinear circuits, the reflected voltage wave $v_{REFL}(t)$ contains not only the forward voltage wave frequency f_{RF}, but also its mixing products with the functional input frequency f_{IN}. In order to include all nonlinear effects into the circuit simulation, the circuit is simulated in the time-domain. Eq. (C.2) is therefore converted into the time-domain:

$$v_{TOT}(t) = v_{FWD}(t) + v_{REFL}(t) + v_{FUNC}(t) \tag{C.3}$$

The total voltage $v_{TOT}(t)$ is obtained by simulating the testbench in Fig.C.1in the time-domain. The forward voltage wave $v_{FWD}(t)$ is determined by separately simulating the RF generator driving an ideal 50 Ω load. The contribution $v_{FUNC}(t)$ of the functional input signal $v_{IN}(t)$ is obtained by simulating the circuit in Fig.C.1with the RF disturbance turned off. Eq. (C.3) is used to calculate the reflected voltage wave $v_{REFL}(t)$ in the time-domain. The forward and reflected frequency components at the fundamental RF frequency $V_{fwd}(f_{RF})$ and $V_{refl}(f_{RF})$ are obtained by applying the fast Fourier transform (FFT) on the time-domain signals:

$$\begin{aligned} V_{refl}(f_{RF}) &= FFT\left\{v_{REFL}(t)\right\}|_{f=f_{RF}} \\ V_{fwd}(f_{RF}) &= FFT\left\{v_{FWD}(t)\right\}|_{f=f_{RF}} \end{aligned} \tag{C.4}$$

The output reflection coefficient Γ_{out} is calculated as the ratio of these values, as it is defined in Eq. (C.1). This definition of Γ_{out} is consistent with the definition of the X-parameters given in [65].

Since the total voltage $v_{TOT}(t)$ contains the mixing products of the two fundamental frequencies f_{IN} and f_{RF}, the fundamental period of the resulting periodic waveform is defined by the "beat" frequency f_B. The beat frequency is the greatest number that divides both fundamental tones, i.e. their greatest common divisor (GCD) [73]. The value of the beat frequency is numerically sensitive: for example GCD(1.53 MHz, 1 GHz) = 10 kHz, however GCD(1.5322 MHz, 1 GHz) = 200 Hz. Since the FFT of the time-domain signal can be properly determined only if at least a single full period of the signal is known, low values of the beat frequency increase the required simulated time. In the presented test case the RF disturbance frequency are chosen such that the resulting beat frequency is never below $f_B = 10$ kHz.

C.2 Functional simulations

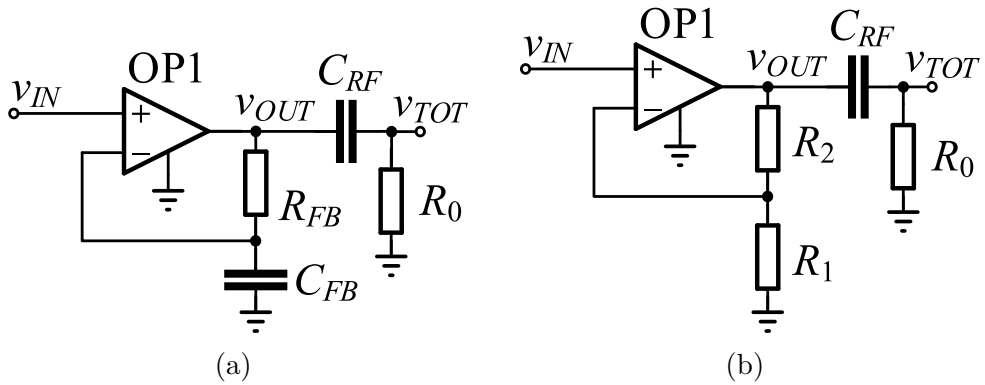


Figure C.2: Testbench for functional simulations: (a) open loop with DC operating point, (b) closed loop with 20 dB gain. Figure published in [35].

The testbenches for functional simulations of the amplifier under test are shown in Fig.C.2. The open loop AC characteristic is obtained by simulating the schematic shown in Fig.C.2a. The RC filter with a very low cut-off frequency ($R_{RB} = 100$ MΩ, $C_{FB} = 100$ mF, $f_g = 16$ nHz) ensures unity gain feedback in the DC conditions, and open loop operation in AC conditions. In both schematics in Fig.C.2the amplifier is loaded by the network used to inject the RF disturbance into the output pin, consisting of the decoupling capacitor $C_{RF} = 6.8$ nF and the input resistance of the RF generator $R_0 = 50$ Ω.

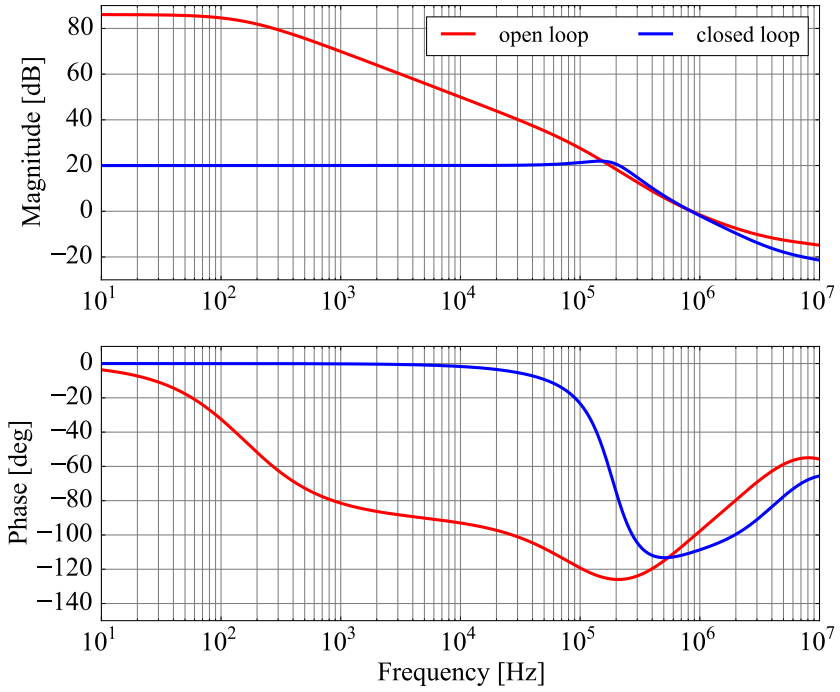
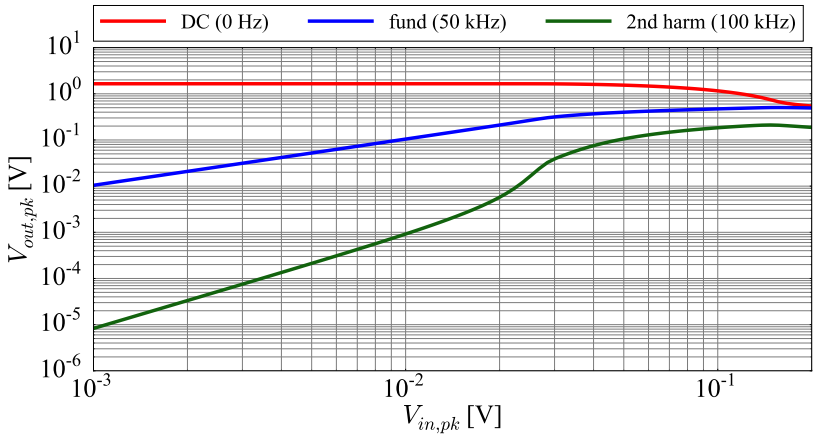


Figure C.3: AC characteristic of the amplifier in open and closed loop [35].

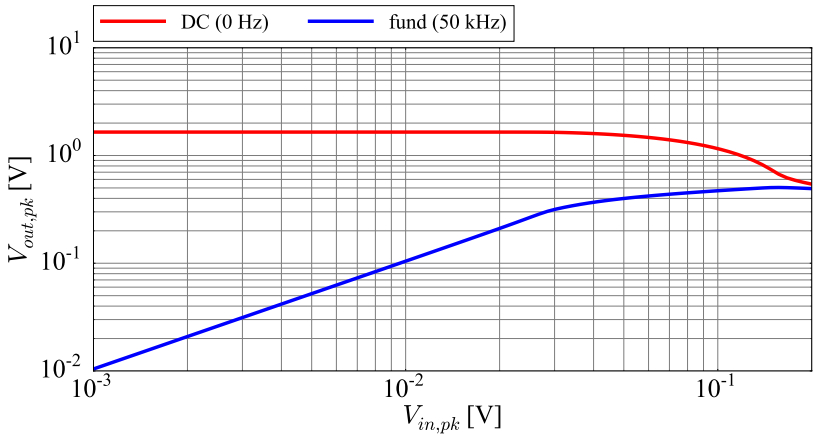
Table C.1: Functional parameters of the op-amp [35].

quantity	open loop	closed loop
A_{V0}	86 dB	20 dB
$f_{-3\text{dB}}$	160 Hz	263 kHz
GBW	3.2 MHz	2.63 MHz
f_{UG}	850 kHz	850 kHz
PM	78°	69°

The open loop and closed loop AC transfer functions of the amplifier are shown in Fig.C.3. The low frequency gain of the open loop amplifier is equal to $A_{V0} = 86$ dB and the -3 dB bandwidth (the dominant pole) is $f_{-3\text{dB}} = 160$ Hz. The gain-bandwidth product is equal to $GBW = 3.2$ MHz. The functional AC specifications of the op-amp are summarized in TableC.1. The phase margin of approximately 70 ° ensures that there is no significant resonance in the closed-loop AC transfer function.



(a)



(b)

Figure C.4: Large signal behaviour of the amplifier at $f_{IN} = 50$ kHz. (a) First three frequency components of $v_{OUT}(t)$, (b) close-up of the DC and fundamental component [35].

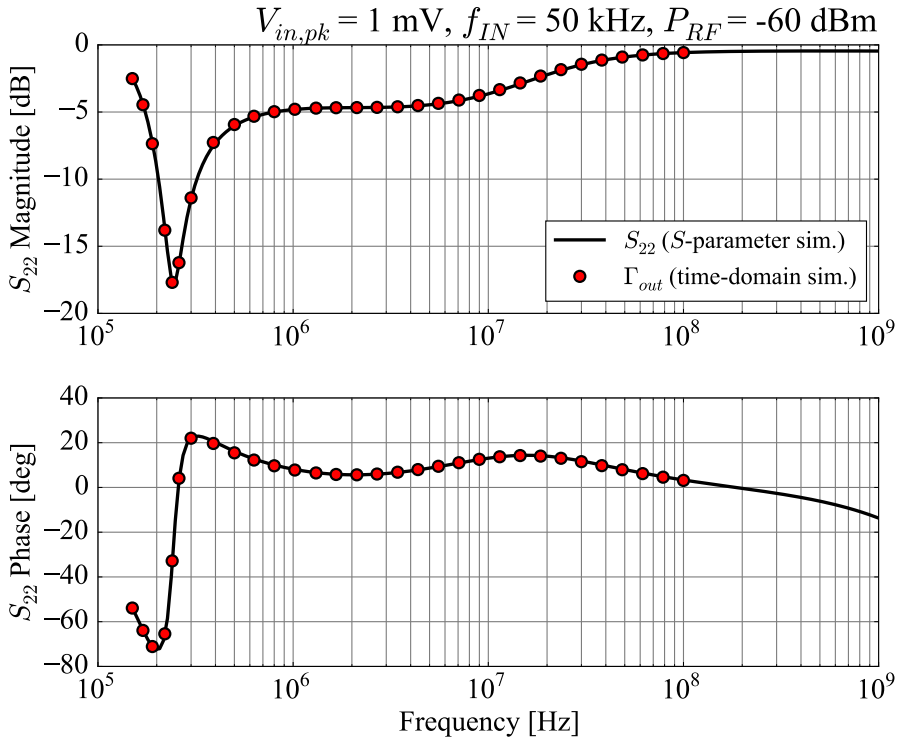


Figure C.5: Verification of the method for obtaining Γ_{out} using time-domain simulations in the linear region of the amplifier [35].

The large-signal behaviour of the modelled amplifier is shown in Fig.C.4via the constant frequency sweep. The amplitude of the functional input signal v_{IN} is swept from 1 mV to 200 mV with the constant functional input signal frequency of $f_{IN} = 50$ kHz. This value is within the amplifier bandwidth and it is used in the remainder of this paper. The amplifier exhibits compression behaviour at input amplitudes $V_{in,pk}$ above 30 mV. The gain of the second harmonic (at 100 kHz) increases by 2 dB/dB in the linear region and enters the compression region at input amplitudes $V_{in,pk}$ above 20 mV. For $V_{in,pk} = 1$ mV the amplifier behaves linearly, with harmonic distortion below -60 dB.

In order to verify the method for calculating the output reflection coefficient Γ_{out} from time-domain simulations presented in SectionC.1, Γ_{out} is compared with the standard small-signal simulation of the parameter S_{22} in the linear region of operation by setting a very small amplitude $V_{in,pk} = 1$ mV. The comparison is shown in Fig.C.5. The simulated time in the time-domain simulations is fixed to 130 µs, which is empirically sufficient for the voltage $v_{TOT}(t)$ to reach the steady-state. The presented simulation results of Γ_{out} are in the frequency range from 150 kHz to 100 MHz due to the high time and memory requirements for the time-domain simulations of the higher RF frequencies.

C.3 Influence of RF phase on the output reflection coefficient

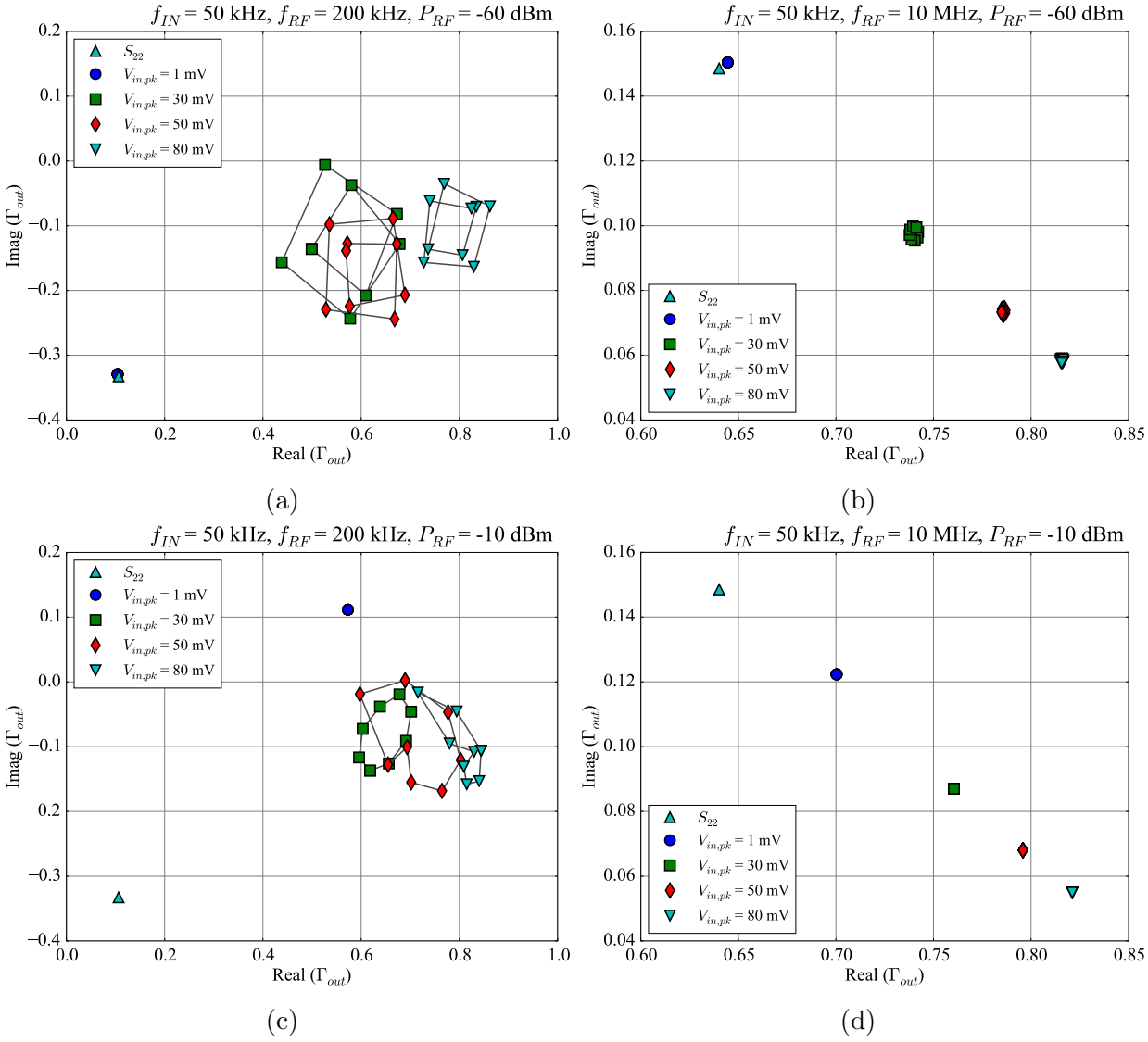


Figure C.6: Output reflection coefficient Γ_{out} as a function of the input functional signal amplitude $V_{in,pk}$ and RF disturbance initial phase θ_{RF} swept in steps of 45° at f_{RF} = 200 kHz and f_{RF} = 10 MHz [35].

The output reflection coefficient Γ_{out} is plotted as a function of varying input signal amplitude $V_{in,pk}$ and varying initial phase of the RF disturbance θ_{RF} in Fig.C.6, at the RF disturbance frequencies f_{RF} of 200 kHz and 10 MHz, and at the RF forward power levels P_{RF} of -60 dBm and -10 dBm.

At f_{RF} = 200 kHz and the lower value of P_{RF} and $V_{in,pk}$, the value of Γ_{out} corresponds to the small-signal parameter S_{22}. At the higher value of P_{RF}, the value of Γ_{out} changes for all input amplitudes $V_{in,pk}$, including the linear case with $V_{in,pk}$ = 1 mV.

The strong dependence of the output reflection coefficient Γ_{out} on the initial phase θ_{RF} is observed at both RF power levels P_{RF}, but only for the higher input amplitudes $V_{in,pk}$.

At f_{RF} = 10 MHz, the dependence of Γ_{out} on the RF power level and the input amplitude is observed. However, the dependence of Γ_{out} on θ_{RF} is only slightly visible at P_{RF} = -60 dBm, while at P_{RF} = -10 dBm it completely vanishes.

C.4 DPI simulations

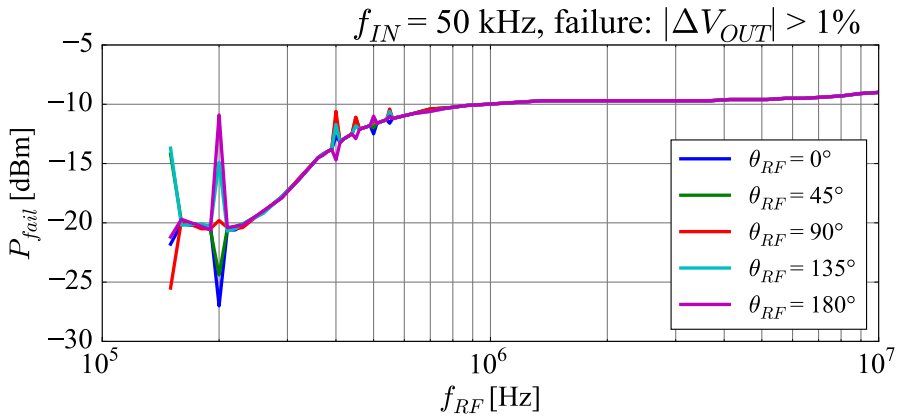


Figure C.7: The simulated DPI characteristic of the amplifier in the nonlinear region with $V_{in,pk}$ = 50 mV, f_{IN} = 50 kHz for several values of the initial RF disturbance phase θ_{RF} [35].

The testbench in Fig.C.1is used to run DPI simulations in the frequency range from 150 kHz to 10 MHz. The simulated DPI characteristic is shown in Fig.C.7. The forward power level P_{fail} at which the circuit functionality fails is plotted as the function of the RF disturbance frequency f_{RF} for several values of the initial RF disturbance phase θ_{RF}. The failure criterion is defined as the DC-shift of the output voltage by more than 1%. The initial phase of the RF signal θ_{RF} is swept from 0° to 180° in steps of 45°. The dependence of the DPI characteristic on the initial RF phase θ_{RF} is visible in harmonic multiples of the functional input frequency f_{IN} = 50 kHz. The maximum deviation caused by the varying RF phase θ_{RF} is equal to 16.1 dB at f_{RF} = 200 kHz.

C.5 Discussion

The method for calculating the output reflection coefficient from the time-domain simulations is confirmed in the linear region of amplifier operation by direct comparison with the small-signal S-parameter simulations. The validity of the approach in the nonlinear region of amplifier operation is demonstrated qualitatively by observing the correlation between the sensitivity of the DPI curve on the RF phase and the sensitivity of the calculated output reflection coefficient on the RF phase in the same RF disturbance conditions.

The output impedance nonlinearity is observed in Fig.C.6in two ways: (i) the output reflection coefficient, i.e. the output impedance, depends both on the RF disturbance forward power and on the functional input signal amplitude; (ii) the output impedance also depends on the initial phase of the RF disturbance in the presented conditions. Since this dependence vanishes for low input amplitudes, regardless of the RF power level, this effect is attributed to the large-signal operating point defined by the functional input signal driving the amplifier into the nonlinear region of operation.

The influence of the RF phase θ_{RF} on the DPI characteristic is a narrow-band effect. It is observed at the harmonic frequencies of the functional input signal, and it diminishes with the order of the harmonic. This behaviour is also observed in Fig.C.6, where the dependence of Γ_{out} on θ_{RF} is negligible at $f_{RF} = 10$ MHz. The DPI standard requires that the RF disturbance signal is not correlated with (i.e. an exact harmonic of) the functional input signal.

However, several scenarios exist where this effect may become visible. One such scenario is the test case reported in our previous paper [37], where the RF disturbance is injected into the power supply of a buffered voltage reference circuit consisting of several circuit blocks, including the output buffer. The RF disturbance is coupled to the output buffer block via two paths: through the functional input signal pin of the buffer connected to the output of the bandgap reference block, and through the supply voltage pin of the buffer. From the point of view of the output buffer block, these are two input signals of different power that occur at the same frequency, which is enough to cause the presented effect on the DPI characteristic. From the point of view of the DPI measurement setup, only one RF generator is used, i.e. no functional signal generator is included in the setup, therefore this simulation/measurement setup is compliant with the DPI standard.

Another scenario where the presented effect may be relevant is the DPI simulation environment. Since the frequency points in the simulation are often chosen from the set of "round" numbers, not being aware of the effect may cause seemingly random "glitches" at isolated frequencies.

Appendix D

Determining discrete-time system poles

The research from this chapter is presented in [42].

D.1 The Cauchy integral

In order to obtain the root locus of an ESN model in a given testbench, it is necessary to determine the open-loop poles of the ESN, and of the transfer function $\mathbf{G_{FB}}(z)$ that describes the outside circuit. The presented methodology is derived for a rational discrete-time system S defined by N poles p_k and M zeros q_l:

$$S... \;\; f_S(z) = G \cdot \frac{\prod_{l=0}^{M}(z - q_l)}{\prod_{k=0}^{N}(z - p_k)}, \;\; z \in \mathbb{C} \tag{D.1}$$

The discrete-time system S is stable if and only if all poles p_k are located within the unit circle in the complex z-plane. All poles of real discrete-time systems are either real-valued or come in complex-conjugate pairs. The frequency response of the discrete-time system S is equal to $f_S(e^{\jmath\Omega})$, $z = e^{\jmath\Omega}$, where $\Omega = \omega T_s$ is the discrete-time radial frequency in rad/sample, and T_s is the uniform sampling time [52].

The Cauchy integral formula (CIF) is given in Eq. (D.2). The CIF is used in [43] to find the transfer function from the given frequency response of continuous-time systems:

$$f\left(a\right) = \frac{1}{2\pi\jmath} \oint_{l} \frac{f\left(z\right)}{z - a} \, \mathrm{d}z \tag{D.2}$$

where $f(z)$ is a complex-valued function that is analytic (differentiable) in the region in the complex plane that contains the point $a \in \mathbb{C}$ bounded by the closed curve l. In this work, the CIF is applied to the discrete-time transfer function $f_S(z)$ in Eq. (D.1), which is analytic in the entire z-plane except in the poles p_k, where its value is not defined.

A series of N helper functions $\hat{f}_k(z)$ is defined to cancel out each term $(z - p_k)$ from the transfer function $f_S(z)$:

$$\hat{f}_k\left(z\right) = f_S\left(z\right) \cdot \left(z - p_k\right), \, k = 1, ..., N \tag{D.3}$$

Each function $\hat{f}_k(p_k)$ is analytic in the pole p_k. It should be noted that this framework does not apply to discrete-time systems with multiple poles in the same point in the z-plane. Based on Eqs. (D.2) and (D.3) the following expression is derived:

$$I = \frac{1}{2\pi\jmath} \oint_c f_S\left(z\right) \, \mathrm{d}z = \sum_{k=1}^{N} \hat{f}_k\left(p_k\right), \;\; c... \, z = e^{\jmath\Omega} \tag{D.4}$$

where c is the unit circle in the complex z-plane. The integral I on the left-hand side of Eq. (D.4) is real-valued for real systems. The integral I is calculated over the unit circle $c... \, z = e^{\jmath\Omega}$, therefore its value is obtained from the frequency response $f_S(e^{\jmath\Omega})$:

$$I = \frac{1}{2\pi} \int_0^{2\pi} f_S\left(e^{\jmath\Omega}\right) e^{\jmath\Omega} \, \mathrm{d}\Omega \tag{D.5}$$

The right-hand side sum in Eq. (D.4) is defined by the helper functions $\hat{f}_k$ evaluated in the poles p_k. The values of the poles do not enter the equation directly, therefore the equation is extended with the additional term z^n:

$$\begin{aligned} I_n = \frac{1}{2\pi\jmath} \oint_c f_S\left(z\right) z^n \, \mathrm{d}z = \sum_{k=1}^{N} p_k^n \cdot \hat{f}_k\left(p_k\right) \\ c... \, z = e^{\jmath\Omega}, n \in \mathbb{N}_0 \end{aligned} \tag{D.6}$$

The right-hand side sum in Eq. (D.6) depends also on the values of the poles p_k raised to the power n. The left-hand side integral I_n is a function of the power n, and its value is expressed using the frequency response $f_S(e^{\jmath\Omega})$:

$$\begin{aligned} I_n &= \frac{1}{2\pi} \int_0^{2\pi} f_S\left(e^{\jmath\Omega}\right) e^{\jmath\Omega(n+1)} \, \mathrm{d}\Omega \\ &= \mathrm{IDTFT}\left\{ f_S\left(e^{\jmath\Omega}\right) \right\} |_{k=n+1} = y_{IR}\left[n+1\right] \end{aligned} \tag{D.7}$$

The right-hand side expression in Eq. (D.7) is the inverse discrete-time Fourier transform (IDTFT) of the frequency response $f_S(e^{\jmath\Omega})$, linking the value of the integral I_n to the discrete-time impulse response $y_{IR}\left[k\right]$.

D.2 Pole optimization problem

Eqs. (D.6) and (D.7) form the basis for finding the open-loop poles of an unknown discrete-time system S because they relate the poles p_k to the frequency response $f_S(e^{\jmath\Omega})$ and the impulse response $y_{IR}[k]$, both of which can be obtained by running the system S in the discrete-time domain.

Since Eq. (D.6) holds for all $n \in \mathbb{N}_0$, an arbitrary number of equations M can be defined, with the N poles p_k as the unknowns weighted by N unknown complex-valued coefficients $\hat{f}_k(p_k)$. An overdetermined system of $M > 2N$ equations defines the optimization problem in the complex z-plane in the variables p_k and $\hat{f}_k(p_k)$:

$$\begin{aligned}
\min_x \sum_{n=0}^{M} \left\| I_n - \sum_{k=1}^{N} p_k^n \cdot b_k \right\|_2 \\
x &= \Big[(r_k), (\hat{r}_k), (R_k), (\hat{R}_k), (\varphi_k), (\hat{\varphi}_k)\Big] \\
p_k &= r_k, \;\; k = 1, ..., N_r \\
b_k &= \hat{r}_k, \;\; k = 1, ..., N_r \\
p_{N_r+k} &= R_k \angle \varphi_k, k = 1, ..., N_c \\
b_{N_r+k} &= \hat{R}_k \angle \hat{\varphi}_k, \;\; k = 1, ..., N_c \\
p_{N_r+N_c+k} &= R_k \angle -\varphi_k, \;\; k = 1, ..., N_c \\
b_{N_r+N_c+k} &= \hat{R}_k \angle -\hat{\varphi}_k, \;\; k = 1, ..., N_c
\end{aligned} \tag{D.8}$$

The total number of poles N is considered to be a known design variable. The poles p_k are divided into two groups: N_r real-valued poles and N_c complex-conjugate pole pairs, giving a total number of $N = N_r + 2N_c$ poles. The optimization variable x is a vector of length $2N$:

- N_r real-valued poles:
  $r_k \in (-1, 1), \;\; k = 1, ..., N_r$
- N_c magnitudes of the complex-conjugate pole pairs:
  $R_k \in (0, 1), \;\; k = 1, ..., N_c$
- N_c phases of the complex-conjugate pole pairs:
  $\varphi_k \in (0, \pi), \;\; k = 1, ..., N_c$
- N_r real-valued coefficients:
  $\hat{r}_k \in \mathbb{R}, \;\; k = 1, ..., N_r$
- N_c magnitudes of the complex-conjugate coefficient pairs: $\hat{R}_k \in \mathbb{R}^+, \;\; k = 1, ..., N_c$
- N_c phases of the complex-conjugate coefficient pairs:
  $\hat{\varphi}_k \in (-\pi, \pi), \;\; k = 1, ..., N_c$

Since the number of real-valued poles N_r is not known in advance, the optimization problem is solved for all possible values of N_r for a given N, and the solution with the lowest error is chosen. E.g. for $N = 5$ poles, the possible values of N_r are 1, 3 or 5 because the number of remaining poles that are divided into N_c complex-conjugate pairs has to be an even number. Once the poles p_k are known, the value of the transfer function $f_S(z)$ can be determined in all points a within the unit circle using Eq. (D.2) and the analytic function $\bar{f}_S(z)$:

$$\bar{f}_S(z) = f_S(z) \cdot \prod_{k=1}^{N} (z - p_k) \tag{D.9}$$

The line integral in Eq. (D.2) is calculated over the unit circle $c... z = e^{\jmath\Omega}$ from the known frequency response $f_S(e^{\jmath\Omega})$ using the Eq. (D.10), which is obtained by substituting Eq. (D.9) into Eq. (D.2):

$$f_S(a) = \frac{1}{\prod_{k=1}^{N} (a - p_k)} \int_0^{2\pi} f_S\left(e^{\jmath\Omega}\right) \frac{\prod_{k=1}^{N} \left(e^{\jmath\Omega} - p_k\right)}{e^{\jmath\Omega} - a} e^{\jmath\Omega} \, \mathrm{d}\Omega \tag{D.10}$$

$$\forall a \in \mathbb{C},\ |a| < 1$$

Once the transfer function $f_S(z)$ is known within the unit circle in the complex z-plane, the zeroes q_l both inside and outside the unit circle can be found by fitting Eq. (D.1) to the known transfer function values within the unit circle.

D.3 Test case: second-order bandpass filter

A second-order bandpass filter S_1 is used as a well-defined analytical test case for verifying the mathematical relations introduced in SectionD.1. The second-order filter is designed with the central passband frequency of 1 rad/s and the damping factor 0.707, and it is transferred from the s-domain to the z-domain using the zero-order hold (ZOH) discretization method [52]. The sampling time $T_s = 10$ µs is chosen. The z-domain poles, zeroes and proportional gain of the second-order discrete-time system S_1 are:

- poles: $p_{1,2} = 0.99292905 \pm 0.00702119\jmath$
- zeroes: $q_1 = 1$
- proportional gain: $G = 14.0424 \cdot 10^{-3}$

The frequency response of the difference equation defining the filter in discrete-time is derived from the known transfer function $f_{S1}(z)$. The goal of this test case is to find the values of the system poles using only the discrete-time domain behaviour of the filter.

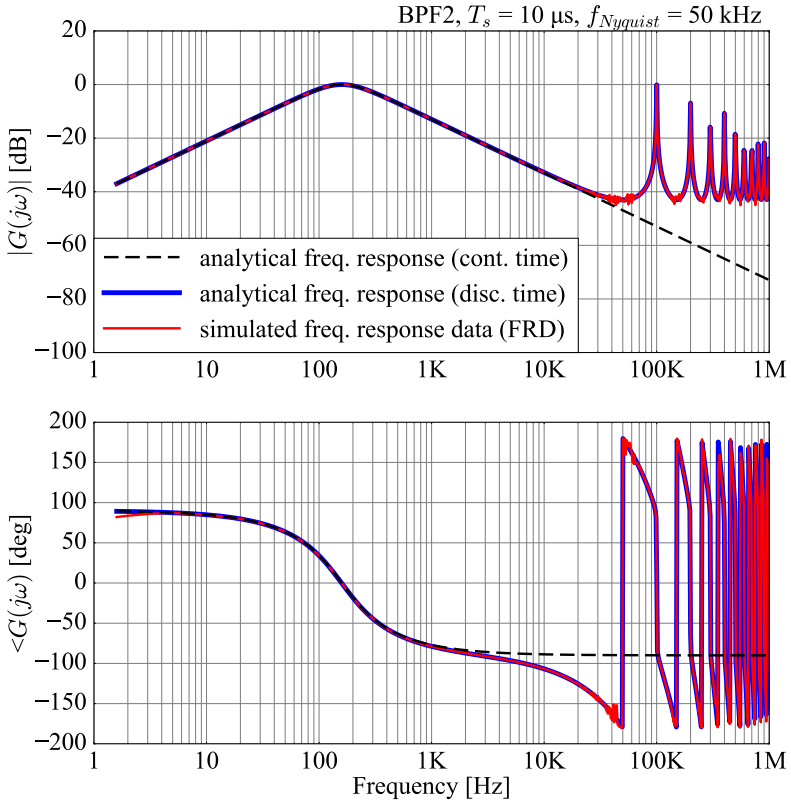


Figure D.1: Frequency response data (FRD) of the second-order bandpass filter compared to the analytically calculated frequency response of the discrete-time and continuous-time versions of the filter [42].

The frequency response $f_{S1}(e^{j\Omega})$ is determined by driving the filter S_1 in the discrete-time domain by sinewaves of varying frequency and observing the amplitude and phase relationship between the resulting output signal and the driving signal. The obtained frequency response data (FRD) is analogous to the continuous-time FRD introduced in [43]. Fig.D.1shows the comparison of the FRD to the analytically calculated frequency response of the discrete-time filter and its continuous-time counterpart.

The discrete-time frequency response is periodic above the Nyquist frequency of 50 kHz. The FRD is in good agreement with the analytically calculated frequency response up to the Nyquist frequency, where noise is observed. This noise is caused by the number of samples in one sinewave period close to the Nyquist frequency dropping to two or three samples. The Cauchy integral is calculated from the frequency response using Eq. (D.7) and it is shown in Fig.D.2. The obtained result is compared to the analytical expression in Eq. (D.6) using the root mean square error (RMSE) measure. The comparison with the shifted filter impulse response $y_{IR}[n+1]$ based on Eq. (D.7) is also shown.

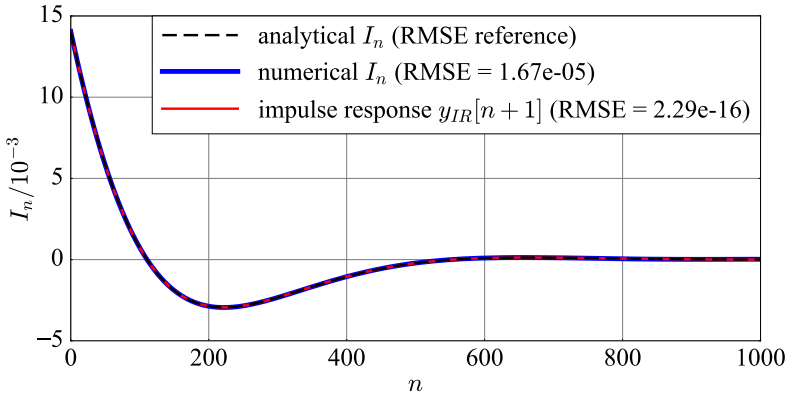


Figure D.2: The Cauchy integral I_n of the second-order bandpass filter compared to the analytically calculated Cauchy integral and the shifted impulse response $y_{IR}[n+1]$ using the root mean square error (RMSE) measure [42].

The optimization problem presented in SectionD.2is solved for the Cauchy integral data of the bandpass filter S_1 using the global optimization method basin-hopping, which is available in the SciPy package in Python [55]. The optimization results are summarized in TableD.1. The number of poles N is set to 2. The possible number of real-valued poles is 0 or 2, and the optimization problem is solved for each case starting from ten random initial conditions for the optimization variable x defined in Eq. (D.8). The solution with the lowest cost function value from the ten optimization runs is chosen for each number of real-valued poles N_r.

Based on the cost function values given in TableD.1, the final solution for the open-loop poles of the system is chosen from the case with no real-valued poles, which corresponds to the presented bandpass filter S_1. The optimization time is in the order of minutes using a workstation with the Intel® Core® i7 CPU @ 3.0 GHz and 12 GB of RAM.

Table D.1: Optimized open-loop poles of the bandpass filter S_1 and the minimized value of the cost function in Eq. (D.8). The number of poles N is set to 2 *a priori* [42].

N	N_r	poles	cost function
2	0	$0.99292965 \pm 0.00701861\jmath$	$6.90{\cdot}10^{-9}$
2	2	0.97526112, 0.97526112	2.88

Biography

Marko Magerl was born in 1990 in Zagreb, Croatia, where he attended the primary and secondary schools. In 2009, he enrolled at the University of Zagreb Faculty of Electrical Engineering and Computing, where he studied electrical engineering with focus on the area of electromagnetic compatibility of integrated circuits under the mentorship of Professor Adrijan Barić, PhD. He obtained his bachelor degree in 2012 with the thesis entitled "Symmetrical two-stage compensated amplifier in 0.35 micrometer technology". He attended the first year of Master studies at KU Leuven, Belgium, a leading European university for the area integrated circuits. He obtained the title of Master of Science in electrical engineering and information technology in 2014 with the diploma thesis entitled "Electrooptical modulator of large amplitude large bandwidth analogue signal". In 2014, he was employed as a doctoral student at the Department of electronics, microelectronics, computer and intelligent systems, where he worked on the research project "Electromagnetic Compatibility Simulation Environment" in collaboration with ams AG, Austria, developing behavioural models of integrated circuits using artificial neural networks with the goal of reducing the model complexity for conducted immunity simulations of integrated circuits. Since 2017, he is employed at ams-OSRAM AG, Austria as a staff engineer for electromagnetic compatibility in the department for research and development.

List of published work

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1. Magerl, M., Čeperić, V., Barić, A., "Echo State Networks for Black-Box Modelling of Integrated Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 35, No. 8, Aug 2016, pp. 1309-1317.
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1. Magerl, M., Stockreiter, C., Eisenberger, O., Minixhofer, R., Barić, A., "Building Interchangeable Black-Box Models of Integrated Circuits for EMC Simulations", 10th Int. Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Edinburgh, United Kingdom, 2015, pp. 258-263.
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3. Magerl, M., Stockreiter, C., Barić, A., "Influence of RF Disturbance Phase on Amplifier DPI Characteristics", Int. Symposium and Exhibition on Electromagnetic Compatibility (EMC Europe), Angers, France, 2017, pp. 1-5.
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3.Magerl, M., Mandić, T., Barić, A., "Broadband characterization of SMA connectors by measurements", 37th Int. Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), Opatija, Croatia, 2014, pp. 104-109.

Životopis

Marko Magerl rođen je 1990. godine u Zagrebu, gdje je pohađao OŠ „dr. Ivan Merz" i XV. gimnaziju. Godine 2009. upisao je Fakultet elektrotehnike i računarstva Sveučilišta u Zagrebu, smjer Elektrotehnika. Pod mentorstvom prof. dr. sc. Adrijana Barića usmjerio se na područje elektromagnetske kompatibilnosti integriranih sklopova radeći na projektima s industrijskim partnerima. Preddiplomski studij završio je 2012. godine završnim radom naslova „Simetrično dvostupanjsko kompenzirano pojačalo u 0,35 mikrometarskoj silicijskoj tehnologiji". Prvu godinu diplomskog studija položio je na KU Leuven, Belgija, vodećem europskom sveučilištu za područje integriranih sklopova. Titulu magistra inženjera elektrotehnike i informacijske tehnologije stekao je 2014. godine diplomskim radom naslova „Elektrooptički modulator širokopojasnog analognog signala velike amplitude". Godine 2014. zapošljava se kao doktorski student pri Zavodu za elektroniku, mikroelektroniku, računalne i inteligentne sustave, gdje provodi istraživački rad na projektu „Electromagnetic Compatibility Simulation Environment" u suradnji s kompanijom ams AG, Austrija, razvijajući ponašajne modele integriranih sklopova temeljene na umjetnim neuronskim mrežama s ciljem smanjivanja kompleksnosti modela radi provođenja simulacija otpornosti integriranih sklopova na vođene smetnje. Od 2017. godine zaposlen je u kompaniji ams-OSRAM AG, Austrija kao inženjer za elektromagnetsku kompatibilnost pri grupi za istraživanje i razvoj.