Radiofrequency power amplifiers in horizontal current bipolar transistor technology

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RADIOFREKVENCIJSKA POJAČALA SNAGE U TEHNOLOGIJI BIPOLARNOGA TRANZISTORA S HORIZONTALNIM TOKOM STRUJE

DOKTORSKI RAD

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Tomislav Suligoj je diplomirao, magistrirao i doktorirao u polju elektrotehnike na Sveučilištu u Zagrebu, Fakultetu elektrotehnike i računarstva (FER), 1995., 1998. odnosno 2001. godine. Trenutno je redoviti profesor na Zavodu za elektroniku, mikroelektroniku, računalne i inteligentne sustave FER-a gdje predaje kolegije u području elektronike i mikroelektronike. Bio je gostujući istraživač na University of California, Los Angeles od 1999. do 2001. godine te na poslijedoktorskom usavršavanju na Hong Kong University of Science and Technology od 2001. do 2002. Dosada je vodio više od 20 projekata financiranih državnih institucija, međunarodnih kompanija i Sveučilišta. Objavio je više od 20 patenata i više od 150 radova u časopisima i zbornicima konferencija u području projektiranja, mjerenja i modeliranja elektroničkih elemenata, mikro- i nano- elektronike, poluvodičke tehnologije i projektiranja integriranih sklopova. Prof. Suligoj dobitnik je 14 nagrada uključujući Državnu nagradu za znanost 2015. g., Zlatnu plaketu na izložbi inovacija ARCA, Best paper award na MIPRO MEET konferenciji, srebrnu plaketu "Josip Lončar" za posebno istaknutu doktorsku disertaciju te Fulbright-ovu stipendije. Član je Technical Program Committee, Publications co-chair i Chairman of Device Physics Subcommittee konferencije IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). Član je Steering Committee konferencije MIPRO MEET. Bio je predsjednik Odjela za elektroničke elemente i poluvodičke integrirane sklopove Hrvatske sekcije IEEE 2010.- 2013. Održao je velik broj pozvanih predavanja na međunarodnim konferencijama, sveučilištima, institutima i kompanijama.

To my wife Ana and son Petar, without whom this would not have been such an exciting adventure.

Abstract

The large-signal performance of the horizontal current bipolar transistor (HCBT) is investigated by extensive measurements and simulations, and its suitability for the radiofrequency power amplifier design is demonstrated by designing advanced high-efficiency and wideband power amplifiers. An accurate and calibrated scalar load-pull setup is firstly employed for the determination of the optimal input and output matching impedances for different HCBT structures to achieve the maximum output power. The HCBT in Class-AB regime at the fundamental frequency of 2.4 GHz provides up to 25 dBm output power with the gain of 11 dB, exhibiting optimal matching impedances close to 50 Ω. The suitability of different collector region designs is investigated by performing load-pull measurements for the HCBTs with uniform, *n*-well, and low-doped collectors, where the low-doped HCBT achieves the highest gain, whereas the *n*-well HCBT provides the highest collector efficiency in the power back-off power range. Due to its robustness in large-signal operation, the HCBT is analyzed in the regime where the load line penetrates the impact ionization region, for the base-emitter bias applied by either a voltage or current source. Additionally, the boundary of linear operation is found for the HCBT by developing a dedicated vector load-pull setup with the possibility of a time-domain waveform measurement in large-signal operation. A high-efficiency Doherty power amplifier is designed using discrete HCBTs at 2.4 GHz, where the amplifier achieves 38.7% collector efficiency with the modulated excitation of 3.5-dB peak to average power ratio. Finally, a wideband balanced amplifier with 700-MHz bandwidth at 2.4 GHz is designed, exhibiting efficiency greater than 35.6% over the bandwidth. The amplifiers provide a performance surpassing that of the most advanced power amplifiers implemented in costlier semiconductor technologies.

Keywords: horizontal current bipolar transistor (HCBT), bipolar transistors, large-signal, scalar load-pull, vector load-pull, waveform measurement, linear operating area, power amplifiers, Doherty, balanced.

Radiofrekvencijska pojačala snage u tehnologiji bipolarnoga tranzistora s horizontalnim tokom struje

Ubrzani rast industrije mobilnih bežičnih komunikacija donosi sve veće brzine prijenosa podataka i proširenje područja primjene bežičnih komunikacija, s ciljem povećanja kvalitete i pouzdanosti komunikacije s bilo kojeg mjesta i u bilo koje vrijeme. Ovaj rast omogućava sklopovlje ekstremnih performansi sa mogućnosti rada na frekvencijama i do nekoliko teraherca. S obzirom da se od sklopovlja bežičnih komunikacija iz generacije u generaciju zahtijeva ogroman rast performansi, tako raste i cijena radiofrekvencijskih (RF) sklopova odgovornih za odašiljanje radiofrekvencijskog signala. Razne poluvodičke tehnologije koriste se za implementaciju ovih sklopova, poput III-V poluvodiča, što uzrokuje rast cijene implementacije u odnosu na CMOS tehnologije, koje se uobičajeno koriste u području digitalne i analogne elektronike. Cilj modernih bežičnih komunikacija su visoke performanse uz nisku potrošnju i, naravno, uz nisku cijenu implementacije. Doktorski rad pod naslovom „*Radiofrequency power amplifiers in horizontal current bipolar transistor technology*“ (Radiofrekvencijska pojačala snage u tehnologiji bipolarnoga tranzistora s horizontalnim tokom struje), predstavlja tehnologiju bipolarnoga tranzistora s horizontalnim tokom struje (HCBT) kao idealnu tehnologiju za implementaciju RF pojačala snage u frekvencijskom području do 6 GHz, uz neznatno višu cijenu u odnosu na komercijalne CMOS procese. Cilj rada je istražiti i demonstrirati složena pojačala snage za bežične komunikacije visokih performansi i niske cijene, koja zadovoljavaju zahtjeve modernih bežičnih komunikacijskih standarda.

Prvo poglavlje „*Introduction*“ daje osvrt na postojeća rješenja i donosi pregled najvažnije teorije bitne za razumijevanje u radu dobivenih rezultata. U prvom dijelu uvodnog poglavlja, dan je pregled najvažnijih bežičnih komunikacijskih standarda, počevši od prve generacije pa sve do pete generacije, čija implementacija je još u tijeku. Tendencija rasta frekvencije nosioca u modernih standarda, opravdana je povećanjem frekvencijskog pojasa modernih moduliranih signala, što omogućava ogroman rast brzine prijenosa podataka. Ovaj rast, nadalje, uzrokuje i rast složenosti radiofrekvencijskog predajnika, čije performanse uvelike određuju performanse cijelog komunikacijskog kanala. Opisana je osnovna arhitektura modernih RF predajnika, a glavne značajke moduliranih signala, kao rezultata rada predajnika, objašnjene su korištenjem simulacija Wi-Fi predajnika na 2.4 GHz. Modulacije, poput frekvencijskog multipleksa ortogonalnih podnosioca (OFDM), prikazane su pomoću konstelacijskih dijagrama, na kojima se promatra i utjecaj nelinearnosti komunikacijskog kanala na poslani, odnosno, primljeni signal. Glavni uzrok nelinearnosti u kanalu najčešće je RF pojačalo snage, čija je glavna uloga pojačati signal uz što manje izobličenje, i uz što nižu potrošnju energije. Blok shema pojačala snage objašnjena je korištenjem analize sklopova pomoću raspršnih parametara u režimu malog signala, a pomoću nelinearnog modela u režimu velikog signala. Glavni pokazatelji perfor-

mansi pojačala snage, poput korisnosti, izlazne snage, pojačanja, i linearnosti, objašnjene su i matematički opisane kako stoji u standardima modernih bežičnih komunikacija. Nadalje, dan je pregled glavnih svojstava RF pojačala snage, poput klasa A, AB, i B, koje predstavljaju osnovni način povećanja korisnosti pojačala. U kontekstu optimizacije rada pojačala snage, dan je opis empirijskog načina utvrđivanja optimalnih radnih uvjeta koristeći mjerni sustav za karakterizaciju tranzistora u režimu velikog signala (eng. *load-pull*). Povećanje korisnosti pojačala snage dobiva se korištenjem naprednih arhitektura, poput Doherty i ET (eng. *Envelope Tracking*), čiji je rad i utjecaj na predani RF signal ukratko opisan u nastavku uvodnog poglavlja. Također, povećanje frekvencijskog pojasa, i time brzine prijenosa podataka, moguće je dobiti korištenjem arhitektura pojačala snage koje za glavnu zadaću imaju optimalni rad na širokom frekvencijskom pojasu, poput *balanced* RF pojačala snage. Povećanje korisnosti i frekvencijskog pojasa, može se dobiti i upotrebom naprednih poluvodičkih tehnologija, gdje su performanse sklopova projektiranih u tim tehnologijama ukratko opisane u nastavku. Na kraju poglavlja, opisana je tehnologija bipolarnoga tranzistora s horizontalnim tokom struje (HCBT), gdje je dan pregled najvažnijih mjerenih rezultata i varijanti tranzistora za postizanje visokih probojnih napona.

Drugo poglavlje opisuje skalarni mjerni sustav za karakterizaciju tranzistora u režimu velikog signala, metodologiju, i najvažnije rezultate koji se odnose na optimalne radne uvjete za HCBT u režimu velikog signala. Nadalje, opisana je korištena ispitna tiskana pločica za mjerenje diskretnih tranzistora, i prikazan je postupak uklanjanja utjecaja prijenosnih linija koje ostvaruju prijelaz sa koaksijalnog standarda mjerne opreme, na miktotrakastu liniju koja predstavlja sučelje sa mjerenim tranzistorom. Prvi mjerni rezultati predstavljaju performanse HCBT-a površine emitera od 31.2 μm^2 uz zaključenje optimalnim impedancijama za postizanje maksimalne izlazne snage. Mjerene veličine, poput izlazne snage, pojačanja, i korisnosti, matematički su opisane, kao i analitička metoda za izbor početne istosmjerne radne točke za karakterizaciju. Metodologija mjerenja sadrži karakterizaciju tranzistora u režimu velikog signala uz zaključenje na ulazu i izlazu impedancijom od 50 Ω, mjerenje izlazne snage i korisnosti u ovisnosti o raznim vrijednostima ulazne i izlazne impedancije, i na kraju, mjerenje izlazne snage i korisnosti za optimalno zaključenje dobiveno iz prethodnih koraka analize. Uz optimalno zaključenje i rad u klasi A, HCBT postiže maksimalnu linearnu izlaznu snagu od 16.95 dBm i korisnost od 30%. Od tri analizirane klase rada, A, AB, i B, HCBT postiže najbolje performanse u klasi AB, gdje dostiže izlazu snagu od 18.6 dBm, pojačanje od 10 dB, i korisnost od 46%, uz optimalne impedancije bliske impedanciji sustava od 50 Ω. Rezultati ukazuju na pogodnost analiziranih HCBT-a za primjene u širokopojasnim RF pojačalima snage.

Utjecaj karakteristika strukture tranzistora na performanse u režimu velikog signala je, nadalje, ispitan karakterizacijom HCBT-a tri različita kolektorska doping profila, korištenjem sustava za karakterizaciju u režimu velikog signala. Tri tranzistora razlikuju se u maksimal-

nom dopingu, kao i u profilu primjesa u području intrinzičnog kolektora, a to su: HCBT sa uniformnim, CMOS n-*well*, i niskodopiranim kolektorom, a površine kolektora 58.5 μm^2. Objašnjena je metodologija za izbor optimalne struje istosmjerne radne točke analizirajući maksimalno pojačanje snage za mali signal, na frekvencijama 0.9, 1.8, i 2.4 GHz. Izbor optimalnog napona istosmjerne radne točke temelji se na maksimalnom naponu između kolektora i emitera koji osigurava stabilan rad za sve vrijednosti snage ulaznog signala. Ovaj napon je, stoga, određen kao nešto niži napon od probojnog napona BV_{CEO}. Mjerni rezultati pokazuju da HCBT sa niskodopiranim kolektorom postiže najviše pojačanje snage, a HCBT sa CMOS n-*well* kolektorom, najvišu korisnost, uz optimalno zaključenje na ulazu i izlazu. Također, HCBT sa niskodopiranim kolektorom ima optimalne impedancije najbliže 50 Ω, što pruža najbolje rješenje za primjene u širokopojasnim pojačalima snage. U području nižih ulaznih snaga od maksimalne (eng. *power back-off*), HCBT sa CMOS n-*well* daje najvišu linearnu izlaznu snagu i korisnost, pa tako predstavlja najbolji izbor u primjenama gdje je korisnost u linearnom području najvažniji parametar.

U trećem poglavlju, istražene su granice linearnog rada HCBT-a u režimu velikog signala. S ciljem pronalaska linearnog područja rada na visokim frekvencijama, postavljen je i kalibriran vektorski mjerni sustav sa mogućnosti mjerenja vremenskih valnih oblika na visokim frekvencijama. Navedeni mjerni sustav koristi osciloskop koji radi na principu poduzorkovanja za mjerenje periodičnih visokofrekvencijskih signala, a preciznom karakterizacijom komponenti sustava, mjerna referentna ravnina pomaknuta je na kolektorski kontakt na čipu unutar kućišta diskretnog tranzistora. Predstavljena je i opisana metodologija za mjerenje područja linearnog rada, koja obuhvaća snimanje radnih pravaca na frekvencijama 0.9, 1.8, i 2.4 GHz, za ulaznu snagu u kojoj pojačanje tranzistora padne za 1 dB (P1dB). Izborom odgovarajuće istosmjerne radne točke i impedancije tereta, određena je granica linearnog rada, koja je, nadalje, određena područjima zasićenja i Kirk efekta. Izmjerena granica definira istosmjernu radnu točku i radni pravac za maksimalnu izlaznu snagu, uz uvjet da je postavljen maksimalni izlazni napon tranzistora. Za niskodopirani HCBT, ova analiza daje maksimalnu izlaznu snagu od 21.25 dBm i korisnost od 30% u klasi A, uz maksimalni izlazni napon od 9 V.

Drugi dio trećeg poglavlja predstavlja rezultate analize ponašanja istosmjerne radne točke u ovisnosti ulaznoj snazi. Točnije, analizirana je ovisnost istosmjernih veličina HCBT-a o ulaznoj snazi, i to za nelinearnost valnih oblika uzrokovanu različitim područjima izlaznih karakteristika bipolarnog tranzistora; zapiranjem, zasićenjem, i probojem. Glavne poteškoće u radu pojačala snage uzrokuje promjena istosmjerne točke prilikom ulaska u kompresiju, stoga, analizirani su radni pravci u točki kompresije, i to za dvije različite konfiguracije napajanja baznog kruga; naponskim i strujnim izvorom. Za izobličenje radnog pravca u zapiranju, rezultati pokazuju da je područje linearnog rada 13 dB veće za napajanje baznog kruga naponskim izvorom u odnosu na strujni izvor, što je rezultat rasta istosmjerne struje kolektora zbog izobličenja u

ulaznom krugu tranzistora. Suprotno je dobiveno za izobličenje u području zasićenja, gdje je područje linearnog rada 1 dB veće u slučaju napajanja baznog kruga strujnim izvorom. Zanimljivi rezultati dobiveni su za naponski hod veći od probojnog napona, gdje se utjecaj lavinske multiplikacije ne vidi na valnim oblicima struje i napona, ali je izražen kao nagli rast istosmjerne struje kolektora u blizini točke kompresije. Rezultati dobiveni u ovom poglavlju važni su za izbor optimalnih radnih uvjeta HCBT-a koji se koristi za projektiranje RF pojačala snage opisanih u sljedećim poglavljima.

U četvrtom poglavlju, opisan je postupak projektiranja i karakterizacije Doherty RF pojačala snage izrađenog sa HCBT-om na 2.4 GHz. Ukratko je objašnjena teorija pojačala, gdje se koristi aktivna modulacija impedancije tereta pojačala za postizanje optimalnog prilagođenja i za snage ulaznog signala niže od snage u točki kompresije. Pojačalo se sastoji od dva jednostavnija pojačala snage, klase AB i C, gdje pojačalo klase C modulira izlaznu impedanciju pojačala klase AB. Optimalne impedancije za oba pojačala pronađene su korištenjem sustava za karakterizaciju tranzistora u režimu velikog signala, a ulazne i izlazne prilagodne mreže projektirane su koristeći elektromagnetske simulacije fizičkog dizajna pločice. Pojačalo je implementirano na pločici materijala FR4, dielektrične konstante 4.3, i debljine 1 mm, a prijenosne linije su mikrotrakastoga tipa. Doherty pojačalo implementirano s HCBT-ima postiže 22 dBm izlazne snage i maksimalnu korisnost kolektora od 45%. Uz pobudu moduliranim signalom treće generacije, omjera vršne i srednje snage (PAPR) 3.5 dB i širine pojasa od 10 MHz, pojačalo postiže 38.7% srednju korisnost kolektora, na frekvenciji nosioca od 2.4 GHz, što je usporedivo sa pojačalima implementiranim u naprednijim i skupljim poluvodičkim tehnologijama.

U petom poglavlju, opisano je projektiranje pojačala snage širokog pojasa tipa *balanced*, koje se sastoji od dva jednaka pojačala snage klase AB, a također je implementirano koristeći diskretni HCBT na središnjoj frekvenciji od 2.4 GHz. Ova arhitektura pojačala snage koristi ulazni i izlazni hibridni sprežnik za postizanje širokog propusnog pojasa, gdje je moguće dobiti izvrsno ulazno i izlazno prilagođenje, neovisno o prilagodnim mrežema pojedinih pojačala arhitekture. Ulazni i izlazni sprežnici projektirani su u *double-box* tehnici kako bi se postigao velik frekvencijski pojas, a karateristike sprežnika optimirane su koristeći elektromagnetske simulacije fizičkog dizajna. Sprežnik je implementiran i karateriziran na posebnoj pločici i postiže širinu pojasa od 800 MHz, i razliku u fazi dvaju izlaznih signala od 89.6° na 2.4 GHz. Mikrotrakaste prijenosne linije korištene su za projektiranje prilagodnih mreža i mreža za napajanje, a optimalne impedancije za pojedine tranzistore pronađene su korištenjem sustava za karakterizaciju tranzistora u režimu velikog signala. Za napajanje, korištena je četvrtvalna prijenosna linija, koja, uz visoku impedanciju prema napajanju na fundamentalnoj frekvenciji, daje i nisku impedanciju na frekvenciji drugog harmonika, što povećava korisnost pojačala snage u klasi AB. Izrađeno HCBT *balanced* pojačalo snage na 2.4 GHz, postiže izlaznu snagu od $21.4 +/- 0.18$ dBm, pojačanje snage od $10.4 +/- 0.15$ dB, korisnost kolektora najmanje 36%

u propusnom pojasu, i širinu frekvencijskog pojasa od 700 MHz. Performanse pojačala snage usporedive su ili bolje od pojačala snage implementiranih u nekima od skupljih poluvodičkih tehnologija.

Zadnje poglavlje „*Conclusion*“, daje osvrt na glavne rezultate dobivene u sklopu provedenog istraživanja, i preporuke za daljnji rad u području karakterizacije HCBT-a u režimu velikog signala i projektiranja RF pojačala snage, kako u diskretnoj, tako i u integriranoj tehnici.

Ključne riječi: bipolarni tranzistor s horizontalnim tokom struje (HCBT), bipolarni tranzistori, režim velikog signala, skalarni sustav za karaterizaciju u režimu velikog signala, vektorski sustav za karaterizaciju u režimu velikog signala, mjerenje visokofrekvencijskih valnih oblika, područje linearnog rada, pojačala snage, Doherty.

Contents

Chapter 1

Introduction

The connectivity of people and devices tremendously evolved over the last decade with the proliferation of high-speed and low-latency communications. Countless smartphones, computers, and gadgets, employ such a connectivity to collect data and perform tasks to increase the quality of our lives. The key enabler of this ubiquitous connectivity are wireless communications, the fastest growing segment of the communications industry.

1.1 Wireless communications

The vision of wireless connectivity where every device, vehicle, sensor, or home appliance, is connected to a common network and communicates efficiently real-time and all the time, is a tendency of both the industry and academic research [1]. Nowadays, the wireless communications market grows at a remarkable pace due to high-performance handheld devices, usually termed smartphones, with the ability to create multimedia materials of high quality and send them across the world at an instant. Additionally, the automotive industry is adopting the wireless communications in the form of radars of a small form factor, which can detect and thereby prevent the collision if the driver fails to react. More importantly, the wireless connectivity plays a crucial role for the networks which predict or analyze the events hazardous to human life, such as massive networks of wireless-enabled sensors monitoring fire hazards, hazardous waste sites, stress and strain in buildings and bridges, or the spread of chemicals and gasses at a disaster site. Therefore, the wireless communications provide a means of monitoring the places and processes which are difficult or impossible to approach by a human, or observe over a wired network.

1.1.1 Radiofrequency spectrum

Wireless communications employ radiofrequency waves to send and receive the information over the air. The frequencies of interest for the modern wireless communications are placed in

the range from 300 MHz to 300 GHz. The frequency range is further segmented in multiple frequency bands for easier reference, as shown in Tab. 1.1 [2, 3], where the letter designations for radar systems are also shown due to their widespread use in commercial wireless communications. Although the bands span up to the visible light, the majority of commercial wireless communications nowadays operate in the range from 300 MHz to 6 GHz, wherein the most of the commercial wireless communication standards are defined.

Table 1.1: Designations of frequency bands according to International Telecommunication Union [2] (left), and radar frequency bands according to The Institute of Electrical and Electronics Engineers (IEEE) [3] (right).

Band no.	Symbols	Frequency range
3	ULF	300 - 3000 Hz
4	VLF	3 - 30 kHz
5	LF	30 - 300 kHz
6	MF	300 - 3000 kHz
7	HF	3 - 30 MHz
8	VHF	30 - 300 MHz
9	UHF	300 - 3000 MHz
10	SHF	3 - 30 GHz
11	EHF	30 - 300 GHz
12		300 - 3000 GHz
13		3 - 30 THz
14		30 - 300 THz
15		300 - 3000 THz

Band designation	Frequency range
HF	3 - 30 MHz
VHF	30 - 300 MHz
UHF	300 - 1000 MHz
L	1 - 2 GHz
S	2 - 4 GHz
C	4 - 8 GHz
X	8 - 12 GHz
Ku	12 - 18 GHz
K	18 - 27 GHz
Ka	27 - 40 GHz
V	40 - 75 GHz
W	75 - 110 GHz
mm	110 - 300 GHz

1.1.2 Wireless communication standards

The development of wireless communication standards is mainly driven by the preferences of the users, thus, roughly every ten years a new standard generation brings new applications along with a significant increase in performance [4].

First generation (1G)

The basic service in the first generation of mobile communications was voice calling. The coverage was excellent, but due to the different proprietary standards in different countries, completely different equipment was needed when travelling from one country to another.

Second generation (2G)

The second generation of mobile communications was a synonym for the most widespread Global System for Mobile Communication (GSM) standard. The GSM brought along the widely used short messaging service (SMS). Additionally and more significantly, the GSM offered first data transfer service with the speed of 9.6 kbps. Later on, the General Packet Radio Services (GPRS) and Enhanced Data Rates Service (EDGE) increased the speed to several tens of kilobits and 1-200 kpbs, respectively.

Third generation (3G)

The third generation, on the other hand, is a synonym for Universal Mobile Telecommunication System (UMTS). The most significant novelty is a data transfer speed of 2 Mbps. Nevertheless, the end-user speed did not go above 364 kbps, which made UMTS not as quite successful. Only did the later introduction of High-Speed Uplink Packet Access (HSUPA) and High-Speed Downlink Packet Access (HSDPA) bring more popularity, supporting several tens of megabits per second. This, for the first time, enabled the access to the e-mail service over a wireless network.

Fourth generation (4G)

The main wireless communication standard in the fourth generation is Long-Term Evolution (LTE) [5]. The standard is still evolving nowadays, with the highest speeds of 1 Gbps, whereas the voice calling service is transferred to the Internet Protocol (IP), called voice-over-IP, which enables much higher voice quality with respect to legacy solutions.

Fifth generation (5G) and beyond

The deployment of the fifth generation of mobile communications is currently in progress, whereas the specifications for the sixth generation are also debated among the industry and regulatory bodies. The newest generations, besides the sub-6 GHz spectrum, employ the milimeter-wave spectrum which enables much wider channel bandwidths and, therefore, higher data throughputs [6].

Wi-Fi

The above mentioned standards are based on a concept of frequency reuse wherein the network is spatially divided in cells [1]. Although not a cellular network, one of the most important wireless communication standards in use is wireless fidelity or Wi-Fi. It enables high-speed wireless connections of smaller area coverage than the cellular networks, commonly used for indoor

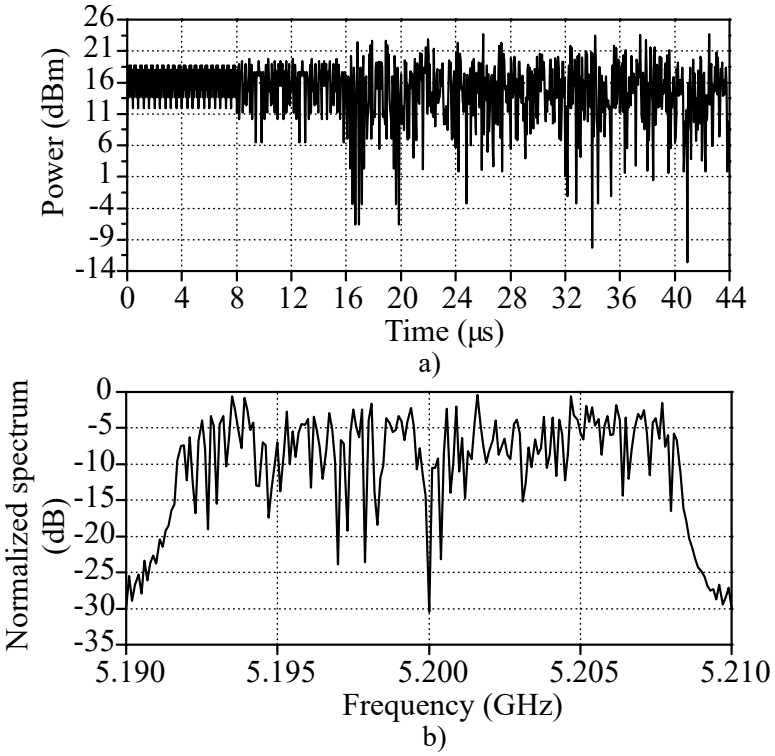


Figure 1.1: Power (a) and spectrum (b) of 802.11a standard-compliant OFDM signal at the carrier frequency of 5.2 GHz and bandwidth of 20 MHz.

high-performance wireless communication. The Wi-Fi has a lot in common with the modern cellular networks since the LTE is developed by borrowing the traits of the physical network layer from the Wi-Fi. More precisely, both 4G LTE, 5G, and Wi-Fi, employ the same signal modulation, which is used in digital wireless communications to imprint the digital information to the radiofrequency signal, namely, Orthogonal Frequency Division Multiplex (OFDM).

1.1.3 Modern modulated signals

The characteristics of the radiofrequency signal transmitted over the air are modulated in accordance to the digital information being sent. The goal of the modulation is to send as much as possible bits of information in a given time period and over a given bandwidth, usually termed spectral efficiency and measured in b/s/Hz. The OFDM is a modulation of choice for all modern wireless communication standards since it provides the highest spectral efficiency and, additionally, a way to combat the multipath propagation [1]. The example OFDM-modulated signal is shown in Fig. 1.1 both in time and frequency domains. The main characteristics of such a modulated signal is a power which varies in time and a relatively wide bandwidth. In the time domain, the signal is formatted in time frames, which can be discerned from Fig. 1.1a. For example, at the beginning of the transmission ($t = 0$ s), there is a guard interval of 8 μs in which no information bits are being sent. Besides the bandwidth, some information is also visible from the spectrum in Fig. 1.1b, e.g., there is no carrier frequency of 5.2 GHz in the

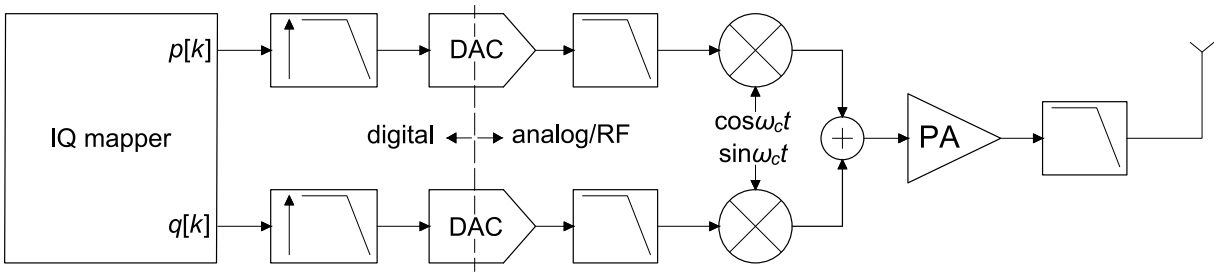


Figure 1.2: Block diagram of a direct up-conversion (DU) or zero-intermediate frequency (ZIF) transmitter. The transmitter is divided in digital and analog/RF part. The IQ mapping and oversampling take place in digital domain. Digital signal is converted to analog signal and passed to the reconstruction filter for the rejection of unwanted spectrum images of the baseband signal. The signal is then amplified, filtered, and passed to the antenna for the transmission.

transmitted signal, since carrier alone does not carry the information. To further investigate the characteristics of the modulated signals employed in wireless communications, an overview of the architecture and operation of a radiofrequency transmitter is given in the following.

1.2 Radiofrequency transmitter

The transmitter is responsible for modulating the digital information onto the carrier frequency. There are many ways to perform this task and, consequently, there are many transmitter architectures. The choice of wireless transmitter architecture depends on many factors, which are mainly dictated by the application and communication standard that the transmitter operates in. Some of the most important parameters to consider are performance, bandwidth, complexity of implementation, output power, and cost.

Due to its simplicity and low cost, a direct up-conversion (DU,) also called zero-intermediate frequency (ZIF), transmitter architecture recently became popular in cellular radio systems [7, 8, 9, 10]. This architecture does not employ an intermediate-frequency mixing stage and provides more flexibility in designing multi-standard, multi-band transmitters for modern radio systems [11]. An example of this radiofrequency transmitter architecture is shown in Fig. 1.2. The resulting modulated bandpass signal at the output of the transmitter is given by [12]

$$s(t) = \Re\left\{\tilde{s}(t)\, e^{j\omega_c t}\right\}, \tag{1.1}$$

where ω_c is the carrier frequency, whereas $\tilde{s}(t)$ is a complex modulated baseband signal given by

$$\tilde{s}(t) = p(t) + jq(t), \tag{1.2}$$

where p and q are in-phase and quadrature components of the baseband signal, respectively.

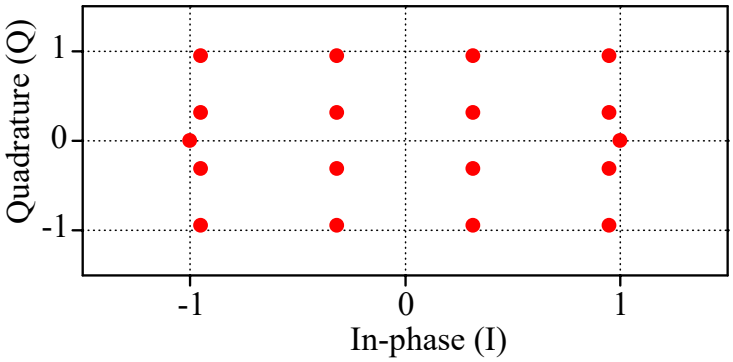


Figure 1.3: Constellation of the 802.11a-compliant OFDM signal. The constellation consists of both the BPSK and 16QAM points.

The transmitter can be separated in two main parts; the digital and analog section. The two differ with respect to the signals being processed. Additionally, the analog part deals with both the low-frequency baseband signals and radiofrequency signals to be transmitted.

Both p and q signals are processed separately in the transmitter. The $s(t)$ is a sum of sine waves with amplitude and phase determined according to the wireless communication standard employed. Firstly, the digital representation of a complex modulated bandpass signal $\tilde{s}(t)$ is generated in the IQ mapper according to the constellation of the modulation. The constellation diagram of the signal from Fig. 1.1 is shown in Fig. 1.3. Each constellation point carrier certain number of information bits. The shown constellation is, actually, composed of two separate modulations; Binary Phase Shift Keying (BPSK) with two points at (-1, 0) and (1, 0), and Quadrature Amplitude Modulation with the rest 16 points (16QAM). The two modulations are part of the OFDM modulation scheme used in Wi-Fi.

Information bits are assigned (mapped) to the constellation points of the modulation and the p and q are then created entirely in the digital domain [13]. Hence, sampled versions of $p(t)$ and $q(t)$, $p[t]$ and $p[t]$, are output from the IQ mapper. Such sampled signals exhibit spectrum that repeats itself at the multiples of the sampling frequency f_s. The frequency separation between those unwanted spectrum images usually implies filters with high roll-off that are difficult to design. Because of that, the signals are delivered to the oversampling stage to increase this frequency separation and relax the constraints on the reconstruction filter that comes later in the transmitter chain. Oversampling is implemented in the digital domain by zero padding the original digital signal [13]. The oversampled signals are then converted to analog domain using the digital to analog converters (DACs) and unwanted spectrum images are filtered out by the reconstruction filter stage. The baseband analog signals, $p(t)$ and $q(t)$, are then up-converted to the carrier frequency f_c such that the quadrature component is multiplied with the sine function and the in-phase component with the cosine function. The signals are then summed, resulting in a signal given by (1.1), and delivered to the power amplifier. Finally, the signal is amplified by the power amplifier stage and filtered to reject out-of-band emission

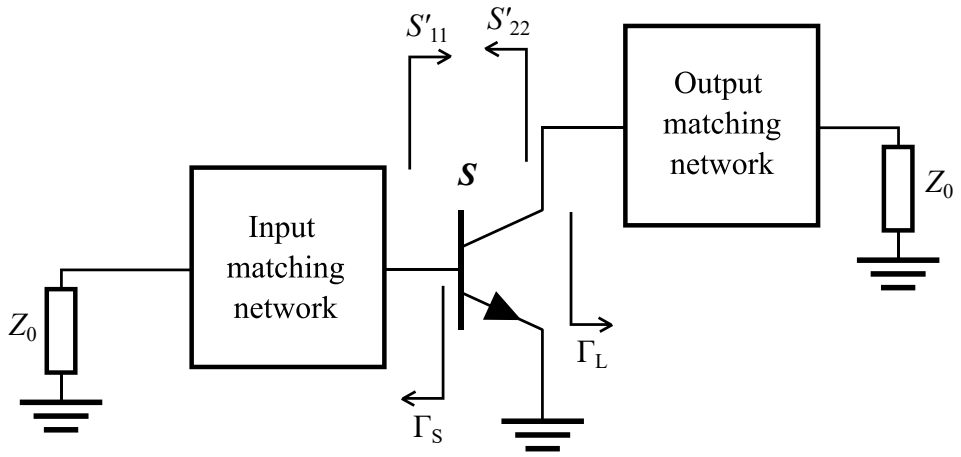


Figure 1.4: Block schematic of the amplifier for small-signal analysis with a bipolar transistor as an active device.

resulting from the nonlinearity of the power amplifier, and lastly, the signal is fed to the antenna.

1.3 Radiofrequency power amplifier

The bandpass signal of (1.1) is usually of insignificant power when output from the summation stage. Since the range of wireless communication is determined to a large extent by the power of the radiated signal, an amplification is needed to increase the power of this signal. A radiofrequency power amplifier (PA) amplifies the bandpass signal to be transmitted over the wireless communication channel. It dissipates the greatest amount of power in the transmitter. Furthermore, while amplifying the useful bandpass signal, it generates an in-band distortion that degrades the quality of the transmitted signal, and out-of-band distortion that pollutes adjacent frequency channels in use by other users. Additionally, power amplifiers for modern radio systems need to be efficient and also highly linear to provide signals of sufficient quality for a proper demodulation at the receiver side.

1.3.1 Small-signal operation

A power amplifier excited by a signal of a small enough amplitude so that neither voltage nor current swing is limited at the terminals of the amplifier, is operating in the small-signal regime. It is assumed in this regime that the output signal is a linear function of the input signal. The performance of such an amplifier can be analysed and predicted employing a linear analysis. To analyze the amplifier in the small-signal regime, scattering parameters, termed S parameters, are readily employed [14]. Due to the difficulty of measuring voltage and current at high frequencies, an S parameter is defined as a ratio of two voltage travelling waves at specified measurement planes, called reference planes.

The block schematic of an amplifier used for small-signal analysis is shown in Fig. 1.4 [15]. The active device providing the necessary gain is a transistor of a bipolar or metal-oxide-semiconductor (MOS) type. Regardless of the technology, a transistor is described by

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{1.3}$$

where $\mathbf{S}$ is the S-matrix of the transistor. The input and output matching networks are passive networks used to match the impedance of the transistor to the system impedance $Z_0 = 50\ \Omega$. The matching networks resonate out the parasitics of the transistor so that the maximum gain is achieved for a given active device. The transformation is contained in the reflection coefficients Γ_S and Γ_L for the input and output, respectively. Since the matching networks are passive, the following applies:

$$|\Gamma_S| < 1, \tag{1.4}$$

and

$$|\Gamma_L| < 1. \tag{1.5}$$

It can be shown that the input and output impedances are a function of the output and input networks, respectively [14]. The reflection coefficient looking into the input port of the transistor, S'_{11}, is given by

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \tag{1.6}$$

whereas the reflection coefficient looking into the output port of the transistor, S'_{22}, by

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{1.7}$$

To achieve maximum transfer of the signal from the source to the input port of the transistor, the input matching network is designed so that

$$S'_{11} = \overline{\Gamma_S}. \tag{1.8}$$

Similarly, the output matching network is designed so that the maximum signal transfer is achieved from the output port of the transistor to the load:

$$S'_{22} = \overline{\Gamma_L}. \tag{1.9}$$

One important parameter regarding the stability of the amplifier, termed Rollet's stability factor k, can be calculated as

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2S_{12}S_{21}}. \tag{1.10}$$

wherein D is a determinant of the $\mathbf{S}$. The k parameter gives the information about the stability of the amplifier; if $k > 1$, it can be shown that both $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$, which are constraints which need to be met if the passive matching networks are to be designed. In other words, $k > 1$ ensures a stable small-signal operation of the amplifier. If (1.8) and (1.9) are fulfilled, the gain of the amplifier is equal to the S_{21} parameter of the transistor.

Although the small-signal analysis assumes a linear relationship between the output and input signals, the nonlinearities arise in the small-signal range due to the nonlinearities of the transistor. These nonlinearities are usually described by a power series

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 + \cdots +, \tag{1.11}$$

where v_i, v_o, and a_i, are input voltage, output voltage, and voltage gain of the transistor, respectively, and are sometimes called weakly nonlinear effects [15], since they arise in the small-signal (linear) regime. The weakly nonlinear effects are the cause of intermodulation distortion which results in the in-band distortion.

1.3.2 Large-signal operation

In a normal operation, however, a power amplifier is operating with signals which are comparable in amplitude to its maximum current and voltage ratings. Therefore, such signals, for certain input power levels, experience clipping at the terminals of the amplifier. Since the clipping of the voltage and/or current waveforms is a distortion of the signal, such a regime is termed large-signal operation. Therefore, these nonlinearities are termed strongly nonlinear effects since they occur in large-signal operation.

The large-signal performance of an example power amplifier is shown in Fig. 1.5. The performance entails output power (AM/AM) and phase (AM/AM) of the output signal as a function of the power of the input signal at the fundamental (carrier) frequency [16]. Due to the strongly nonlinear effects present, the output power does not increase linearly with the input power, in high-power range. The increase of output power becomes smaller and, at certain input power levels, saturates. The region of the transfer characteristics in which the output power increase starts to deviate from the linear function, is called a compression. Additionally, the phase difference between the output and input signals is also a function of the input power. The gain of the amplifier is, therefore, decreasing due to the output power saturation.

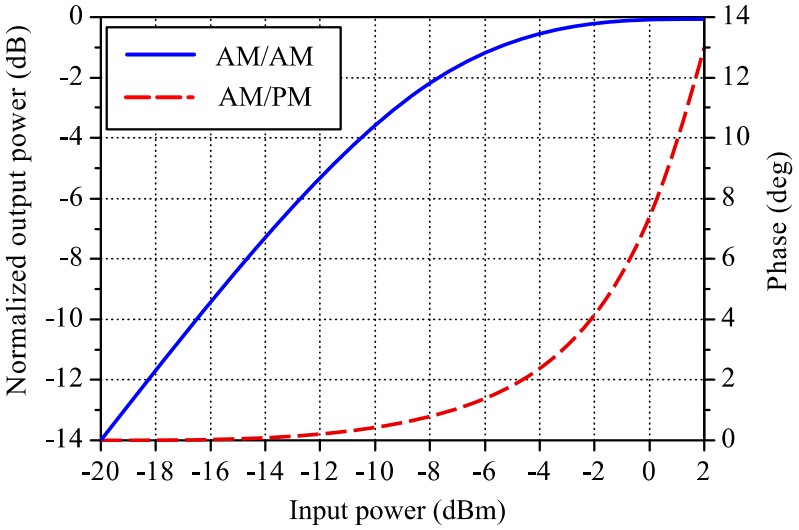


Figure 1.5: Transfer characteristics of a power amplifier at the fundamental frequency. The dependence of output power (AM/AM) and phase (AM/PM) on input power are shown.

The impact of large-signal operation on the output signal is shown in Fig. 1.6, where the spectrum and constellation diagram of the OFDM signal from Fig. 1.1 is shown at the output of the power amplifier operating in the compression region. The input power is high enough so that, besides weakly nonlinear effects, the strongly nonlinear effects also have significant impact on the output signal. As shown in Fig. 1.6a, the power is radiated in the neighbouring frequency bands, thus interfering with other communication channels. Additionally, an example of a spectrum mask is shown, which defines the maximum power in the adjacent frequency bands with respect to the channel power. The mask is defined for all wireless communication standards in order to limit the interference between the adjacent channels [17]. In the example shown in the figure, the power amplifier outputs higher power in the adjacent bands than the allowed by the communication standard. Furthermore, due to the clipping of the voltage and current waveforms at the output of the amplifier, the output signal contains significant power at the harmonics of the the carrier frequency, usually termed the fundamental frequency.

The spectrum of the signal gives information about the output power in the adjacent bands, but not about the quality of the transmitted information. To analyze the quality of the transmitted signal, the signal should be demodulated by the receiver so that the received signal can be compared to the transmitted one. The constellation of the transmitted signal of Fig. 1.6a, is shown in Fig. 1.6b. The constellation points deviate from the reference constellation of Fig. 1.3. The probability of a receiver demodulating the information of a specific constellation point depends on how far the point is from its reference location. Therefore, due to the difference between the transmitted signal's constellation and the ideal one, the probability of a demodulation error is higher, thus, increasing the bit error rate (BER) of the communication channel.

Linearity constraints are becoming increasingly difficult to satisfy because of the complex modulations envisioned for the future wireless communications employing dense constellation

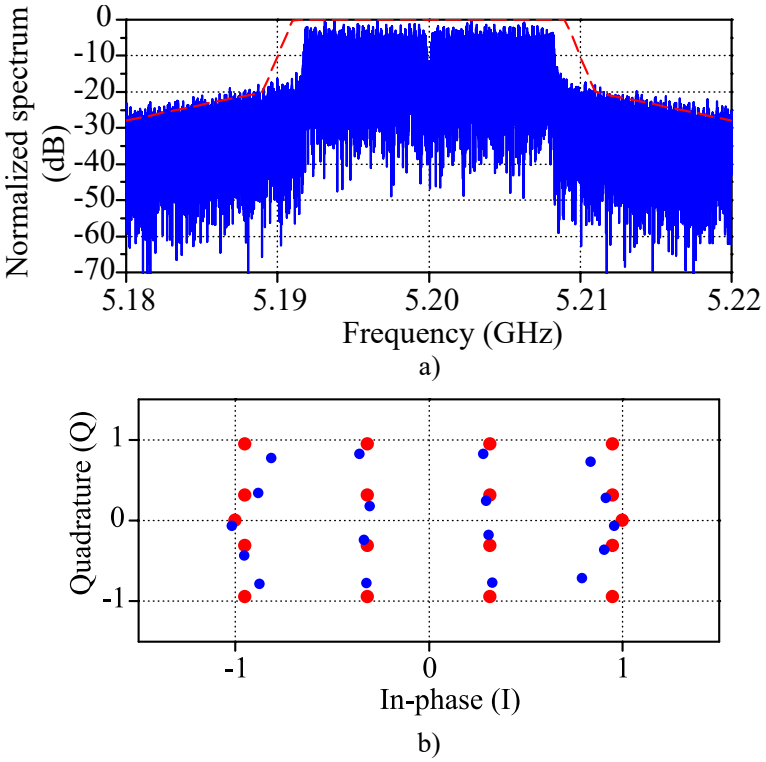


Figure 1.6: Spectrum (a) and constellation diagram (b) of a 802.11a-compliant OFDM signal from Fig. 1.1 for the power amplifier operating in compression. The spectrum mask [17] (red dashed line) shown in (a) for reference. Both the transmitted (blue dots) and reference (red dots) constellation diagrams shown in (b) for reference.

diagrams [4], e.g. 1024QAM or 4096QAM. Although the large-signal operation of the power amplifier negatively impacts the performance of the wireless communication channel, the necessary output power to achieve a desired communication range is usually set near the compression region. If the input signal power is decreased to achieve a linear response, the performance of the power amplifier degrades significantly. In other words, the power amplifier operates with the optimal performance in the compression, which can be described employing the performance parameters of the power amplifier.

1.3.3 Performance parameters

The performance of the power amplifier is described by a different set of parameters with respect to small-signal amplifiers. The most important performance parameters of a power amplifier directly influencing the performance of the transmitter are:

- Output power - a power delivered from the output of the amplifier to the load at the fundamental frequency, defined by

$$P_{\mathrm{OUT}} = \frac{1}{2}\Re\{V_{\mathrm{OUT}}\overline{I_{\mathrm{OUT}}}\}, \tag{1.12}$$

where P_{OUT}, V_{OUT}, and $\overline{I_{\mathrm{OUT}}}$, are real output power, output voltage phasor, and a complex-conjugate of the output current phasor, respectively.

- Gain - a ratio of the output power and the input power, defined by

$$G = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}}, \tag{1.13}$$

where G and P_{IN} are the gain and input power of the amplifier.

- Collector/drain efficiency - a ratio of the output power and DC power consumed, defined by

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{DC}}} \cdot 100\%, \tag{1.14}$$

where P_{DC} is a DC power consumed by the amplifier. Since η does not take into account the input RF power, power-added efficiency (PAE) is defined by

$$\mathrm{PAE} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}} = \eta \left(1 - \frac{1}{G}\right) \cdot 100\%, \tag{1.15}$$

where PAE is the power-added efficiency of the amplifier.

- Linearity - defined separately for in-band and out-of-band signals. The out-of-band emissions are taken into account by adjacent channel power ratio (ACPR), defined by

$$\mathrm{ACPR} = \frac{P_{\mathrm{ADJ}}}{P_{\mathrm{MAIN}}}, \tag{1.16}$$

where P_{ADJ} and P_{MAIN} are powers of the adjacent and main channel, respectively. This measure is limited by the communication standards and, in general, should be as low as possible. The example of a power amplifier exhibiting high ACPR is shown in Fig. 1.6a. The in-band linearity is described by measuring the difference between the transmitted and ideal constellation diagrams and averaging over time frames, the process which is also defined in the respective standards. The parameter quantifying the in-band linearity of the power amplifier is error vector magnitude (EVM), defined by [18]

$$\mathrm{EVM}_{\mathrm{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} |S_{\mathrm{ideal,i}} - S_{\mathrm{meas,i}}|^2}}{\sqrt{\frac{1}{M}\sum_{i=1}^{M} |S_{\mathrm{ideal,i}}|^2}}, \tag{1.17}$$

where $S_{\mathrm{ideal,i}}$ and $S_{\mathrm{meas,i}}$ are the ideal and measured (transmitted) constellation points, respectively. The calculation of EVM is done over many symbols (N) and then normal-

ized, which is defined by a factor M. In essence, the EVM is a ratio of the root mean square value of all the error vectors, averaged over N symbols, and then divided by some normalization factor.

The performance of a power amplifier is directly influenced by the chosen circuit architecture. Thus, the performance parameters are dependent on the chosen transistor, bias point, input and output matching impedances seen by the transistor, and the class of operation.

1.3.4 Classes of operation

A power amplifier can operate in different classes of operation, depending on the bias level, load impedance, and input signal. Since the output is of a main concern, the ideal equivalent schematic of the output of the power amplifier is shown in Fig. 1.7a. The schematic consists of a current generator and a load resistor. The current generator represents an ideal behaviour of the output of a transistor, be it a bipolar or a MOS [15]. The current generator provides the current I_g to the load resistor R_{load}. The result of this is the output voltage V_{out}, which is set across the load resistor. The output power can now be calculated as

$$P_{OUT} = \frac{1}{2} V_{out} I_g = \frac{1}{2} I_g^2 R_{load}. \tag{1.18}$$

where I_g and V_{out} are the amplitudes of the current through, and voltage across the resistor R_{load}. According to (1.18), the output power can be increased indefinitely by increasing the load resistance R_{load} or current I_g, wherein the latter is increased by increasing the amplitude of the input signal. This fact is the result of the current generator not having maximum current and voltage ratings. On the other hand, a transistor operates reliably up to a certain voltage and current values, which then directly define the maximum allowed voltage and current amplitudes at the terminals of the transistor. Since the load resistance and input power, therefore, determine the voltage and current amplitudes, respectively, their value should be selected such that the maximum voltage and current values at the output are not higher than the maximum allowed values for a given active device.

Therefore, the load resistance and input power define the load line at the output of the transistor. If it is assumed that the maximum voltage and current values supported by the transistor are, for simplicity, defined by

$$V_{max} = 1 \text{ V}, \tag{1.19}$$

and

$$I_{max} = 1 \text{ A}, \tag{1.20}$$

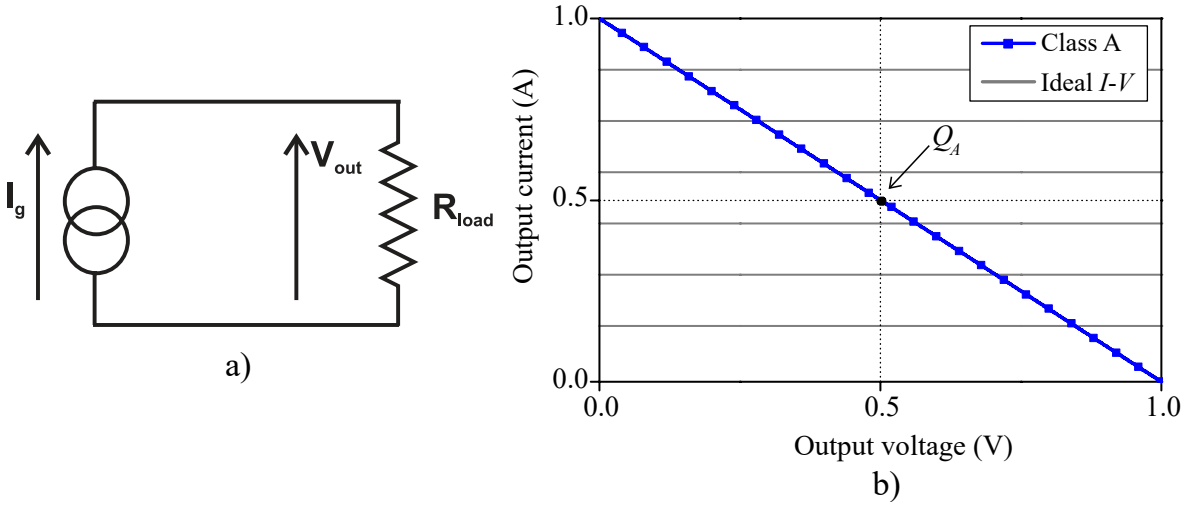


Figure 1.7: (a) Ideal equivalent schematic of the output of the power amplifier and (b) load line for Class-A operation. The output *I*-*V* characteristics of the current generator from (a) are also shown.

then, the maximum output power for a given transistor is achieved when the load line is defined as in Fig. 1.7b.

Class-A

Both the voltage and current swing from 0 V to 1 V and 0 A to 1 A, respectively. The bias point and load impedance are set such that the maximum voltage and current swings are achieved. Thus, the bias point is

$$Q_{\mathrm{A}} = (I_{\mathrm{QA}}, V_{\mathrm{QA}}) = (0.5\ \mathrm{A}, 0.5\ \mathrm{V})\,, \tag{1.21}$$

where I_{QA} and V_{QA} are DC current and voltage in bias point Q_{A}, respectively. The load resistance is given by

$$R_{\mathrm{load}} = \frac{V_{\mathrm{out}}}{I_{\mathrm{g}}} = \frac{0.5}{0.5} = 1\ \Omega. \tag{1.22}$$

It is evident from (1.21) and (1.22) that the amplitudes of the voltage and current, V_{out} and I_{g}, are equal to 0.5 V and 0.5 A, respectively. Then, according to (1.18), the maximum output power for this transistor, $P_{\mathrm{OUT,max}}$, is

$$P_{\mathrm{OUT,max}} = \frac{1}{2} \cdot 0.5 \cdot 0.5 = 125\ \mathrm{mW}. \tag{1.23}$$

where $I_{\mathrm{g}} = (1/2)I_{\mathrm{max}}$ and $V_{\mathrm{out}} = (1/2)V_{\mathrm{max}}$. Furthermore, the collector efficiency (a bipolar transistor assumed) is

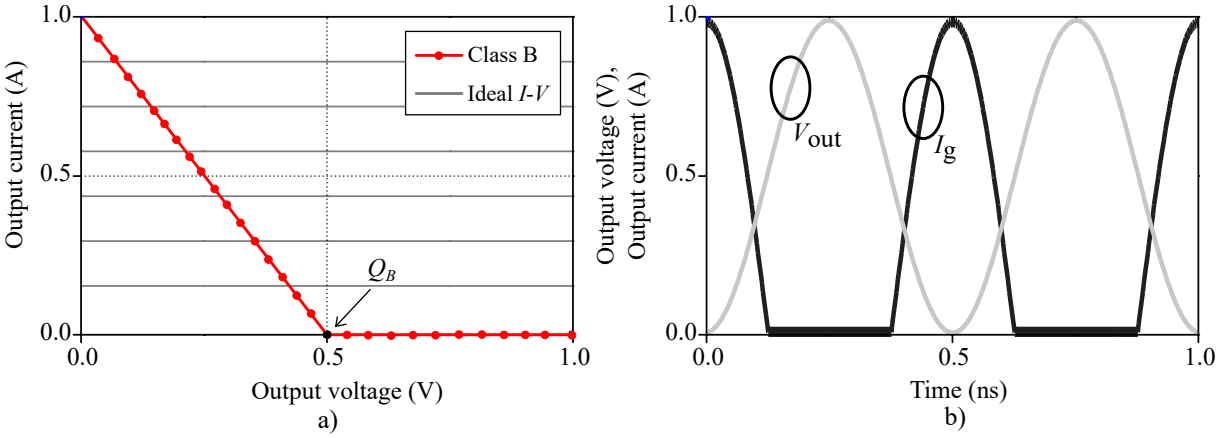


Figure 1.8: (a) Load line and (b) voltage and current waveforms of the fundamental frequency $f_0 = 2$ GHz for a Class-B power amplifier.

$$\eta = \frac{0.125}{0.5 \cdot 0.5} \cdot 100\% = 50\%. \tag{1.24}$$

The parameters calculated in (1.21) - (1.24) are for the Class-A power amplifier. Therefore, a Class-A PA provides the maximum output power for a given transistor while exhibiting a collector efficiency of 50 %.

It is assumed in this analysis that the input power is set at the level for which the current I_g swings from 0 A to 1 A. For lower input power, the output power is also lower, whereas the DC power is the same, thus, the efficiency is lower. For example, according to (1.24), for a 3-dB lower output power in Class-A operation, the collector efficiency drops to 25%. For a higher input power, the amplifier enters the compression region at the output [see Fig. 1.5], wherein the clipping of the voltage V_{out} and current I_g occurs due to the nonlinearities of the transistor. Additionally, the higher input power results in the higher output power which causes the voltage and current swings to go above the maximum values V_{max} and I_{max}. Therefore, the $P_{OUT,max}$ is a maximum output power if the current and voltage swings are to be kept at their maximum values.

Additionally, the gain of the Class-A power amplifier is equal to the small-signal gain, which, if (1.8) and (1.9) are satisfied, is equal to S_{21} parameter of the transistor. Therefore, the Class-A PA provides the small-signal gain and linear response for lower input powers, which is a great advantage for achieving high linearity.

Class-B

Although the Class-A provides a linear response, the efficiency is only 50%. According to (1.14), the collector efficiency can be increased by increasing the output power or by decreasing the DC power. The maximum output power is limited by the transistor, and, therefore, cannot be

increased above a certain value. On the other hand, the DC power can be decreased to achieve higher collector efficiency.

Since the power amplifier is operating with large signals, the DC current I_{Q} can be set, e.g., to 0 A, when there is no input signal present. Thus, the output current waveform resembles that of the half-wave rectified sine wave. The load line for such a mode of operation, termed Class-B, is shown in Fig. 1.8. Since the DC current is set to 0 A, the transistor (current source) conducts current only for the positive half-wave of the current waveform, whereas for the negative one, the transistor's cut-off region does not allow the negative current swing at the output. Due to the clipping of the current waveform, the output current signal contains the harmonics of the fundamental frequency. The voltage is, on the other hand, a full sine wave as is the case for the Class-A operation; there are no harmonics in the spectrum of the output voltage V_{out}. This is achieved by placing a parallel resonant tank of high quality factor across the load resistor R_{load}. The tank has its resonant frequency set at the fundamental frequency so that the harmonics get shorted to ground, whereas the fundamental frequency gets dissipated in the load. The voltage and current waveforms for Class-B operation are shown in Fig. 1.8b.

If the input power is set such that the current and voltage swing to I_{max} and V_{max}, the DC current is the DC component of the half-wave sine wave, given by

$$I_{\mathrm{QB}} = \frac{I_{\mathrm{max}}}{\pi} = 0.32 \text{ A}. \tag{1.25}$$

$$Q_{\mathrm{B}} = (I_{\mathrm{QB}}, V_{\mathrm{QB}}) = (0.32 \text{ A}, 0.5 \text{ V}), \tag{1.26}$$

where the I_{QB} is lower with respect to I_{QA}. The output power of Class-B PA can be found once the amplitude of the fundamental component of the current is determined. For a half-wave rectified sine wave, which swings from 0 to $I_{\mathrm{max}} = 1$ A, the fundamental component is given by

$$I_{\mathrm{g}} = \frac{I_{\mathrm{max}}}{2} = 0.5 \text{ A}, \tag{1.27}$$

which is exactly equal to the amplitude of the current in Class-A operation. Thus, the output power is also the same and given by (1.23), whereas the collector efficiency is

$$\eta = \frac{0.125}{0.32 \cdot 0.5} \cdot 100\% = 78.5\%. \tag{1.28}$$

Therefore, a Class-B PA provides the same output power as Class-A, but with higher collector efficiency of 78.5%.

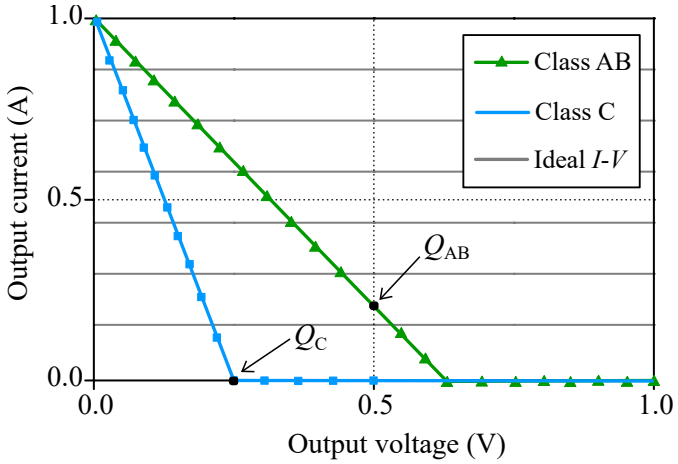


Figure 1.9: Load lines for Class-AB and Class-C power amplifiers.

Class-AB

The bias point can be set in-between the Class-A and Class-B operation, resulting in Class-AB operation shown in Fig. 1.9. The input power is again chosen so that the current swings up to I_{max}. The transistor conducts for more than only half of the period as in Class-B, therefore, the DC current is

$$I_{\text{QB}} < I_{\text{QAB}} < I_{\text{QA}}, \tag{1.29}$$

whereas the collector efficiency is

$$50\% < \eta < 78.5\%. \tag{1.30}$$

Class-C

Even higher efficiencies than Class-B can be achieved by further lowering the bias point so that the transistor conducts for shorter than half of the period of the fundamental signal. This operation is termed Class-C. The load line for this class is shown in Fig. 1.9. The Class-C is highly nonlinear and, therefore, not considered as a linear class of operation, but efficiencies higher than 78.5% can be achieved.

The load resistance R_{load} for each class of operation is chosen such that the maximum output power is achieved, i.e., so that the voltage and current swing up to the maximum allowed values of the active device. This resistance, which results in maximum output power, is termed the optimal load resistance. Interestingly, this load resistance is exactly equal for Class-A and Class-B, whereas for Class-AB, it deviates insignificantly from the Class-A and Class-AB values [15]. Furthermore, all classes except Class-A, require parallel resonant tank at the output to short the voltage harmonics to ground. Only then the maximum efficiencies can be achieved

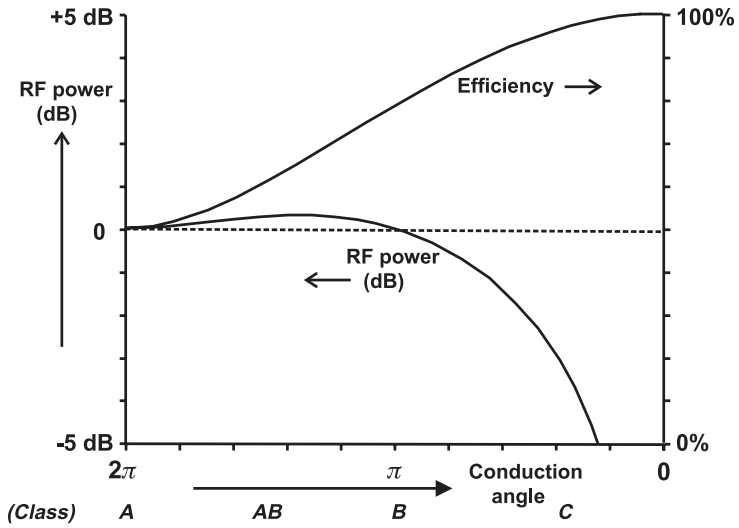


Figure 1.10: Output power and collector efficiency of the Class-A, Class-AB, Class-B, and Class-C, with respect to the Class-A. The load resistance is set at the optimal value and the ideal harmonic short is assumed [15].

in the respective classes. The performance of the four classes regarding the output power and collector efficiency is summarized in Fig. 1.10 [15]. The output power is the same for classes A and B, whereas drops significantly for Class-C. The output power is slightly higher in Class-AB. The classes are sometimes differentiated by the conduction angle; a value which states what fraction of the signal's period transistor conducts current. Thus, for Class-A and Class-B it is equal to 2π and π, respectively.

Therefore, the efficiency of a power amplifier can be increased simply by decreasing the DC current, i.e., by reducing the conduction angle of the transistor. But, once the DC current is lower, the harmonics occur due to the clipping of the current waveform, and the performance degrades since the power is transferred to the harmonics, which is an unwanted effect. To mitigate this, a parallel resonant tank is employed to short the harmonic components of the voltage to ground and, thus, restore the voltage to a pure sine wave. Thus, more efficient classes require additional circuitry at their output, which might become difficult to implement at high frequencies. Nevertheless, the linear classes are still widely used both as a standalone amplifiers, and as a part of advanced PA architectures.

1.3.5 Load-pull

The optimal load resistance is a load resistance for which the maximum output power is achieved. In the simplified schematic shown in Fig. 1.7a, the output of the transistor is represented as a current source and, thus, to achieve maximum output power, the R_{load} should be connected at the output. Regardless of the type of the transistor used, there are significant parasitic reactances associated with the transistor. In that case, the output of the transistor should be matched by the optimal load impedance, Z_{load}, wherein the reactive part of Z_{load} cancels out the reactances

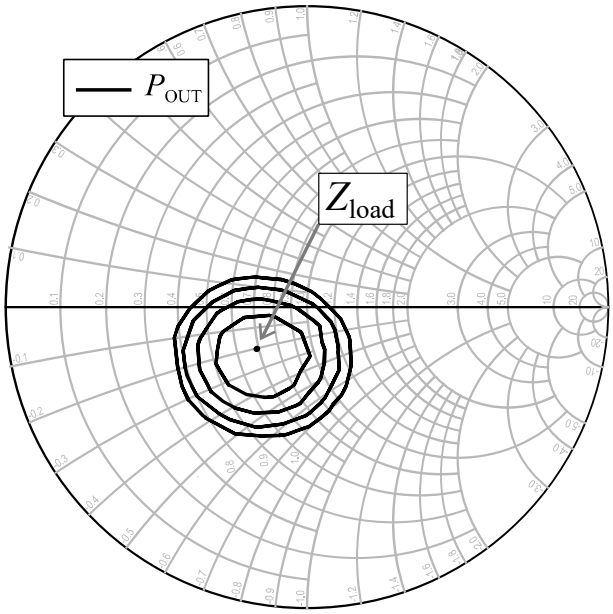


Figure 1.11: Example of a load-pull measurement.

of the transistor. The real part of Z_{load} is the optimal load resistance R_{load}. The difficulty of determining the optimal load impedance lies in the fact that the maximum allowed voltage and current values limit the maximum output power available at the output of the transistor. Additionally, the parasitics of a transistor are highly nonlinear and difficult to analytically take into account. Thus, the optimal load impedance for maximum output power is usually determined by measurements in which the load impedance is varied until the maximum output power is measured. Such measurements are termed load-pull measurements.

Although the small-signal analysis states that for the maximum signal transfer the load should be a complex-conjugate of the impedance of a transistor, the complex-conjugate match does not ensure the maximum output power [15]. For power amplifiers, the load-pull measurements are employed to empirically find the load impedance for which the maximum output power or, in some cases, maximum collector efficiency is achieved. The example results of a load-pull measurement are shown in the Smith chart in Fig. 1.11. The load impedance is varied and the output power is measured. The data is then interpolated so that the lines of equal output power are drawn. Since there is only one Z_{load} for which the maximum output power is achieved, the function has one maximum, which occurs in the center of the lines of equal output power. These lines are termed load-pull contours [15], and they approximate an elliptical shape. The contours provide an information about the change of output power when the load impedance deviates from the optimal value Z_{load}. For the example from Fig. 1.11, the optimal load impedance is $Z_{\mathrm{load}} = 35 - j10\ \Omega$. Therefore, the capacitance of 10 Ω is to cancel the parasitic inductance of the transistor's output.

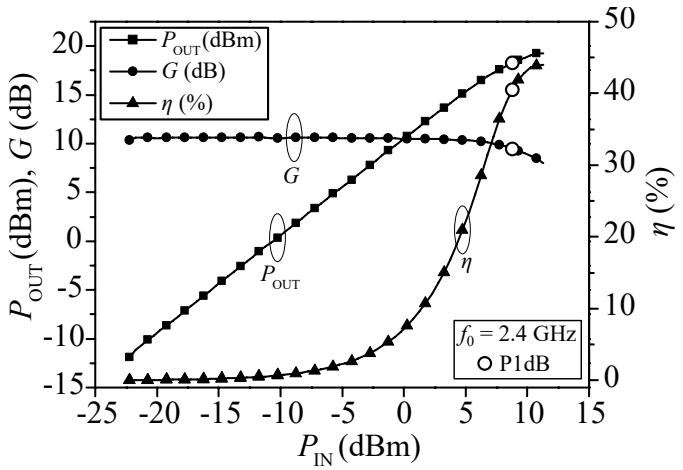


Figure 1.12: Measured performance of a Class-A power amplifier at the fundamental frequency $f_0 = 2.4$ GHz.

1.3.6 Measured performance

The analysis presented so far assumes one level of input power for which the maximum current and voltage swings are achieved. For this input power, both output power and collector efficiency are at their maximum values. The measured performance of a fabricated power amplifier differs somewhat with respect to the simplified analysis of Fig. 1.7a, mainly because the transistor cannot be represented by an ideal current source.

The example of a measured performance of a Class-A power amplifier is shown in Fig. 1.12. The figure shows output power P_{OUT}, gain G, and collector efficiency η, as a function of input power P_{IN}, for a Class-A power amplifier operating at the fundamental frequency f_0 of 2.4 GHz. The output power characteristic comprises two main parts; the linear input power range, in which the linear relationship between the input and output is maintained, and the large-signal region, where the gain compression occurs and the output power does not increase linearly with input power. The gain is constant in the small-signal range, whereas it decreases in the compression region. The input power for which the gain drops by 1 dB (P1dB), is usually taken as the boundary between the linear and compression regions. For the linear classes of operation, a P1dB is the point of maximum output power, above which high nonlinearity occurs and, thus, the PA is not operated.

The collector efficiency shows an exponential increase for low input powers and a maximum in the compression region. Interestingly, the collector efficiency maximum occurs for output power higher than P1dB. The maximum, thus, is seldom reached in normal operation, but still, the efficiency is the highest for the maximum output power of P1dB. Therefore, in the power range of interest, the power amplifier operates with the highest efficiency in P1dB, whereas for lower input power, it drops significantly. As shown in Fig. 1.12, the efficiency in P1dB is 40%, whereas for 3-dB lower input power it is 22%; the collector efficiency of a power amplifier

depends on the power of the input signal. This fact makes power amplifier extremely difficult to design for high efficiency while operating with modern modulated signals.

As shown in Fig. 1.1a, the power of a modulated signal varies in time. The signal shown in the figure has more than 10-dB difference between the peak and average power. This value is termed peak to average power ratio (PAPR) and is important figure of merit for the modern modulated signals. The PAPR is defined as

$$\mathrm{PAPR} = \frac{P_{\mathrm{peak}}}{P_{\mathrm{avg}}}, \tag{1.31}$$

where P_{peak} and P_{avg} are peak and average power of the modulated signal, respectively. The power amplifier from Fig. 1.12 has a collector efficiency of 6% for a 10-dB lower input power with respect to P1dB. Thus, the collector efficiency also varies with time for a modulated excitation. The average collector efficiency is then a proper measure of efficiency for a given input signal, which can be quite low for high-PAPR input signals of 802.11a standard [19]. It should be noted, however, that the efficiency depends on the technology of implementation and architecture of the power amplifier, as shown in the following.

1.4 Efficiency enhancement

The efficiency of the power amplifier directly impacts the end-user experience during wireless communication; by employing more efficient power amplifier, the battery in a handheld device lasts longer. On the other hand, the efficiency of a power amplifier operating in a base station determines the cooling costs needed for a reliable operation. For a power amplifier of high efficiency, the DC dissipation is lower for the same output power, thus, the generated heat is also lower. Since the efficiency is by far the most important parameter of the power amplifiers employed in modern wireless communications, there are specific circuit architectures which maximize the efficiency while, usually, sacrificing the linearity and complexity. There are two main techniques to increase the efficiency of a power amplifier; load modulation and power supply modulation.

1.4.1 Doherty PA

The Doherty power amplifier modulates the load impedance in order to keep the transistor optimally matched both for full output power and for lower output powers [20]. The power range lower than the full output power of a power amplifier is usually termed output power back-off (OPBO).

The simplified block schematic of a Doherty amplifier is shown in Fig. 1.13a. The Doherty comprises two separate power amplifiers, usually Class-AB and Class-C, connected in parallel

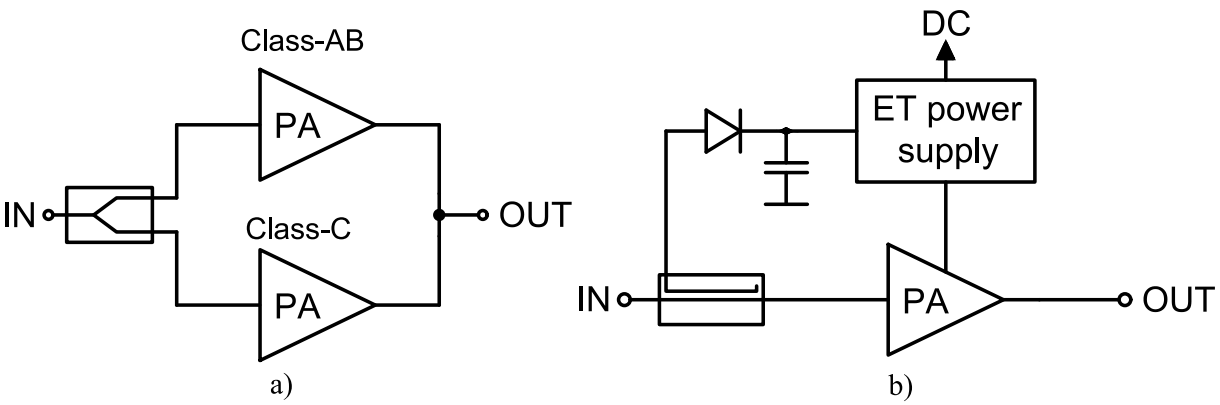


Figure 1.13: Simplified block schematic of (a) Doherty and (b) Envelope Tracking high-efficiency power amplifiers.

at the output. The input signal is split at the input by employing a signal splitter, usually in the form of a hybrid coupler [14], whereas the output signal is combined again at the output. In its most basic form, the Doherty splits the input signal equally, and then the input signals are fed to the power amplifiers. The Class-AB amplifier is configured such that it is active for all values of output power, whereas the Class-C is driven to conduction for higher input powers, which is, for a 3-dB split at the input, at the 6-dB output power back-off. By injecting the signal into the load, the Class-C PA effectively modulates the load impedance presented to the Class-AB PA. This load modulation is configured such that the maximum efficiency is achieved in the entire 6-dB output power back-off range. Therefore, for signals exhibiting PAPR of 6 dB, the ideal symmetrical Doherty provides the maximum efficiency equal to the value achieved for the maximum output power.

1.4.2 Envelope Tracking PA

The efficiency can also be increased by modulating the supply voltage of the power amplifier. Since the supply voltage is set at the value to ensure the maximum voltage swing for the maximum output (input) power, once the input signal power is decreased, the supply voltage can also be decreased to accommodate the reduced swing at the output [21]. In this way, the efficiency is increased by reducing the DC power dissipated by the PA. Such an operation is a characteristic of the Envelope Tracking (ET) architecture, the simplified block diagram of which is shown in Fig. 1.13b. The input signal power is varying in accordance with the envelope of the signal. Thus, to enable the change of the power supply voltage with the input power, the envelope is extracted from the input signal by a directional coupler [14], and fed to the envelope detector. The envelope is the input to the ET power supply, which modulates the supply voltage of the PA in rhythm with the envelope, i.e., the input power. This concept is shown in Fig. 1.14, wherein the carrier signal and its envelope are shown. Due to the large dips in signal power, the requirements on the ET power supply are extremely harsh and their efficiency can be as low as

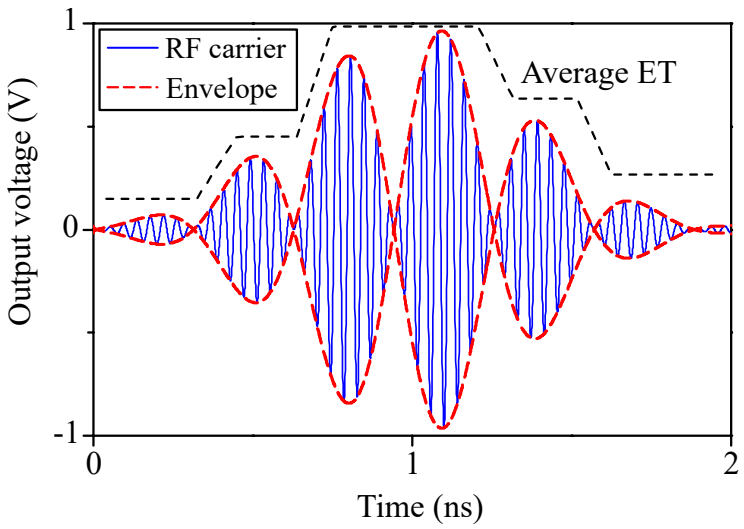


Figure 1.14: The concept of Envelope Tracking power supply.

60%, which then lowers the overall efficiency of the ET power amplifier. The technique termed average Envelope Tracking mitigates this problem by tracking the envelope in discrete steps. But, the possible efficiency increase is lower since the DC power is still wasted in the envelope dips. In the modern transmitters, the envelope is generated in the digital domain, converted to the analog by DACs, and then brought to the input of a fast DC-DC converter which supplies the PA.

1.5 Bandwidth enhancement

The power amplifiers analyzed so far operate with the stated performance at a signal frequency, called carrier or fundamental frequency, as shown in Fig. 1.12. For example, Class-AB, B, and C, amplifiers require the harmonic tank of high quality factor at the output, which, due to a high-Q, exhibits low bandwidth around the fundamental frequency. In other words, the performance of the power amplifier deviates significantly from the optimal performance when shifted away from the fundamental frequency. The matter is even more severe for high-power amplifiers which readily have optimal matching impedances as low as few Ohms. The higher the transformation ratio, the lower the bandwidth of the match [14]. On the other hand, modern modulated signals exhibit bandwidths exceeding 100 MHz [5, 6]. Additionally, handheld devices operate in multiple frequency bands and with signals of different modulations. The result is a separate power amplifier for each wireless communication standard.

To widen the bandwidth of a power amplifier, advanced architectures can be employed, such as a balanced power amplifier [14]. The balanced configuration also comprises two separate amplifiers, which are usually the same. Both the input and output signals are split and combined, respectively, using a coupler. Due to the use of couplers, the inputs and outputs of each amplifier

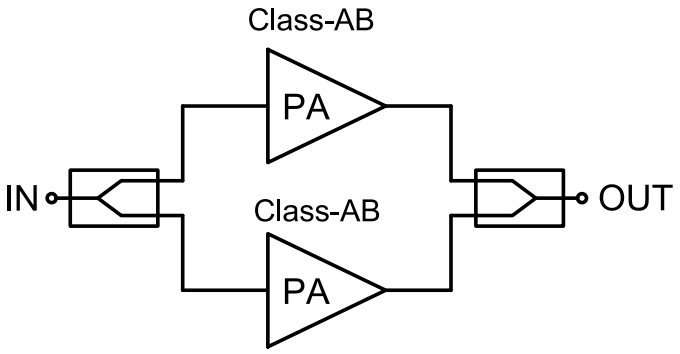


Figure 1.15: Simplified block schematic of a balanced power amplifier.

in a balanced configuration are isolated from each other. The couplers are designed such that the reflections from the input and output of the amplifiers dissipate in the isolated port of the coupler [14]. In this way, the reflected travelling wave is significantly decreased with respect to the incident wave, thus, the input and output match of a balanced configuration is good regardless of the mismatch present between the coupler and the Class-AB amplifiers. The advantage of such a configuration is the possibility to match the transistors to very different impedances than 50 Ω and still retain a good input and output match at the ports of the couplers. Additionally, if one amplifier fails, the balanced configuration continues to operate with a lower performance. Thus, this architecture is popular in applications where high reliability is of great importance [22].

1.6 Transistor technologies for power amplifiers

The performance of a power amplifier depends on the transistor employed. In essence, the role of the input and output matching networks, bias and stabilization networks, is to deliver as much performance as possible out of a given transistor. Many amplifier parameters are that of the transistor itself, e.g., input and output match are better for transistors having base and collector impedances near 50 Ω. Thus, the choice of a transistor technology plays a crucial role in the power amplifier design process.

1.6.1 Evolution of transistor technology

A transistor technology is a semiconductor technology in which a transistor is being processed. Recently, the transistors for power amplifier applications are being made in highly complex semiconductor technologies due to the stringent requirements on the performance of the modern wireless communication circuitry.

The power amplifiers employed in the first generations of wireless communication used silicon (Si) bipolar junction transistors (BJTs) [23]. Then came along Gallium Arsenide (GaAs)

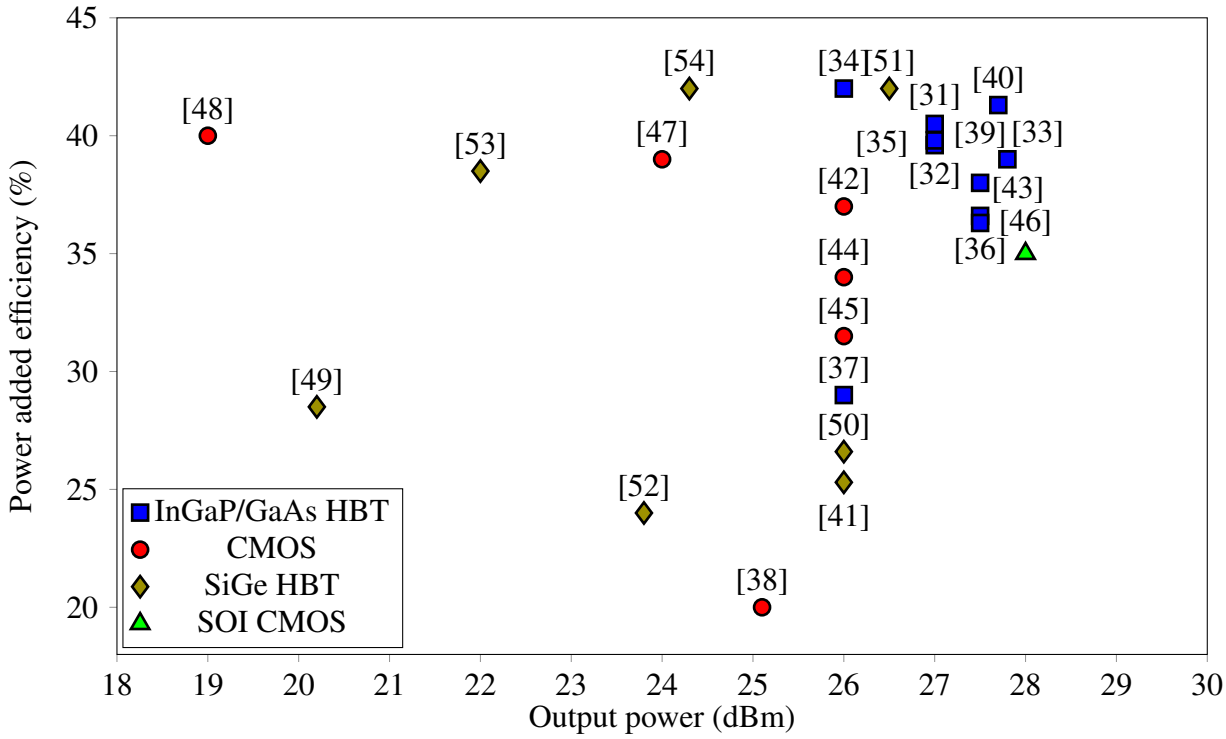


Figure 1.16: Performance of the state-of-the-art power amplifiers implemented in different semiconductor technologies. The results are shown for the 10-MHz-wide 64QAM LTE modulated signal with 7.5-dB PAPR.

material and the GaAs heterojunction bipolar transistor (HBT) [24], which became the technology of choice for low-power applications for handheld devices [15]. For high-power amplifiers used in base stations, laterally diffused MOS (LDMOS) transistors were used [25], and are nowadays replaced by gallium nitride (GaN) high electron mobility transistors (HEMTs) [26, 27, 28, 29, 30]. The LDMOS enabled high output powers but at the cost of operating with low voltages, thus, exhibiting low optimal impedances in the order of few Ohms. The GaN HEMT enabled high output power with high-voltage operation, which increased the optimal impedances close to 50 Ω and made wideband power amplifier design possible.

Today, there is still a gap between the transistor technology used for low- and high-power applications, i.e., handsets and base stations, respectively. Although GaN HEMT is dominating the high-power applications, the power amplifiers for handsets employ transistors processed in very different technologies, depending on the application. For extremely high frequency of operation penetrating the terahertz frequency range, indium phosphide (InP) HBT is the technology of choice [55], whereas for high-end mobile handsets employed in wireless communications of the fourth and fifth generation, silicon germanium (SiGe) HBT is dominating the market [56]. The goal of the industry is to decrease the costs of implementation as much as possible, thus, the complementary MOS (CMOS) is increasingly penetrating the wireless communications market, wherein the output voltage swing is usually increased by stacking multiple

transistors [57]. The performance of power amplifiers processed in several mentioned semiconductor technologies for a 10-MHz-wide LTE signal excitation with 7.5 dB PAPR is shown in Fig. 1.16.

Since a power amplifier exploits the transistor up to its limits, wherein the load line penetrates both the saturation and cut-off regions in order to achieve maximum output power, the device technology parameters directly impact the performance of the amplifier. To that end, an overview of the most important phenomena in bipolar transistors occurring in large-signal operation is given in the following.

1.7 Bipolar transistor for power amplifiers

Most of the transistors used nowadays for high-performance power amplifiers for mobile handsets are of a bipolar type. Furthermore, a low-cost alternative to advanced semiconductor technologies, SiGe, is also popular due to the ease of integration with the digital circuitry implemented in CMOS. Although large-signal operation is a characteristic of a power amplifier, the performance of a transistor in small-signal regime is equally important for the modulated signals excitation, since the average power of the input signal forces the transistor to operate in the back-off power range. Thus, the output power, gain, and efficiency, are equally important in both the small- and large-signal regimes for the performance of a power amplifier.

1.7.1 Small-signal equivalent schematic

To analyze the performance of a bipolar transistor in the small-signal regime, a small-signal equivalent schematic of a bipolar transistor, with the bias point set in the forward active region, is shown in Fig. 1.17, wherein the most important capacitances are included to enable high-frequency analysis [58].

The voltage-dependent current source, $g_{\mathrm{m}}V_{\pi}$, is, in fact, an ideal current source used for the analysis of Fig. 1.7. The current source is a function of the voltage V_{π} developed across the input resistance r_{π}. The term g_{m} is a transconductance, and is given by

$$g_{\mathrm{m}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{T}}}, \tag{1.32}$$

where I_{C} and V_{T} are DC collector current and thermal voltage, respectively. Furthermore, the schematic contains two capacitances; C_{μ} and C_{π}, where the former is the depletion capacitance of the collector-base *pn* junction, and the latter is a total capacitance of the base-emitter *pn* junction. From the equivalent schematic shown in Fig. 1.17, the transition frequency f_{T} can be derived by first calculating the short-circuit current gain in the common emitter configuration h_{fe}, as

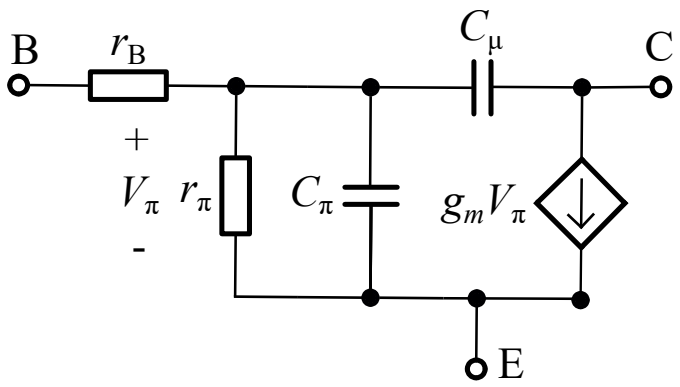


Figure 1.17: Small-signal equivalent (π-hybrid) schematic of a bipolar transistor in the forward active region. The main capacitances are also included to enable high-frequency analysis.

$$h_{\mathrm{fe}} = \frac{g_{\mathrm{m}} r_\pi}{1 + j\omega\left(C_\pi + C_\mu\right) r_\pi}. \tag{1.33}$$

If now the absolute value of h_{fe} is found and equated to 1, the unity-gain bandwidth ω_{T} is calculated as

$$\omega_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{C_\pi + C_\mu}, \tag{1.34}$$

from which the transition frequency f_{T} is found as

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi\left(C_\pi + C_\mu\right)}. \tag{1.35}$$

The transition frequency is a characteristic of a transistor, and it is an estimate of the performance which is available for a given device and technology process. Another important performance parameter of a bipolar transistor is a maximum frequency of oscillation, f_{max}. The f_{max} is a measure of a maximum power gain available from the device, and it is derived by finding the output impedance of the schematic shown in Fig. 1.18, and then matching the output by its complex conjugate. The maximum frequency of oscillation is then given by

$$f_{\mathrm{max}} = \sqrt{\frac{f_{\mathrm{T}}}{8\pi C_{\mathrm{bc}} r_{\mathrm{b}}}}. \tag{1.36}$$

Therefore, a transistor with smaller C_{bc}, higher f_{T}, and smaller r_{b}, exhibits higher f_{max} and, thus, can achieve higher gain when operated in a power amplifier in the back-off input power range.

The transition frequency and maximum frequency of oscillation depend on the bias, since (1.35) and (1.36) are given for a predetermined bias point. The dependence of f_{T} and f_{max} on DC collector current I_{C} is shown in Fig. 1.18. Both have a maximum for a certain value of

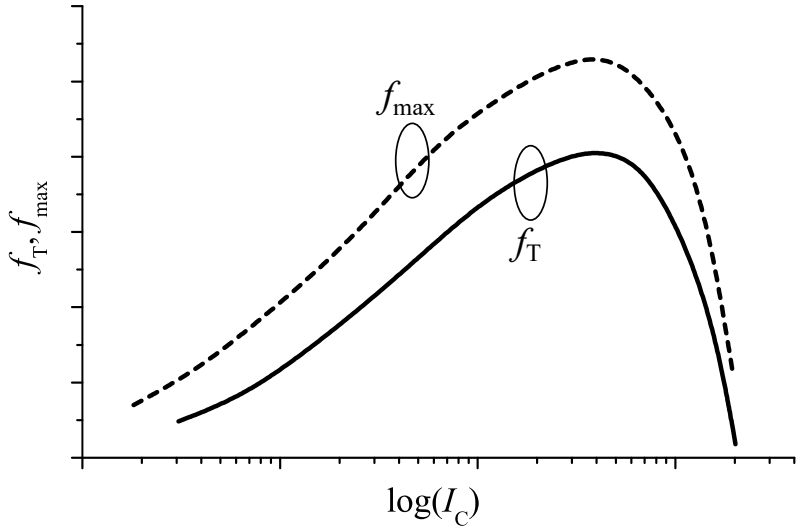


Figure 1.18: Dependence of transition frequency f_T and maximum frequency of oscillation f_{max} on DC collector current I_C.

collector current, which is significant when choosing the bias point for an amplifier. On the other hand, since the value of bias current depends on the power of the input signal in power amplifiers, the small-signal parameters vary with time and give rise to nonlinearity in the small-signal back-off power range. The nonlinearity arising in the back-off power range is due to the fact that the small-signal parameters of the equivalent schematic are constantly changing, but the nonlinearity arising in the large-signal operation arises due to a large voltage and current swing at the terminals of the transistor.

1.7.2 Large-signal equivalent schematic

The large-signal DC model of a bipolar transistor is shown in Fig. 1.19a. The collector current i_C is a function of the base-emitter voltage v_{BE} according to

$$i_C = I_S \exp \frac{v_{BE}}{V_T}, \tag{1.37}$$

where I_S is the saturation current of a *pn* junction. Although the collector current depends exponentially on the base-emitter voltage, it is linearly dependent on the base current I_B through the common-emitter DC current gain β as

$$\beta = \frac{I_C}{I_B}. \tag{1.38}$$

The exponential characteristic of collector current on base-emitter voltage is shown in Fig. 1.19b. Interestingly, this is the main difference with respect to MOS transistors and, thus, impacts the behaviour of the transistor in large-signal operation. This impact can be analyzed by applying a base-emitter voltage v_{BE} of large enough amplitude so that the voltage swing covers both the

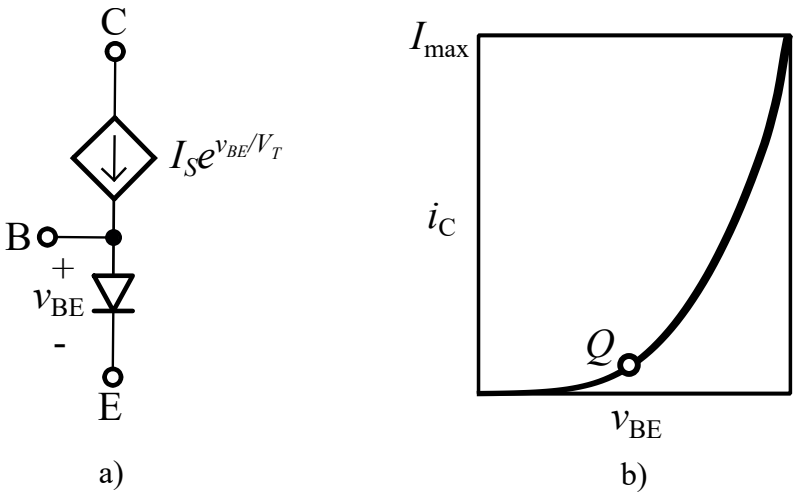


Figure 1.19: (a) Large-signal DC model and (b) transfer characteristic of a bipolar transistor in the forward active mode.

off and on regions of the exponential characteristic of Fig. 1.19b. Furthermore, this voltage is applied in Class-AB bias point Q to analyze the impact of the entire exponential characteristic on the collector current. Additionally, it is assumed that the base-emitter voltage is applied by an ideal voltage source with zero resistance, so that the ideal sine wave is applied directly across the base-emitter junction. The analysis is performed according to [15].

If a sine wave base-emitter voltage v_{BE} is applied, given by

$$v_{\mathrm{BE}} = V_{\mathrm{Q}} + V_{\mathrm{s}} \cos \omega t, \tag{1.39}$$

where V_{Q} and V_{s} are base-emitter DC value and amplitude, respectively, then the output power for the optimal load resistance is shown in Fig. 1.20. The collector current is calculated by replacing the v_{BE} in (1.37) with (1.39). Then, the output power is calculated for each value of v_{BE} by matching the transistor with the optimal load resistance. The case where V_{Q} is the highest (top curves) represents a Class-A operation, wherein a slight gain expansion is observed for higher input power. For lower bias voltage, the bias point is lowered into the Class-AB and the expansion becomes more pronounced, and it is the highest for deep Class-AB bias condition (the lowest V_{Q}). Therefore, a bipolar transistor, represented by an ideal large-signal equivalent schematic of Fig. 1.19a, when driven by a sinusoidal voltage exhibits an output power characteristic with a gain expansion before the compression region. This is due to the exponential characteristic of the base-emitter *pn* junction and such effect is, therefore, not observed in MOS transistors [15]. Although the effect is a deviation from the ideal characteristic, a gain expansion is much easier to correct than the gain compression. Furthermore, this trait of a bipolar transistor is readily exploited in power amplifiers to achieve a cancellation of the intermodulation products and, therefore, the increase in the linearity of the amplifier [59]. Thus, the gain of the power amplifier depends on both the small- and large-signal parameters of a bipolar transistor,

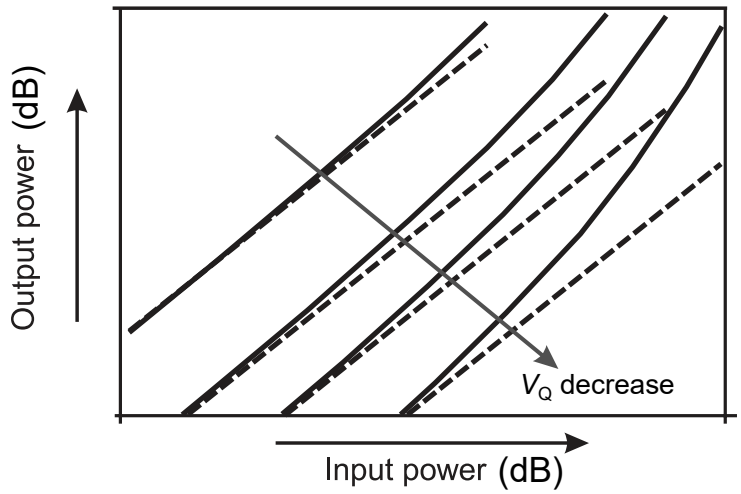


Figure 1.20: Output power of a bipolar transistor excited by a large-signal base-emitter voltage for the optimal matching resistance at the collector [15]. Both linear responses (dashed) and calculated from (1.37) and (1.39) (solid) shown for different DC base-emitter voltages V_Q.

but the output power is determined solely from the large-signal characteristics of the transistor. To that end, the output DC characteristics of a bipolar transistor are next explained.

1.7.3 Output DC characteristics

In the previous analysis, the output of a transistor has been presented with an ideal current source, as shown in Fig. 1.7a. To reach the maximum output power for a given bipolar transistor, a maximum current and voltage swing at the output should be known in order to determine the optimal matching impedance correctly. These limits in bipolar transistors are maximum collector current and maximum collector-emitter voltage. Therefore, to facilitate the analysis of the maximum swing at the collector, the output DC characteristics of a bipolar transistor are shown in Fig. 1.21.

The output characteristics are different with respect to an ideal current source in two aspects. Namely, the collector-emitter voltage swing is limited in the low end by the saturation region, i.e., saturation voltage V_{CEsat}, and on the other end, by the breakdown region. Thus, the two are usually the limits of the maximum voltage swing at the collector of a bipolar transistor in large-signal operation. On the other hand, the maximum current swing is limited by the thermal constraints of a transistor, but also by the second-order effect occurring at high collector currents, termed Kirk effect [60].

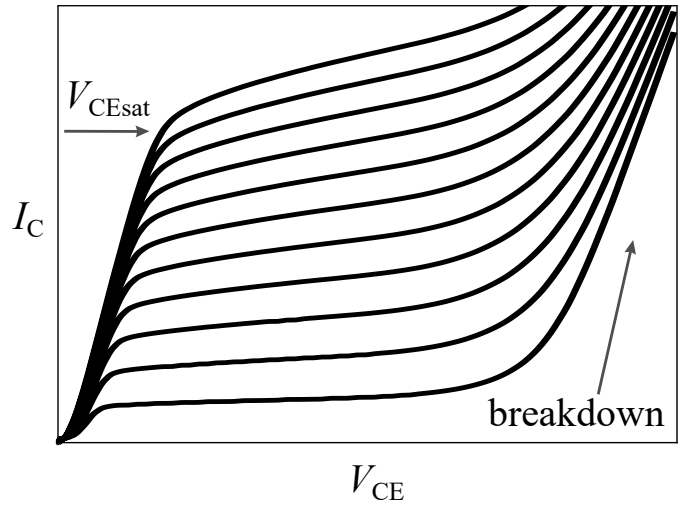


Figure 1.21: Output I_C-V_{CE} characteristics of a bipolar transistor in the common-emitter configuration. The effects limiting the collector-emitter voltage swing shown.

Kirk effect

At sufficiently high collector currents, the behaviour of bipolar transistors starts to deviate from the ideal characteristics due to the high-injection effects. The most important high-injection effect in Si bipolar transistors is Kirk effect [60]. For a certain value of collector current, the minority carrier concentration in the collector-base (CB) region becomes equal to the doping-induced charge in the CB space-charge region. The space-charge region then collapses and moves deeper into the collector region [61]. This displacement effectively increases the width of the base, which decreases both β and f_T due to

$$I_C \propto 1/W_b, \tag{1.40}$$

and

$$\tau_b \propto 1/W_b^2, \tag{1.41}$$

where W_b and τ_b are width of the base and base transit-time, respectively [61]. The estimate of the collector current for which Kirk effect occurs is calculated for the condition when the built-in electric field in the CB region becomes zero. The resulting expression is [61]

$$I_{C,Kirk} \approx q v_s N_{dc} \left\{ 1 + \frac{2\varepsilon \left(V_{CB} + \phi_{bi} \right)}{q N_{dc} W_{epi}^2} \right\}, \tag{1.42}$$

where v_s, N_{dc}, V_{CB}, ϕ_{bi}, and W_{epi}, are saturation velocity, collector doping concentration, collector-base voltage, built-in potential of the CB junction, and the thickness of the collector epi-layer, respectively. To increase the current for which Kirk effect takes place, the collector is doped

to a higher concentration. The same action, on the other hand, lowers the region of impact ionization, i.e., the breakdown voltage.

Impact ionization

For high enough collector-emitter voltage, a breakdown of the CB junction occurs, and the collector current rises sharply, as shown in Fig 1.21. The physical phenomena responsible for the breakdown is impact ionization, also termed avalanche multiplication [61].

Since the CB junction is reverse biased in forward active region, the electric field becomes high for high reverse voltage across the CB junction. The electrons traversing the CB space-charge region can attain high enough energy to create additional electron-hole pairs by colliding with the lattice. Such a generation process is called impact ionization, and, if the newly generated carriers generated even more carriers, the process is termed avalanche multiplication. The result is a sharp increase in collector current for high collector-base reverse voltages. In other words, the current entering the CB space-charge region is lower than that leaving the region, and the ratio is termed multiplication factor M, given by [61]

$$M = \frac{I_{\text{n,out}}}{I_{\text{n,in}}}, \tag{1.43}$$

where $I_{\text{n,out}}$ and $I_{\text{n,in}}$ are currents leaving and entering the CB space-charge region, respectively. The parameter M is usually employed to determine the breakdown voltages in bipolar transistors. For example, the open-emitter breakdown voltage, BV_{CBO}, can be found by fitting the measured data according to

$$M = \frac{1}{1-(V_{\text{CB}}/\text{BV}_{\text{CBO}})^m}, \tag{1.44}$$

where BV_{CBO} and m are fitting parameters. Similarly, the open-base breakdown voltage, BV_{CEO}, occurs for much smaller value of M, which is given by

$$M - 1 = \frac{1}{\beta}, \tag{1.45}$$

where β is DC current gain in common-emitter configuration. In other words, the BV_{CEO} is lower than BV_{CBO} since the former is measured with the base open, and the avalanche multiplication is triggered by the CB junction leakage current I_{CB0}, which now cannot flow out of the base. The I_{CB0} flows through the emitter which then causes a positive feedback loop wherein the I_{CB0} is amplified by β.

Thus, the BV_{CEO} is the relevant breakdown voltage when the base sees an open circuit at DC. Since seldom in circuit application is a bipolar transistor employed with the current source

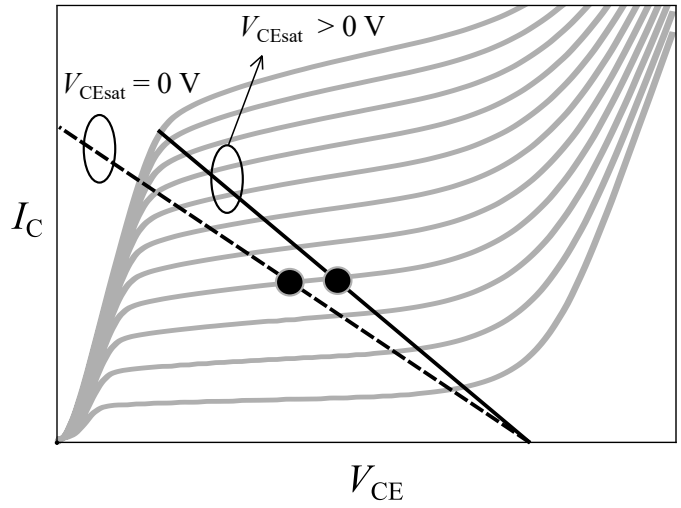


Figure 1.22: The impact of saturation voltage V_{CEsat} on the load line swing in Class-A operation. The dots show the bias points for the respective load lines.

in the base circuit, the breakdown voltage can be increased from the BV_{CEO} value if there is a finite resistance in the base-emitter circuit at DC. This breakdown voltage is then termed BV_{CER}. The matter is further complicated by a different impedance at RF, and this is then the relevant impedance which determines the breakdown voltage experienced by the RF signal at terminals of the transistor. Nevertheless, a breakdown voltage is usually taken as the limit of the maximum collector-emitter voltage swing at the collector reference plane.

1.7.4 Maximum voltage and current swing

Therefore, the collector-emitter voltage swing is limited by both the saturation voltage V_{CEsat} and the relevant breakdown voltage. On the other hand, the collector current swing is limited by the Kirk effect, which can be estimated from (1.42). The impact of V_{CEsat} on the output power is given by

$$P_{OUT} = \frac{1}{2}(V_{BR} - V_{CEsat}) I_{C,kirk}, \tag{1.46}$$

where V_{BR} is the relevant breakdown voltage for a given circuit application. To illustrate the decrease in output power due to the impact of the breakdown voltage, the following short example is given. If $V_{BR} = 5$ V, $I_{C,kirk} = 100$ mA, and $V_{CEsat} = 0.5$ V, the output power is

$$P_{OUT} = \frac{1}{2}(5 - 0.5)\,0.1 = 225 \text{ mW}, \tag{1.47}$$

whereas for $V_{CEsat} = 0$ V,

$$P_{\mathrm{OUT}} = \frac{1}{2} \cdot 5 \cdot 0.1 = 250 \text{ mW}. \tag{1.48}$$

The impact on collector efficiency is more severe since, for the case when $V_{\mathrm{CEsat}} = 0.5$ V, the DC collector-emitter voltage in bias point is even higher than for the ideal case, as shown in Fig. 1.22. Thus, the output power is decreased and the DC power dissipated is increased, which further decreases the collector efficiency.

1.8 Horizontal Current Bipolar Transistor (HCBT)

Although many different transistor technologies are employed for the design of power amplifiers for wireless communications, the performance is usually increased by adopting a costlier process [see Fig. 1.16]. The Horizontal Current Bipolar Transistor (HCBT) is a new structure of a bipolar transistor which provides both the low cost and high performance suitable for modern wireless communications.

The HCBT outperforms other lateral bipolar transistors (LBTs), but inherits their benefits, such as low volume of parasitic parts [62]. The transistor is fabricated by a simpler process since it does not require a few process steps mandatory in vertical bipolar junction transistor processing, such as n^+ buried layer, epitaxial growth, base polysilicon layer, emitter-base spacers, collector plug implantation, and deep trench isolation. Furthermore, such a simple process enables a straightforward integration with the CMOS, providing a low-cost and high-performance BiCMOS process. The integration of the HCBT is done through the cooperation with the Asahi Kasei Microdevices Corp. from Japan. The integration with a 180-nm CMOS is accomplished by adding two or three additional lithography masks on top of the CMOS baseline process. The f_{T} and f_{max} of 51 GHz and 61 GHz, respectively, are achieved for the device with the optimal collector. Additionally, the open-base breakdown voltage $\mathrm{BV_{CEO}}$ is 3.4 V for the optimal device design [63]. This performance makes the HCBT the fastest reported pure-silicon bipolar transistor with an implanted base [64].

1.8.1 HCBT fabrication

The CMOS process used for the integration of HCBT provides 6 aluminum layers, and poly-poly and metal-metal capacitor modules [62, 65]. The HCBT is integrated by employing a base-after-gate integration scheme, which features gate oxide thickness of 3 nm and 7 nm for 1.8 V and 3.3 V supply voltage, respectively. The fabrication sequence of the HCBT with a single polysilicon region is shown in Fig. 1.23. The first step is the Shallow Trench Isolation (STI) process for the fabrication of 350-nm-deep trenches for the device isolation. The active device is defined at the side-walls defined by the STI step. Next, a series of standard CMOS

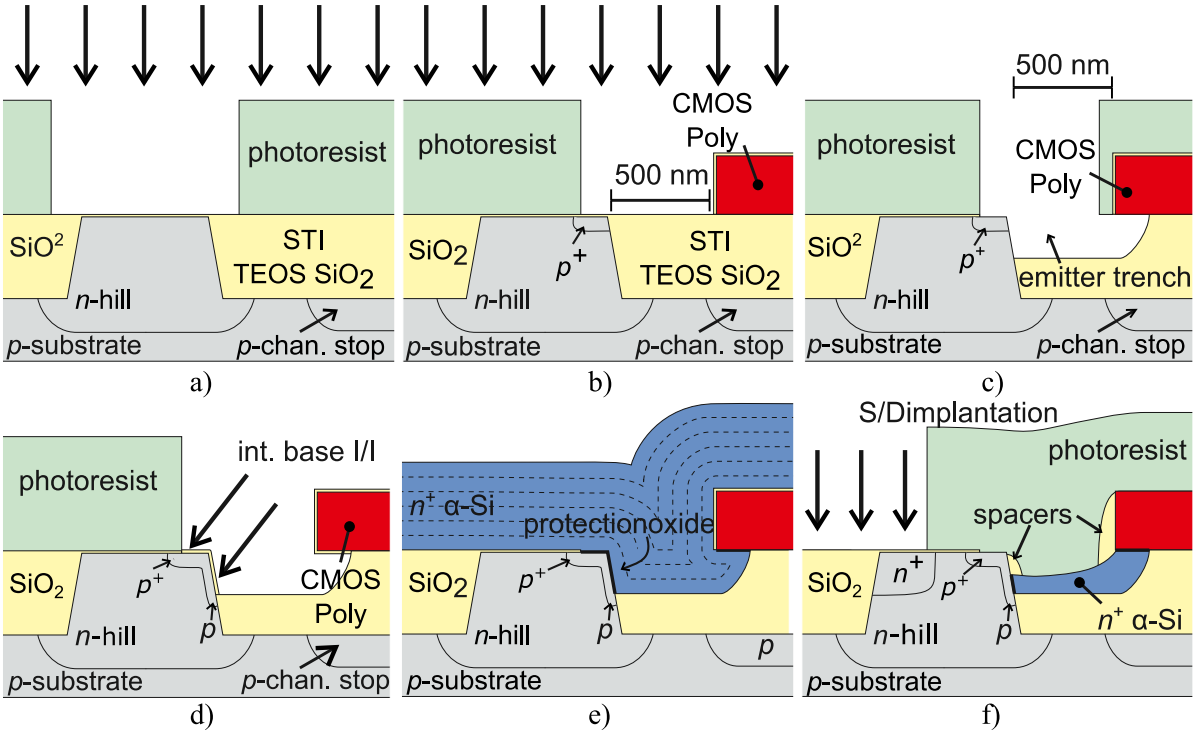
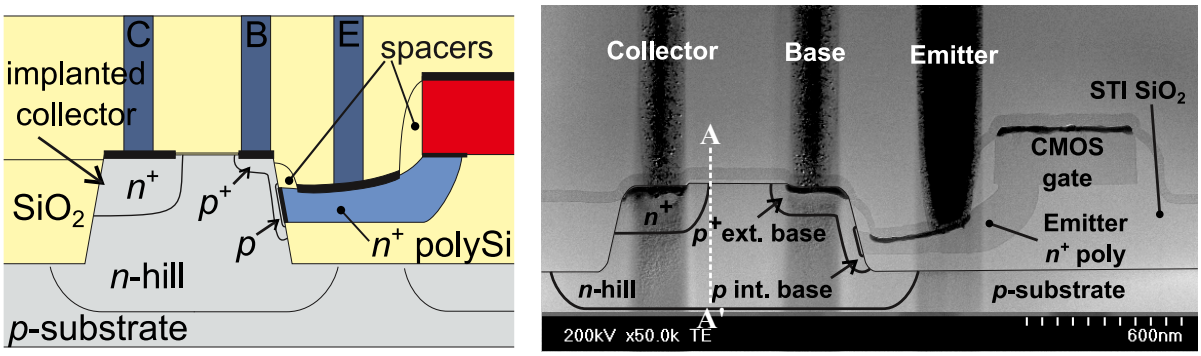


Figure 1.23: Fabrication sequence of HCBT with a single polysilicon region. [63, 65]. (a) Definition of the n-hill collector, (b) extrinsic base implantation, (c) oxide etching and emitter trench definition, (d) intrinsic base implantation, (e) deposition of α-Si, (f) definition of n^+-collector region.

steps are carried out, such as n-well and p-well definitions, threshold voltage adjustment, and punch-through protection. Then, the first HCBT mask is employed for the implantation of the n-hill collector region, as shown in Fig. 1.23a. For this stage, a three-step phosphorous implantation with the energies of 340 keV, 220 keV, and 110 keV, is used. The processed area is the region of the intrinsic collector of the HCBT, whose collector doping profile impacts the most important performance parameters, such as f_T, f_{max}, and BV_{CEO}. Thus, this process step can be tweaked in order to achieve a desired high-frequency performance. This step can be even skipped to achieve further reduction in processing cost, wherein the collector region is defined by the CMOS n-well step. Finally, the CMOS annealing steps are utilized without any impact on the CMOS thermal budget [65].

After the annealing, the standard CMOS process continues with the gate oxide and polysilicon processing, followed by the gate re-oxidation and source/drain extensions implant. The second HCBT mask is then used for the extrinsic base implantation, as shown in Fig. 1.23b. In most cases, the extrinsic base is implanted by difluoroboron (BF_2) at an angle of 0° and energy of 20 keV. This mask determines the distance between the extrinsic base and the n^+ collector, and it also determines the extrinsic base width. Next, the extrinsic base implants are annealed together with the CMOS extension implants, thus keeping the CMOS thermal budget unchanged. The oxide etching and emitter trench definition are the next steps which are implemented by the third HCBT mask [see Fig. 1.23c]. The etching leaves a 100-nm-thick oxide,



a) b)

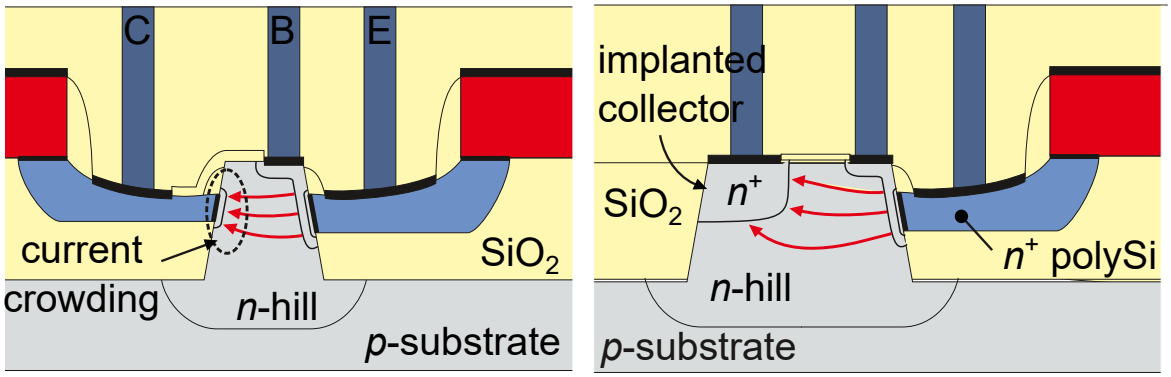
Figure 1.24: Cross-section (a) and TEM micrograph (b) of the HCBT with a single polysilicon region [66].

wherein only the active *n*-hill side-walls are exposed, whereas the side-walls on the collector side, front and back, are surrounded by the oxide. After the photoresist removal, thin screening tetraoxysilane (TEOS) oxide is deposited over the whole wafer to serve as a protection layer during the intrinsic base implantation. The base implantation is performed by reusing the second HCBT mask, as shown in Fig. 1.23d, wherein the implantation is done at 30° and 35 keV by BF_2.

The polysilicon emitter formation is next performed. The TEOS is removed by dipping the wafer into the hydro-fluoric (HF) acid. The base implants are then activated by the rapid thermal annealing (RTA) process, which, additionally, creates a thin native oxide on the *n*-hill side-walls. This oxide serves as a barrier layer for the subsequent tetramethylammonium hydroxide (TMAH) etching step. Firstly, the RTA is followed by the deposition of a 450-nm-thick *in-situ* doped amorphous-silicon (α-Si), which fills the emitter trench, as shown in Fig. 1.23e. Next, a time-controlled etching in TMAH is carried out to achieve a desired polysilicon thickness in the emitter trench [see Fig. 1.23f]. The *n*-hill is protected by the native oxide grown during the RTA step. The CMOS gate facilitates the shaping of the emitter n^+ polysilicon region during the TMAH etching step [62, 65].

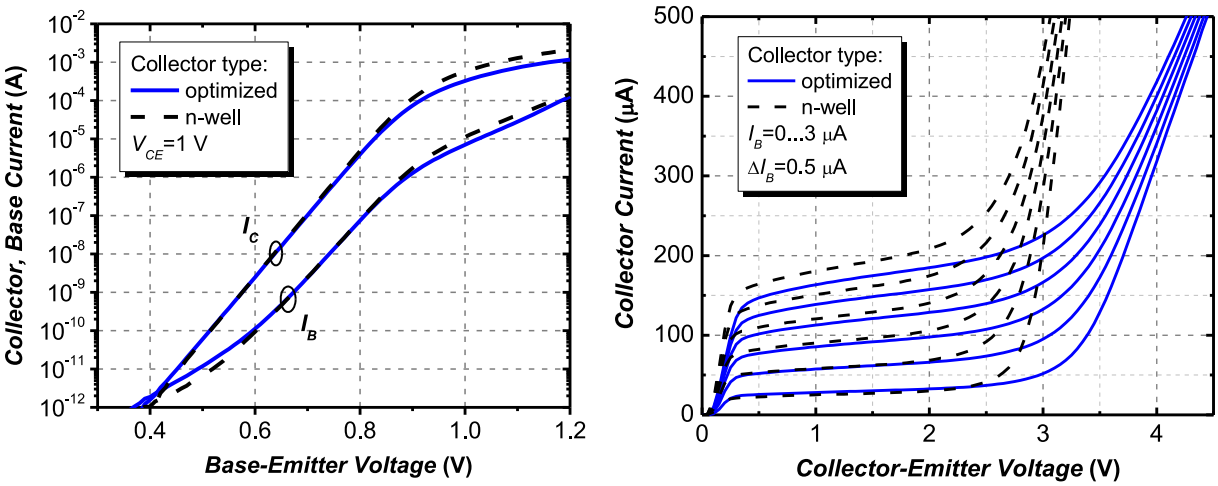
The CMOS spacers are then deposited by lightly-doped drain (LDD) oxide deposition. The anisotropic etching of that oxide leaves the *n*-hill side-walls protected by the oxide spacers. Next, the n^+ collector region is defined along with the CMOS source and drain implantations, as shown in Fig. 1.23f. The final RTA step defines the intrinsic emitter region, which is the result of the diffusion from the n^+ polysilicon region into the *n*-hill [65].

Finally, the contacts are formed. The oxide is deposited to serve as a blocking mask for the silicide, a standard step in the CMOS process. The oxide is removed from the contacts area, but it is kept between the extrinsic base and the implanted n^+ collector to prevent the collector-base shorts. Next, the cobalt is deposited and the silicide is formed, after which the thick oxide is deposited, the holes for the metallization are opened in the oxide, and the step is finished by the



a) b)

Figure 1.25: Cross-section of (a) double-poly and (b) single-poly HCBT. The electron flow from the emitter to the collector is depicted by the arrows [67].



(a) (b)

Figure 1.26: Measured (a) Gummel plot and (b) output characteristics of the single-poly HCBT with optimal (solid) and *n*-well (dashed) collector. Emitter area of both transistors is $0.1 \cdot 1.8\ \mu\text{m}^2$ [62].

metallization process [65]. The cross-section of the final HCBT structure and its transmission electron microscopy (TEM) photograph, are shown in Fig. 1.24.

1.8.2 HCBT electrical characteristics

The HCBT technology offers different varieties of the novel bipolar transistor. Furthermore, the semiconductor processes employed for the complex circuitry of modern wireless communications, usually offer both the high-speed and high-voltage devices, along with the medium-performance devices which offer the best of the both worlds. In the same manner, there are high-speed and high-voltage HCBTs in the BiCMOS process, thus, the technology can satisfy many different requirements of radiofrequency front-ends in wireless communications.

The development of the HCBT first led to a device with two polysilicon regions [68], whereas the single-poly device represents the high-speed version which is an upgrade of the

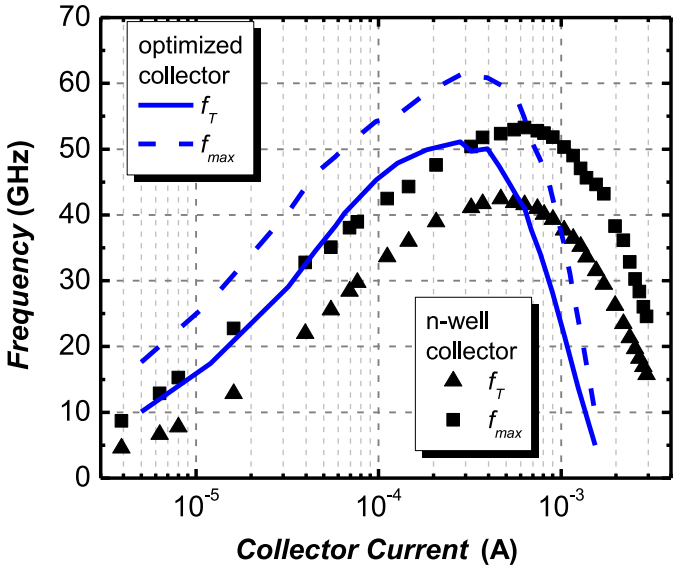


Figure 1.27: Cut-off frequency f_T and maximum frequency of oscillations f_{max} as a function of collector current I_C for the single-poly HCBT with the optimized and n-well collector. Emitter area is $0.1 \cdot 1.8\ \mu m^2$ and collector-emitter voltage V_{CE} is 2 V [63].

double-poly HCBT. The collector region of the double-poly HCBT is fabricated in the same step as the emitter region, and differences in polysilicon thickness arise due to the extrinsic base implantation which damages the isolation oxide. Thus, the polysilicon thickness is larger on the emitter side, i.e., 120 nm and 90 nm on the emitter and collector, respectively [67].

The geometrical differences between the single-poly and double-poly devices are depicted in Fig. 1.25. Since the collector contact is formed on the n-hill in the single-poly HCBT, the n-hill has to be wider to accommodate the contact. Furthermore, the effective collector area is wider in the single-poly HCBT, and the current spreads in the vicinity of the n^+ region. This is the advantage of the single-poly with respect to the double-poly HCBT. Namely, the collector area is much smaller in the double-poly device and the current crowding effect takes place, which causes the onset of Kirk effect at much lower collector currents. Additionally, the double-poly device exhibits larger collector-base capacitance due to the smaller distance between the extrinsic base region and the n-hill edge, in comparison to the single-poly HCBT.

The performance of the two versions of the HCBT differ due to the aforementioned structural differences. Namely, the single-poly HCBT achieves f_T and f_{max} of 51 GHz and 61 GHz, respectively, whereas the double-poly version achieves 34 GHz and 45 GHz, respectively. Additionally, the peak of f_T occurs at a lower current of 180 μA, with respect to 280 μA for the single-poly HCBT [67].

The performance of a single-poly HCBT can be optimized by engineering the collector region and its vertical doping profile. To that end, the characteristics of HCBTs with both the optimized and n-well collector are shown in Fig. 1.27. The optimized collector is designed to achieve an uniform electric field in the collector-base depletion region. This provides the opti-

Table 1.2: Measured electrical parameters of the single-poly HCBT (optimized and *n*-well collector) and the double-poly HCBT [63, 67].

	single-poly		double-poly
	optimized	*n*-well	
Emitter area	$0.1 \cdot 1.8\ \mu\text{m}^2$		
Peak β	72	76	72
BV_{CBO} (V)	9.5	8.3	8.6
BV_{CEO} (V)	3.4	2.8	3.4
V_{A} (V), $I_{\text{B}} = 5\ \mu\text{A}$	10	11	10
C_{BC} (fF), $V_{\text{CE}} = 1$ V	1.1	1.6	1.5
f_{T} (GHz), $V_{\text{CE}} = 2$ V	51	43	34
f_{max} (GHz), $V_{\text{CE}} = 2$ V	61	53	45
$f_{\text{T}} \cdot \text{BV}_{\text{CEO}}$ (GHzV)	173	120	116

mal trade-off between the breakdown voltage BV_{CEO} and the transition frequency f_{T} [63, 66]. On the other hand, the HCBT with an *n*-well collector reuses the CMOS *n*-well mask, which provides a retrograded doping profile in the collector. Although it exhibits a somewhat lower performance regarding f_{T} and f_{max}, the *n*-well collector further reduces the cost of fabrication since it does not need a separate collector implantation mask.

The main performance parameters are given in Tab. 1.2. When comparing the devices with the optimized and *n*-well collector, both transistors have similar β of around 70, whereas the *n*-well HCBT has a lower BV_{CEO} of 2.8 V, compared to 3.4 V for the optimized collector. This is the result of the higher collector doping concentration due to the retrograded doping profile in the *n*-well HCBT. The product $\text{BV}_{\text{CEO}} \cdot f_{\text{T}}$ equals 173 GHzV, which is close to the theoretical Johnson's limit [69]. Additionally, the collector-base capacitance is around 0.8 fF/μm, whereas the Early voltage is also relatively low since the devices are optimized for high-frequency performance [62].

Additionally, device designs which exhibit high breakdown voltages are also developed and fabricated, which enables the applications in high-voltage regimes wherein high-frequency performance is of a lesser importance. The high-voltage device is a double-emitter (DE) HCBT [70, 71], fabricated in the same process flow as the high-speed single-poly HCBT, and it does not need additional lithography masks. This enables seamless integration with the existing BiCMOS process. The device consists of two active transistor regions on the *n*-hill side-walls opposite to each other. The intrinsic base and emitter are, thus, placed opposite to each other in the *n*-hill, whereas the intrinsic collector is shared in the middle. The extrinsic bases are merged

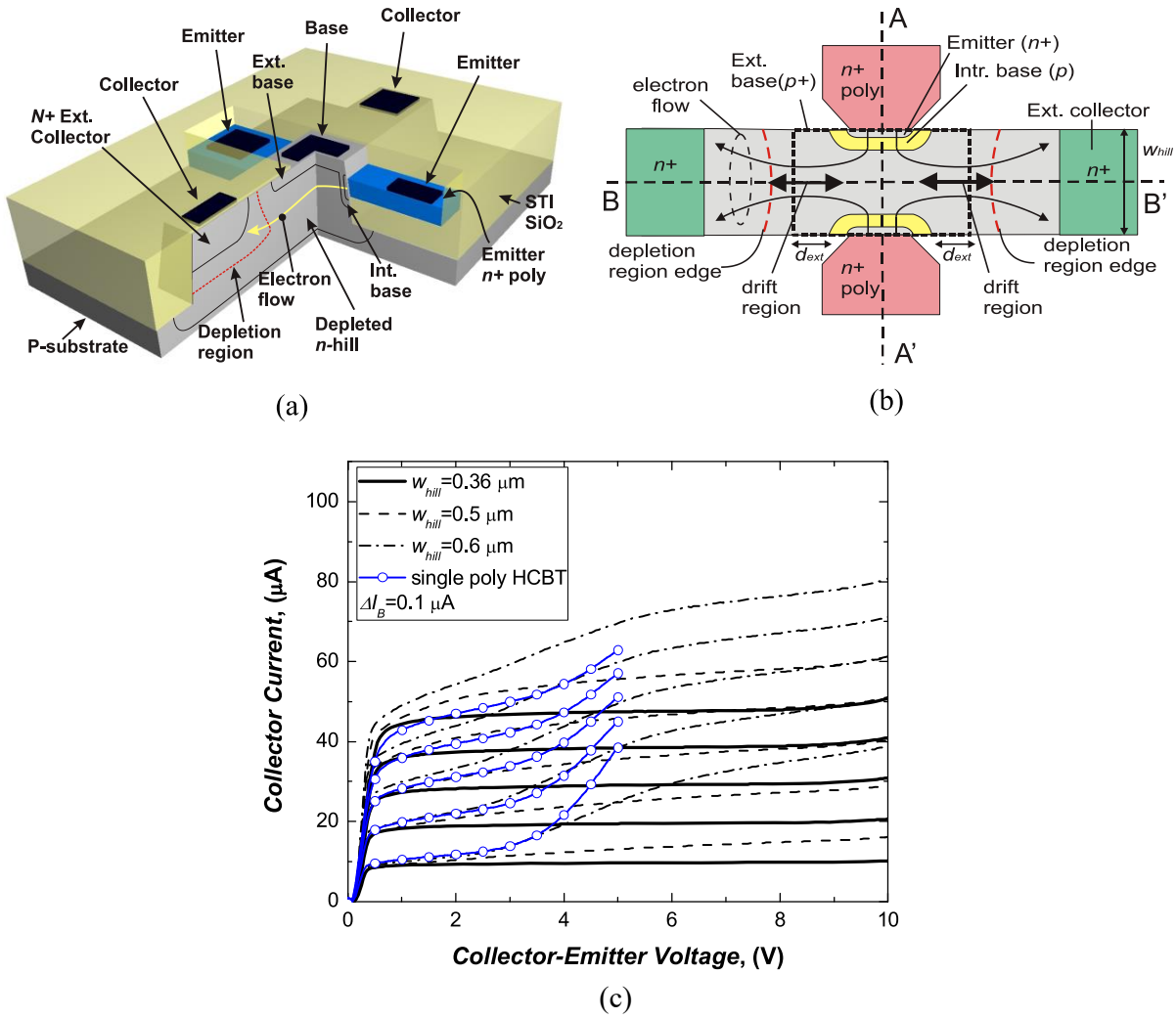


Figure 1.28: (a) 3D cross-section, (b) horizontal cross-section, and (c) measured output characteristics, of the double-emitter (DE) HCBT [65, 70]. Electron flow direction and depletion region boundary shown in (b). Output characteristics for the single-poly HCBT shown in (c) for reference.

on top of the *n*-hill. The extrinsic collector is fabricated laterally in the front and the back of the intrinsic transistor. The intrinsic collector is, thus, surrounded by p^+ extrinsic base from the top, two intrinsic bases from the left and right, and by the *p*-substrate from the bottom [70], as shown in Fig. 1.28a,b. The collector is fully depleted by the applied reverse base-collector voltage. For relatively high voltages, the maximum occurs in the middle and does not depend on the magnitude of the voltage, but the drift region supports the rest of the voltage drop [65].

The measured characteristics of the double-emitter HCBT are shown in Fig. 1.28c. The device exhibits high Early voltage of 301 V for the extrapolation between the collector-emitter voltages of 5 V and 8 V, and for $I_\mathrm{B} = 5\ \mu\mathrm{A}$. Along with the β of 95.4 V at $V_\mathrm{CE} = 5\ V$, the DE HCBT provides a $\beta \cdot V_\mathrm{A}$ product of 28700 V, where both the $\mathrm{BV_{CEO}}$ and V_A are improved with respect to single-poly HCBT. This is the result of the 3D charge sharing effect present in the collector of the DE device. The main electrical parameters of the DE HCBT are summarized in Tab. 1.3. Since the device is designed for high-voltage operation, it does have lower f_T and

Table 1.3: Measured electrical parameters of the double-emitter (DE) HCBT of two different *n*-hill widths [70].

	DE HCBT	
	$w_{\text{hill}} = 0.5\ \mu\text{m}$	$w_{\text{hill}} = 0.36\ \mu\text{m}$
Emitter area	$2 \cdot (0.1 \cdot 1.3)\ \mu\text{m}^2$	
Peak β	104	94
BV_{CBO} (V)	11.2	12.9
BV_{CEO} (V)	11.6	12.6
V_{A} (V)	75	301
f_{T} (GHz), $V_{\text{CE}} = 2$ V	13.6	12.7
f_{max} (GHz), $V_{\text{CE}} = 2$ V	29.5	28
$f_{\text{T}} \cdot \text{BV}_{\text{CEO}}$ (GHzV)	158	160
$\beta \cdot V_{\text{A}}$ (V), $V_{\text{CE}} = 2$ V	7800	28700

f_{max} with respect to single-poly HCBT. Additionally, a current crowding effect takes place in the middle of the DE structure, which causes the onset of Kirk effect at a lower collector current, whereas electron travel through the larger depletion region thus increasing the transit time. Both effects contribute to lower high-frequency performance [70, 71].

On the other hand, the breakdown voltage is further increased up to 36 V by shielding the electric field in the drift region; the result is a reduced-surface-field (RESURF) double-emitter HCBT [72, 73]. The fabrication of this device does not require additional lithography masks, but is done using the *p*-well implant mask from the CMOS process. The *p*-well, which serves as a local substrate in the CMOS processing, is placed beneath the extended extrinsic collector. The *p*-well causes the extrinsic collector region to be fully depleted, as is the case for the intrinsic region. In this way, the breakdown voltage is further increased, thus extending the application spectrum of the HCBT BiCMOS technology.

1.8.3 Collector region design

The performance of the HCBT can be tailored to a specific application by the optimization of the collector region. To illustrate this possibility, three different collector doping profiles of the fabricated HCBT devices are shown in Fig. 1.29 [74]. The collectors of the *n*-hill and steep *n*-hill devices are implanted by using the first HCBT mask, whereas the CMOS *n*-well device uses the *n*-well mask from the CMOS process. The implanted *n*-collectors are annealed by all of the subsequent high-temperature CMOS steps. The *n*-hill HCBT is designed to results in a steep doping profile with the maximum at the extrinsic base-collector *pn* junction. The

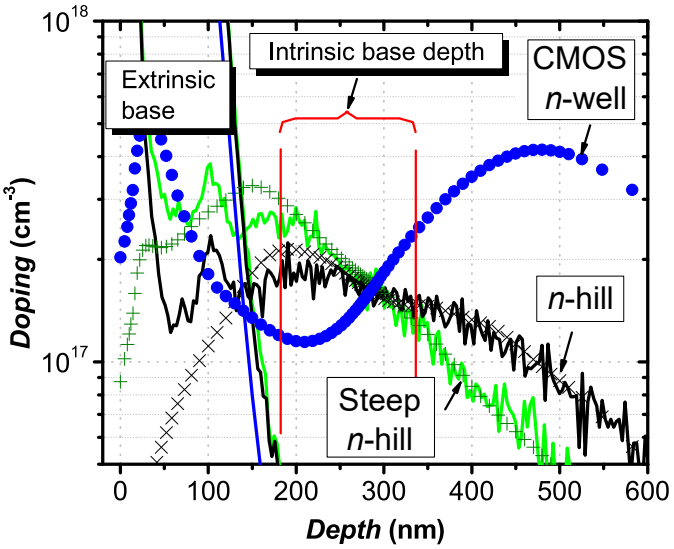


Figure 1.29: Measured secondary ion mass spectrometry (SIMS) (lines) and simulated (symbols) doping profiles of collector regions along the cross-section AA' in Fig. 1.24b, after all of the CMOS annealing steps [74].

HCBT with the uniform *n*-hill exhibits more uniform doping profile with a lower concentration at the top of the intrinsic transistor, and with a deeper distribution. The CMOS *n*-well device has a peak doping at the depth of around 450 nm and has a retrograded profile in the intrinsic transistor region, and it has the highest implanted dose. The steep *n*-hill HCBT suppresses the charge sharing effect, and is shown that such profile relaxes the electric field at the bottom of the intrinsic transistor [75]. Hence, it has higher BV_{CEO} and an optimum f_T versus BV_{CEO} trade-off. Additionally, the HCBT process has a low-doped version of the uniform *n*-collector device, which has a similar doping profile but shifted to lower concentrations over the entire depth. Such version exhibits even higher breakdown voltage and it is fabricated to enable the operation up to even higher voltages, e.g., for the application in radiofrequency power amplifiers.

The HCBT with the low-doped *n*-collector has shown a great noise performance for the applications in low-noise amplifier design [76]. On the other hand, the HCBT with uniform *n*-collector exhibits the highest associated gain implying the best noise-gain tradeoff. Finally, the CMOS *n*-well provides the lowest-cost of implementation, but also satisfies the requirements of the modern sub-6 GHz wireless communication standards. Furthermore, the uniform *n*-collector HCBT is the best solution among the various collector designs for a high-linearity mixer design for the applications in the base stations of the wireless communications infrastructure [77].

Chapter 2

Large-signal characteristics of horizontal current bipolar transistor

The performance of a radiofrequency power amplifier depends to a large extent on the characteristics of the active device. Although small-signal measurements might be sufficient for small-signal circuit design, such as low-noise amplifier, a power amplifier exploits the maximum ratings of the transistor and, therefore, demands large-signal characterization before the circuit design phase can begin. Due to the difficulty of accurately modelling large-signal effects in bipolar transistors, the most reliable process of investigating and determining the large-signal performance of the transistor is to measure its performance using a dedicated measurement setup; such a setup enables terminal impedance variation at RF and, thus, it is called load-pull setup.

2.1 Measurement methodology

The main difference between small-signal and large-signal circuit design is the optimum matching at the transistor's terminals. While the optimum matching impedances Z_{Sopt}/Z_{Lopt} for an amplifier operating in small-signal power range are complex conjugate of its terminal impedances:

$$Z_{\mathrm{Sopt}} = \overline{Z_{\mathrm{in}}}, \tag{2.1}$$

$$Z_{\mathrm{Lopt}} = \overline{Z_{\mathrm{out}}}, \tag{2.2}$$

where $\overline{Z_{\mathrm{in}}}$ and $\overline{Z_{\mathrm{out}}}$ are complex-conjugates of the transistor's input and output impedances, respectively, the two critical amplifiers in an RF front end, low-noise amplifier (LNA) and power amplifier (PA), demand a consideration of different parameters than the maximum signal

power transfer for the matching networks. Namely, an LNA requires an optimal input matching impedance to be presented to the transistor in order to achieve minimum noise figure (NF), which is the most important parameter for an LNA. This optimal input matching impedance can be found by accurate modelling of the noise sources in the compact model or empirically by source-pull setup; measuring noise figure for varied input impedance. Similarly, the power amplifier requires the optimal output matching impedance to be presented to the transistor in order to achieve the maximum output power available for the selected device. Again, this optimal output matching impedance can be found by using accurate compact models in the circuit simulator, or by performing load-pull measurements; measuring output power for varied output impedance. The main difference between an LNA and PA is the signal amplitude on the input and output of the transistor. Namely, an LNA operates with a low enough signal amplitude which does not approach the saturation/cut-off regions in BJTs or resistive/cut-off regions in MOSFETs, i.e., there is no clipping of the current and voltage waveforms in LNA. Such operation ensures that the output is a linear function of the input. On the other hand, a PA outputs a maximum output power for the selected transistors, and as such, the transistor is exploited to its limits; the current and voltage experience clipping and besides the amplified input signal, the harmonics are also created at the output. On the input, the signal amplitude necessary to achieve maximum output power depends on the gain of the transistors; if the gain is low enough, the input also operates with large-signal, whereas the aim of the input matching in PA is to achieve maximum available gain with the optimal output matching. Therefore, the output is always a nonlinear function of the input for a PA, and the optimum output matching impedance, and usually the input impedance, is found empirically by source/load-pull measurements.

The device under test is a packaged HCBT. The transistor is selected according to the requirements of the Wi-Fi communications, where the target output power is usually set at around 18 dBm for the handheld devices. The HCBT is characterized at the fundamental frequency of f_0 = 2.4 GHz by source/load-pull measurements to gain insight into the large-signal behaviour of the transistor and, subsequently, facilitate large-signal (nonlinear) modelling of the HCBT. An automated load-pull setup is implemented which uses two passive automated mechanical impedance tuners for varying the input and output matching impedances presented to the transistor. A fixture is designed and fabricated which provides coaxial-to-microstrip transition at the input and output while adding low insertion loss. Swept-power (AM/AM) measurements are performed prior to and after the load-pull and source-pull for each class of operation to determine the performance of the HCBT both in 50-Ω and optimal matching environment. Both source-pull and load-pull is performed to optimize output power, collector efficiency, and gain, in three classes of PA operation, namely Class A, Class AB, and Class B. The DC output characteristics of the transistor are measured to determine the quiescent points for the respective classes of operation and to determine the load line resistance, output power, and efficiency,

corresponding to the ideal load line. Load-pull and source-pull measurements give information about the optimum match at the output and input, respectively, considering output power, efficiency, or gain.

2.2 Load-pull/source-pull setup

The block diagram of the load- and source-pull measurement setup is shown in Fig. 2.1. The setup is of a traditional scalar type [78], and it enables automated DC and RF measurements, such as input and output *I-V* characteristics, RF power sweeps, PA efficiency and linearity, source-pull and load-pull. The components enabling swept-impedance measurements are automated passive mechanical impedance tuners based on a slab transmission line and a shunt sliding short. Two stepper motors, operated by the tuner controller, set the impedance at the tuner ports to a predefined value. Source tuner sets the impedance seen by the input of the device under test (DUT) looking towards the signal generator, whereas load tuner sets the impedance seen by the output of the DUT looking towards the signal analyzer. Signal generator is used as a source of continuous wave (CW) RF signal that drives the DUT. Output signal power is measured by signal analyzer at frequencies of up to 7.5 GHz. Biasing of the DUT is implemented with the coaxial bias tees positioned before the source tuner and after the load tuner. Such positioning eliminates additional insertion loss that would otherwise be contributed by bias tees in between the tuners and the DUT. In that case, the additional insertion loss would lower the maximum synthesizable reflection coefficient Γ seen by the input and output of the DUT. Signal generator, signal analyzer, DC power supply, and tuner controller are connected to the PC in order to achieve complete automation and synchronization of the signal generation, tuner movement, and signal measurement.

The components used in the measurement setup are characterized by scattering parameter (*S*-parameter) measurements using vector network analyzer (VNA). The accuracy of these measurements is crucial to the performance of the load-pull setup. Since the output power is measured by the signal analyzer at its input port, the measured power is not characteristic of the DUT, but the characteristic of the setup chain between the DUT and the analyzer's input is also added to the measurement result. Therefore, the measured output power is lower than the power at the output of the DUT. The measurement reference plane is shifted to the output of the DUT by characterization of each component between the DUT and the analyzer; load tuner, output bias tee, and all coaxial adapters, connectors, and cables used for component connection. On the input side, the characteristics of the components are also measured in order to accurately define the available power on the DUT's input. Thus, the input available power is defined at input of the DUT, whereas the output power is defined at the output of the DUT. The measurement algorithm, which performs the de-embedding calculations and sets the measurement parameters

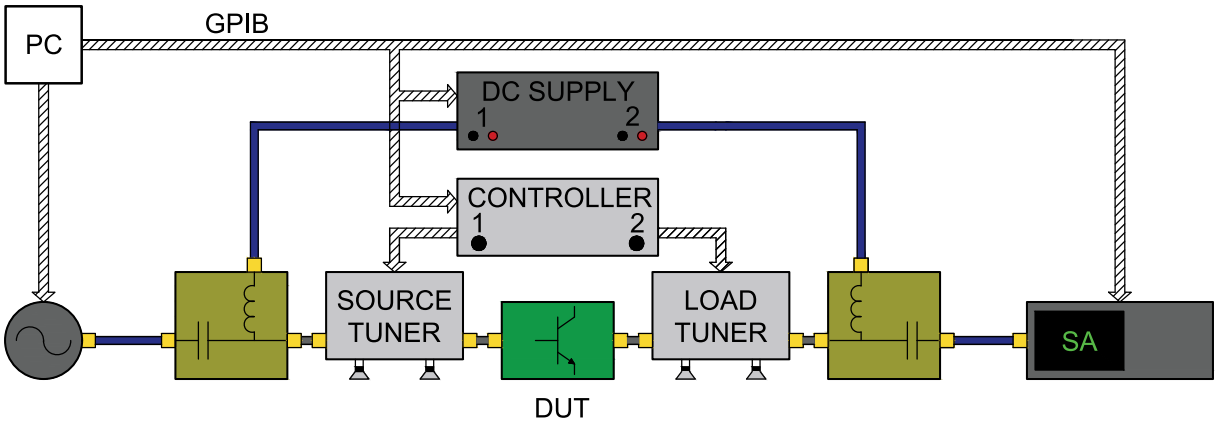


Figure 2.1: Automated load-pull setup used for DC and RF measurements of packaged HCBT transistors. Both source and load tuners are operated by the tuner controller which communicates with the PC. The input and output bias tees, used for DC biasing, are placed away from the DUT to minimize the losses added between the tuners and the DUT. Signal generator, signal analyzer, and DC power supply are also controlled by the PC.

(e.g. DC bias, terminal impedances, and input available power), is designed in LabVIEW [79].

To verify the performance of the setup, transducer gain G_T is measured for the ideal through standard as a DUT. This verification method is usually termed delta-G_T method [80]. The gain is measured for different source and load impedances, with the accuracy being the worst for high reflection coefficient magnitudes, and equal to +/- 0.5 dB.

2.2.1 DUT and test fixture

The DUT is an HCBT packaged in a 4-pin SOT343 package [81]. The package is specifically designed to minimize the inductance of the emitter lead by separating the connection to the HCBT's emitter in two parallel connections; two pins are reserved for the emitter, and the remaining two for the base and collector.

The HCBT is soldered down to the test fixture shown in Fig. 2.2. The fixture is fabricated on a 1-mm-thick FR4 substrate with the relative permittivity ε_r of 4.3, and consists of 50-Ω microstrip lines which interface the HCBT; the lines are 1.93 mm wide. To transition from the coaxial standard, which is common to all components of the measurement setup, edge-mount subminiature version A (SMA) connectors are used at the input and output of the fixture. In this way, the 50-Ω characteristic impedance is maintained all the way up to the input and output reference planes while incurring minimal insertion loss of around 0.05 dB. Both emitter pins are grounded using 4 plated vias with a diameter of 0.5 mm, thus securing a low impedance path to the bottom ground plane, therefore, the HCBT is measured in the common-emitter configuration; the RF signal is fed to the base, whereas the output is measured at the collector. The fixture halves are modelled by measuring 50-Ω lines of different lengths to determine the equivalent schematic of the concatenated identical fixture halves. The model is then compared with the

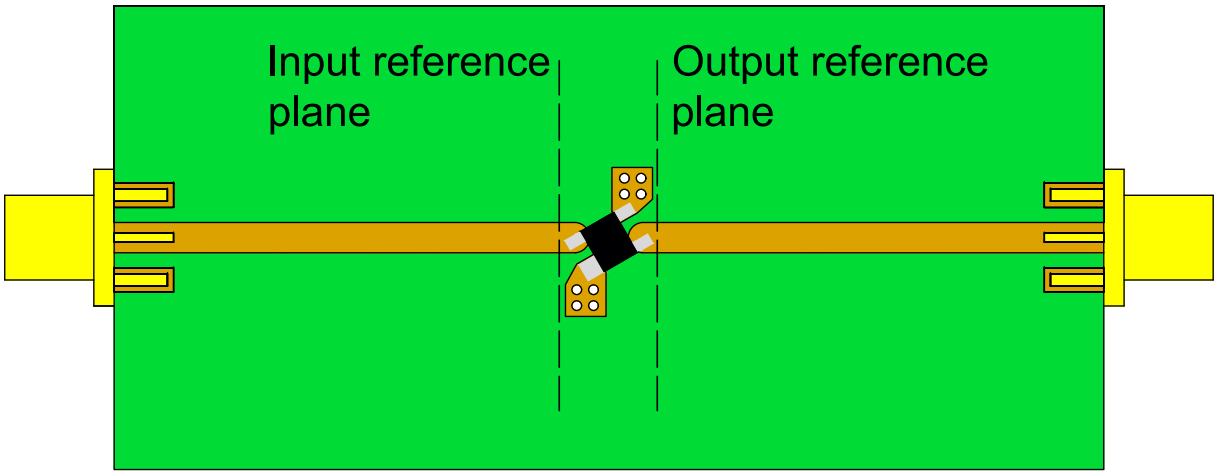


Figure 2.2: Measurement test fixture for the characterization of HCBTs packaged in a 4-pin SOT343 package. The input and output measurement reference planes are shown with the dashed lines. The fixture halves are modelled and de-embedded to enable the reference plane shift to the base and collector pins. Both emitter pins are grounded to the bottom ground plane by 4 plated vias to lower the inductance.

measurements performed on the full test fixture without the DUT, and excellent agreement is achieved.

2.3 Class-A/AB/B performance

The performance of HCBT with an emitter area A_E of 31.2 μm^2 is measured using the developed load-pull setup [82]. The transistor consists of 24 unit HCBTs connected in parallel, each one with the emitter width of 13 μm. The performance is measured for the three common classes of PA operation, namely, Class A, AB, and B, at the fundamental frequency of 2.4 GHz.

2.3.1 Output DC characteristics and load line analysis

The output DC characteristics for the analyzed HCBT are shown in Fig. 2.3. The characteristics are measured with the base-emitter voltage V_{BE} as a parameter and with both source and load impedances set to 50 Ω to ensure stability during DC measurements. The targeted output power for this HCBT is set to around 18 dBm, since this is a common design goal for the power amplifiers used in Wi-Fi standard. To achieve the targeted output power, an idealized dynamic load line is drawn in the output DC characteristics, which is also shown in Fig. 2.3. The maximum collector-emitter voltage V_{CEmax} is chosen to be somewhat lower than the open-emitter breakdown voltage $\mathrm{BV_{CBO}}$ of 5.2 V. The maximum collector current I_{Cmax} is set to 100 mA, which then sets the lower voltage limit for the load line, usually termed the knee voltage V_{knee}, at V_{knee} = 0.75 V. For this load line and Class-A operation, the bias point is defined with I_{CQ} = 50 mA and V_{CEQ} = 2.875 V. Thus, the collector current swings from 0 to 100 mA, whereas the collector-emitter voltage swings from 0.75 to 5 V, while the minimum

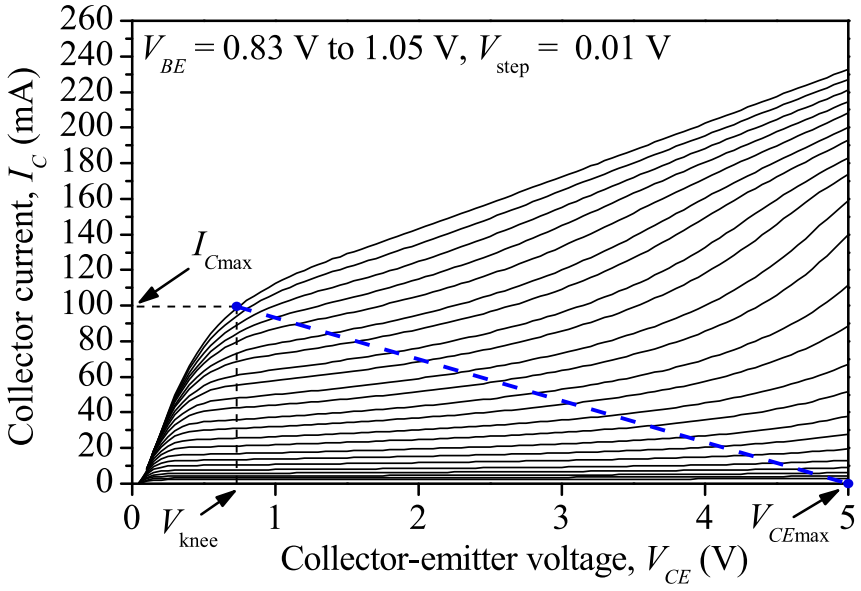


Figure 2.3: Output DC *I-V* characteristics of the analyzed HCBT (A_E = 31.2 μm^2) with base-emitter voltage V_{BE} as a parameter. A targeted, idealized dynamic load line with the respective maximum values of current and voltage swing at the collector exhibiting an output power of around 18 dBm is also shown. The critical parameters determining the overall transistor performance are marked; I_{Cmax}, V_{CEmax}, and V_{knee}.

value of V_{CE} is restricted with the knee voltage V_{knee} of 0.75 V at I_{C} = 100 mA. Additionally, the output DC curves tend to change the slope for the collector-emitter voltage above around 4 V. For the collector current of up to 140 mA, the increase is the result of impact ionization taking place in the base-collector *pn* junction, thus, causing a sharp increase of collector current. For collector current higher than 140 mA, the collector current is again a linear function of the collector-emitter voltage, as is the case for much lower currents of up to 40 mA. This phenomena is usually ascribed to the self-heating of the transistors, which tends to cancel the sharp current increase due to the negative temperature coefficient of the impact ionization. Therefore, the amplitudes of collector current and collector-emitter voltage RF waveforms are 50 mA and 2.125 V, respectively, while the load line is chosen to avoid both the regions of impact ionization and self-heating.

The load line determines the performance of the transistor, considering the output power and collector efficiency. Once determined, the load line provides the necessary output impedance which needs to be presented to the collector in order to achieve the targeted output power, while exhibiting the maximum collector efficiency in Class-A operation. The expected performance of the HCBT can now be calculated by

$$P_{\mathrm{OUT}} = \frac{1}{2}\frac{I_{\mathrm{Cmax}}}{2}\frac{V_{\mathrm{CEmax}} - V_{\mathrm{knee}}}{2} = 53.13\ \mathrm{mW} = 17.24\ \mathrm{dBm}, \tag{2.3}$$

$$R_{\mathrm{L}} = \frac{V_{\mathrm{CEmax}} - V_{\mathrm{knee}}}{I_{\mathrm{Cmax}}} = 42.5\ \Omega, \tag{2.4}$$

$$\eta = \frac{P_{\mathrm{OUT}}}{V_{\mathrm{CEQ}} \cdot I_{\mathrm{CQ}}} \cdot 100\% = 39.7\%, \tag{2.5}$$

where P_{OUT}, R_{L}, η, I_{CQ}, and V_{CEQ} are output power at the fundamental frequency, load resistance, collector efficiency, DC collector current, and DC collector-emitter voltage, respectively [15]. The expected output power is around 17 dBm, which is close to the targeted value for this load line. The load line resistance R_{L} is the optimal matching resistance which is to be presented to the HCBT at the collector reference plane in order to achieve the output power of 17.24 dBm. For this bias point and load resistance, the expected collector efficiency is 39.7%. The output curves are shown up to I_{Cmax} for the voltage V_{knee} (V_{BE} = 1.05 V) since for higher collector currents the exponential dependence of I_{C} on V_{BE} disappears. Furthermore, if higher collector current is selected for I_{Cmax}, the V_{knee} would also increase which would lower the collector efficiency. The load line shown in Fig. 2.3 corresponds to the highest output power for which the linear dependence of output to the input signal is maintained. For higher input power, the collector current and voltage clipping occurs, thus, causing the nonlinear operation and harmonics at the output. Furthermore, the target collector efficiency calculated in (2.5) is lower than the efficiency of the ideal Class-A PA of 50%. The only parameter affecting the efficiency is V_{knee}, and the value of 0.75 V lowers the efficiency by 10.3%. Nevertheless, this parameter is common to every transistor type regardless of the technology and as such needs to be taken into account while choosing the maximum collector current I_{Cmax}, since the two are proportional; higher the I_{Cmax}, higher the V_{knee}.

Although the idealized analysis presented so far can provide the values for DC point and load resistance to start with, the load resistance of 42.5 Ω set at the external collector reference plane is transformed to some other, unknown impedance at the internal collector electrode, i.e., at the collector die pad. In other words, the parasitic capacitance and inductance of the package along with the nonlinear capacitances of the transistors, add to the load resistance which then cause the internal transistor electrodes to be effectively terminated by some different load impedance. This relationship can be expressed by the load reflection coefficient at the internal reference plane as [14]

$$\Gamma_{\mathrm{Lint}} = S_{11} + \frac{S_{12}S_{21}\Gamma_{\mathrm{L}}}{1 - S_{22}\Gamma_{\mathrm{L}}}, \tag{2.6}$$

$$Z_{\mathrm{Lint}} = Z_0 \frac{1 + \Gamma_{\mathrm{Lint}}}{1 - \Gamma_{\mathrm{Lint}}}, \tag{2.7}$$

where Γ_{Lint}, Z_{Lint}, Γ_{L}, and Z_{L}, are reflection coefficient and impedance at the internal reference plane, reflection coefficient and impedance at the load (external) reference plane, respectively, whereas S_{11}, S_{12}, S_{21}, and S_{22} are the terms of the scattering matrix **S** of the transistor and package parasitics. The Z_0 parameter is the reference impedance of 50 Ω. In other words, if the load impedance at the external reference plane is set to a purely resistive impedance of $Z_{\mathrm{L}} = 42.5 + j0\ \Omega$, with the reflection coefficient given by

$$\Gamma_{\mathrm{L}} = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} = \frac{42.5 - 50}{42.5 + 50} = -0.08 + j0, \tag{2.8}$$

which would be transformed to the impedance of nonzero reactive part according to (2.6), since the package and transistor parasitics are mainly reactive and, thus, the **S** contains purely reactive terms.

To present the intrinsic transistor with the optimal load resistance, the optimal impedance needs to be set at the collector reference plane; this impedance is not equal to the purely resistive one calculated from (2.4). As shown in (2.6) and (2.8), this unknown impedance can contain both resistive and reactive parts. Since the reactive part cannot be inferred solely from the output DC characteristics, as is the case for the resistive part, load-pull and source-pull measurements are performed. These measurements enable empirical determination of the optimal load and source impedances which need to be set at the collector and base reference planes, respectively, in order to achieve the targeted output power and collector efficiency calculated in (2.3) and (2.5), respectively. The optimal matching does not take into account the gain of the device, since this is not the critical parameter for PA. Furthermore, the gain is a function of the device's transconductance g_{m}, which is set by the DC point. As shown, the DC point is chosen to set the load line in order to achieve the maximum output power and, therefore, not to a maximum-g_{m} DC point. Nevertheless, the optimal matching on the input serves the purpose of increasing the gain as much as possible while delivering the highest possible collector efficiency and output power. Since both the input and output can operate in large-signal regime, the optimal source impedance is also found by varying the input impedance and measuring the gain of the transistor.

2.3.2 Large-signal performance parameters

The process of searching for the optimal matching impedances at the input (base) and output (collector) entails the iterative process of varying the terminal impedances and measuring the relevant performance parameters, such as output power, gain, and collector efficiency. The analysis performed using the output DC characteristics [see Fig. 2.3] serves as a starting point for the load-pull measurements. The load-pull setup provides the output power, collector efficiency, and gain, for the predefined input power. The output power and collector efficiency are

calculated as in (2.3) and (2.5), respectively, whereas the gain is found by

$$G_T = \frac{P_{OUT}}{P_{IN}}, \tag{2.9}$$

where G_T, P_{IN}, and P_{OUT} are transducer gain, delivered output power, and available input power. The available input power is the maximum power available from the source that can be delivered to the input:

$$P_{IN} = \frac{|V_S|}{8Z_0}\frac{|1-\Gamma_S|^2}{(1-|\Gamma_S|^2)}, \tag{2.10}$$

where V_S and Γ_S are source voltage and source reflection coefficient, respectively. The delivered output power is the power delivered to the load, given by

$$P_{OUT} = \frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2(1-|\Gamma_{SA}|^2)|1-\Gamma_S|^2}{|1-S_{22}\Gamma_{SA}|^2|1-\Gamma_S\Gamma_L|^2}, \tag{2.11}$$

where Γ_{SA} is the reflection coefficient of the signal analyzer's input port (which measures the output power), whereas Γ_L is the load reflection coefficient seen looking from the collector into the load side of the setup, given by

$$\Gamma_L = S_{11}^{ls} + \frac{S_{12}^{ls}S_{21}^{ls}\Gamma_L}{1-S_{22}^{ls}\Gamma_{SA}}, \tag{2.12}$$

where S_{11}^{ls}, S_{12}^{ls}, S_{21}^{ls}, and S_2^{ls}, are the terms of the $\mathbf{S}^{ls}$ including all the components of the load side of the setup between the collector and the signal analyzer.

The DC power dissipated by the transistor is calculated from the measured base and collector currents I_{BQ} and I_{CQ}, whereas the base-emitter V_{BEQ} and collector-emitter V_{CEQ} voltages are set to achieve a desired collector current I_{CQ} and load line.

Impact of load termination

The input port of the signal analyzer is a load termination of the setup, and it exhibits a return loss RL$^{'}$ = -20log$_{10}$|$\Gamma_{SA}^{'}$| = 15 dB at 2.4 GHz. Ideally, the input impedance of the analyzer is assumed to be 50 Ω, but the exact value, if different than the ideal value, might impact the precision of the load impedance tuning for extremely low or high impedances, e.g., 2 Ω or 1 kΩ. To illustrate the impact of the analyzer's input port on the synthesized load impedance Γ_L, the load impedance is calculated for Γ_{SA} of -15 dB. Since the *S*-parameters of the load side components depend on the load tuner position, for this illustrative calculation an arbitrary $\mathbf{S}^{ls}$ given by

$$\mathbf{S}^{\mathrm{ls}} = \begin{bmatrix} 0.15 + j0 & 0.6 - j0.6 \\ 0.6 + j0.6 & 0.2 + j0 \end{bmatrix} \tag{2.13}$$

is employed in (2.12) to calculate the discrepancy with respect to the ideal case of $\Gamma_{\mathrm{SA}} = 0$, i.e., $Z_{\mathrm{SA}} = 50\ \Omega$. For this ideal case, the load impedance is

$$\Gamma_{\mathrm{Lideal}} = S_{11}^{\mathrm{ls}} + \frac{S_{12}^{\mathrm{ls}} S_{21}^{\mathrm{ls}} 0}{1 - S_{22}^{\mathrm{ls}} 0} = S_{11}^{\mathrm{ls}} = 0.15 + j0. \tag{2.14}$$

On the other hand, if the reflection coefficient of the analyzer's input port is -15 dB, e.g., $\Gamma_{\mathrm{SA}} = -0.18 + j0$, then

$$\Gamma_{\mathrm{Lreal}} = S_{11}^{\mathrm{ls}} + \frac{S_{12}^{\mathrm{ls}} S_{21}^{\mathrm{ls}} (-0.18)}{1 - S_{22}^{\mathrm{ls}} (-0.18)} = 0.0273 + j0. \tag{2.15}$$

which deviates from the ideal value in (2.14).

Therefore, a 10-dB attenuator is added to the input of the analyzer in order to increase the input return loss of the signal analyzer to

$$\mathrm{RL} = \mathrm{RL}^{'} + 20 = 35\ \mathrm{dB}, \tag{2.16}$$

where RL is the return loss of the analyzer's input port with the 10-dB attenuation added. The 20-dB increase is the result of a travelling wave passing the attenuator twice; first time in the direction from the collector to the analyzer, and the second time when reflected from the analyzer's input port to the collector. The added attenuation ensures that the analyzer's input port does not impact the accuracy of the load impedance synthesized at the collector. Finally, for a RL = 35 dB, e.g., $\Gamma_{\mathrm{SA}} = -0.0173 + j0$, the load impedance is

$$\Gamma_{\mathrm{L}} = S_{11}^{\mathrm{ls}} + \frac{S_{12}^{\mathrm{ls}} S_{21}^{\mathrm{ls}} (-0.0173)}{1 - S_{22}^{\mathrm{ls}} (-0.0173)} = 0.138 + j0. \tag{2.17}$$

which is much closer to the ideal value. More precisely, for RL of -15 dB and -35 dB, the magnitude of the load impedance $|\Gamma_{\mathrm{L}}|$ differs by -82% and -8% from the ideal value in (2.14), respectively, for the chosen $\mathbf{S}^{\mathrm{ls}}$ and Γ_{L}. Furthermore, the attenuator decreases the power incident on the analyzer input port to a value much lower than the maximum power rating of its input (30 dBm). Additionally, the signal analyzer is more accurate while measuring signals lower than the rating of the input, since the circuitry of the analyzer's input should not be driven to a compression [83]. Therefore, the attenuation serves the dual purpose of increasing the return loss of the analyzer, and protecting it from excessive input power thus facilitating linear response.

2.3.3 Load-pull and source-pull analysis

The first step in finding the optimal matching impedances is to analyze the performance of the transistor with 50-Ω termination at the input and output. To that end, the source and load tuners are set to present the base and collector with a 50-Ω at 2.4 GHz:

$$Z_{\mathrm{S}} = Z_{\mathrm{L}} = 50\ \Omega. \tag{2.18}$$

The DC point is set by defining the base-emitter voltage V_{BEQ} and collector-emitter voltage V_{CEQ} to 0.94 V and 2.87 V, respectively. The resulting operating bias point Q of the HCBT is

$$\mathrm{Q} = (I_{\mathrm{CQ}}, V_{\mathrm{CEQ}}) = (55\ \mathrm{mA}, 2.87\ \mathrm{V}). \tag{2.19}$$

which is the bias point defined in the analysis performed on the output DC characteristics in Fig. 2.3. The bias point remains unaltered in the small-signal operation, but once waveform clipping and harmonics occur, the bias point shifts due to this nonlinear operation. More precisely, the base and collector current shift when the transistor enters the nonlinear regime, whereas the base-emitter and collector-emitter voltages remain constant due to the biasing with voltage sources; they force the voltage on the base and collector regardless of the nonlinearity present. Therefore, the bias point is defined in the small-signal regime, i.e., for low input power levels.

Once the impedance and bias point are set, the input power P_{IN} is swept and the output power P_{OUT}, collector efficiency η, and gain G_{T} are measured, as shown in Fig. 2.4. The output power is a linear function of the input power for power of up to around 5 dBm. For higher input power, the output is not a linear function of the input; the transistor enters the compression region and the output power increases more gradually. Furthermore, the gain is constant in the small-signal region but decreases in the compression region. Thus, there is an input power level which separates the small- and large-signal regions; usually, this power is the point where the gain drops by 1 dB (P1dB). This parameter is usually taken as the maximum output power for the respective terminal impedances and bias point, since for even higher output power the PA is operating with high nonlinearity which might render it unusable for modern wireless communications. The gain in the small-signal region is 10.62 dB. Thus, the point in which gain drops by 1 dB, to 9.62 dB, is for the input power of 7.91 dBm, with the corresponding output power of 17.54 dBm. The collector efficiency behaves differently than the output power and gain, experiencing the maximum in the compression region. The HCBT achieves maximum collector efficiency of 44% for the input power of 11 dBm. The efficiency drops sharply for lower input power.

Although P1dB is taken as the limit of small-signal operation, in this point the transistor already experiences high nonlinearity and somewhat lower point can be taken as a limit of

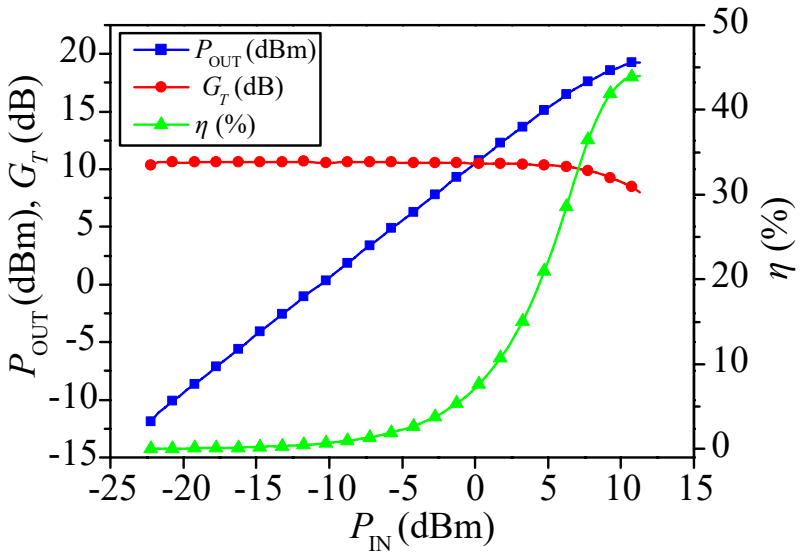


Figure 2.4: Delivered output power P_{OUT}, transducer gain G_T, and collector efficiency η, for the available input power P_{IN} in the range from -23 dBm to 11 dBm. The base-emitter and collector-emitter DC voltages are 0.94 V and 2.87 V, respectively. The input and output impedances are set to $Z_S = Z_L = 50\ \Omega$.

linear operation, e.g., where the gain begins to deviate from the constant value of 10.62 dB. This point is around $P_{IN} = 6$ dBm, which results in the output power of 16.04 dBm. This point is roughly the maximum linear power of the unmatched transistor, for the chosen bias point. In this point, the collector efficiency is 28%. Thus, the load-pull is performed to find the optimal output and input matching impedances in order to maximize the performance of the HCBT, considering all three performance parameters.

To maximize the linear output power, a load-pull measurement is performed for the same bias point, but for the input power of maximum linear power in a 50 Ω environment of 6 dBm. In other words, the load impedance is varied, whereas the input available power is kept constant at 6 dBm for each load impedance. The result is the optimal load impedance Γ_{Lopt}. Once the optimal load impedance is found, the HCBT is terminated by Γ_{Lopt} at the output and source-pull is performed to find the optimal source impedance Γ_{Sopt}, which provides the maximum transducer gain with Γ_{Lopt} at the output. For all source and load impedances, both the output power and collector efficiency are measured. The process is then repeated until there is no change of optimal source impedance with the load termination.

The results of both measurements are shown in the Smith chart in Fig. 2.5. For every load/source impedance, there is an output power and collector efficiency value. If one is to connect the impedances of the same output power or collector efficiency, load/source-pull contours are created. The contours represent the lines of equal output power or collector efficiency. The function of output power/collector efficiency on the source/load impedance has a single maximum, which corresponds to the optimal matching impedance for the respective quantity. For $P_{IN} = 6$ dBm, the HCBT achieves output power of 16.95 dBm while terminated by

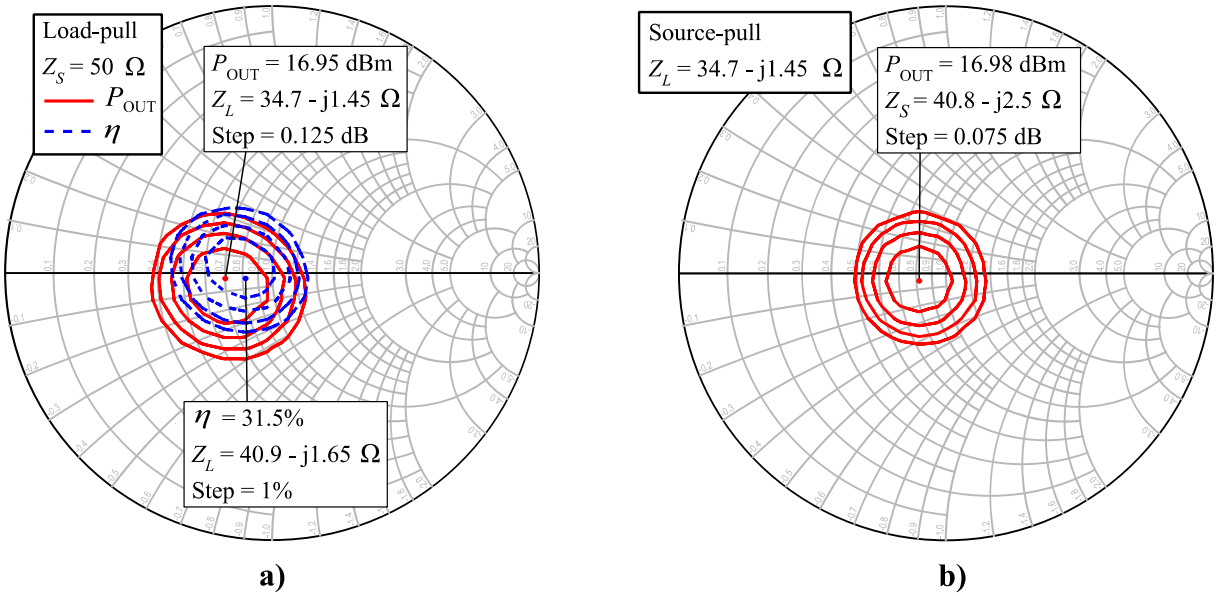


Figure 2.5: a) Output power P_{OUT} and collector efficiency η load-pull contours for the constant available input power P_{IN} of 6 dBm and source impedance of 50 Ω. b) Output power P_{OUT} source-pull contours for the load impedance $Z_{\mathrm{Lopt}} = 34.7 - j1.45$ Ω. The fundamental frequency $f_0 = 2.4$ GHz. Contours are drawn by interpolating the measured data.

$$Z_{\mathrm{Lopt}} = 34.7 - j1.45\ \Omega, \tag{2.20}$$

whereas the maximum collector efficiency of 31.5% is achieved for

$$Z_{\eta\mathrm{opt}} = 40.9 - j1.65\ \Omega. \tag{2.21}$$

The real part of the optimal load impedance $\Re(Z_{\mathrm{Lopt}}) = 34.7$ Ω, corresponds to the predicted load resistance of 42.5 Ω from the idealized load line analysis, but, as already detailed in the preceding sections, differs due to the parasitics of the transistor and the package. Furthermore, Γ_{Lopt} and $\Gamma_{\eta\mathrm{opt}}$ are relatively close; it is possible to achieve both the maximum output power and maximum collector efficiency for the HCBT by matching the output by the impedance in the vicinity of the two optimal impedances.

The source-pull is performed with the HCBT matched by the optimal load impedance Γ_{Lopt} found by load-pull. The source-pull contours in Fig. 2.5b also exhibit a maximum, which corresponds to the optimal source impedance for the HCBT. The HCBT achieves an output power of 16.98 dBm for

$$Z_{\mathrm{Sopt}} = 40.8 - j2.5\ \Omega, \tag{2.22}$$

whereas the transducer gain is 10.68 dB. Contrary to the optimal load matching, the optimal

source impedance does not contribute significantly to the gain increase; the gain increases for only 0.03 dB. This is due to the fact that the optimal source impedance is extremely close to the system impedance of 50 Ω. That means that if the input is left unmatched, the maximum gain is achieved nevertheless. Additionally, if there is no matching network at the input, there is no insertion loss added, and, more importantly, such a termination is inherently broadband. In other words, a device with 50 Ω optimal matching impedances is highly desirable in RF circuit design. The analyzed HCBT operates near its optimal point even in a 50 Ω environment [see Fig. 2.4]. At $\Gamma_{\mathrm{Lopt}} = \Gamma_{\mathrm{Sopt}} = 50\ \Omega$, the output power and collector efficiency decrease by 0.125 dB and 1%, respectively. The efficiency is more sensitive to the load impedance change than the output power, and a 1% drop in efficiency could be a large increase in DC consumption for some high-power PAs in base stations.

There is a difference between the load-pull and source-pull contours in Fig. 2.5. Namely, the load-pull contours are oval-shaped, as predicted by the load-pull theory [15]. On the other hand, the source-pull contours exhibit concentric circles, which is a sign of small-signal operation at the input. The source-pull, in this case, gives the optimal source impedance which is a conjugate complex of the transistor's input impedance, i.e., the optimal source impedance could be found by measuring *S*-parameters of the HCBT and subsequently designing the input matching network. Nevertheless, once the base circuit enters the nonlinear regime, harmonics occur at the input also, and *S*-parameter measurement is not sufficient. The best course of action then is to do the source-pull measurement.

The HCBT, when matched by the optimal source and load impedances, provides the optimal performance with respect to the output power, collector efficiency, or both. To that end, the swept-power transfer characteristics from Fig. 2.4 are measured for $\Gamma_{\mathrm{S}} = \Gamma_{\mathrm{Sopt}}$ and $\Gamma_{\mathrm{L}} = \Gamma_{\mathrm{Lopt}}$ and the results are shown in Fig. 2.6. The curves are shown for both the maximum output power matching and for the unmatched transistor from Fig. 2.4. The optimal match for maximum output power increased the linear output power from 16.04 dBm to 16.9 dBm, whereas the output power in the compression point is increased from 17.54 dBm to 18.7 dBm. The gain also increased from 10.62 dB to 11.1 dB in the linear region. As already mentioned and shown in Fig. 2.5, the optimal matching impedances for the maximum output power and maximum collector efficiency are similar, thus, the optimal matching for the maximum output power also increased the collector efficiency in the entire power range. In the maximum linear power point, the collector efficiency is increased from 28% to 30%. Although the optimal impedances are close to 50 Ω, matching extracts the maximum performance out of the device, wherein the analyzed HCBT achieves an increase in output power and collector efficiency of 0.86 dB and 2%, respectively. The idealized load line analysis from the section 2.3.1, results in the predicted output power and collector efficiency correspond to the maximum linear power, since the load line from Fig. 2.3 experiences clipping and subsequent gain compression for higher output

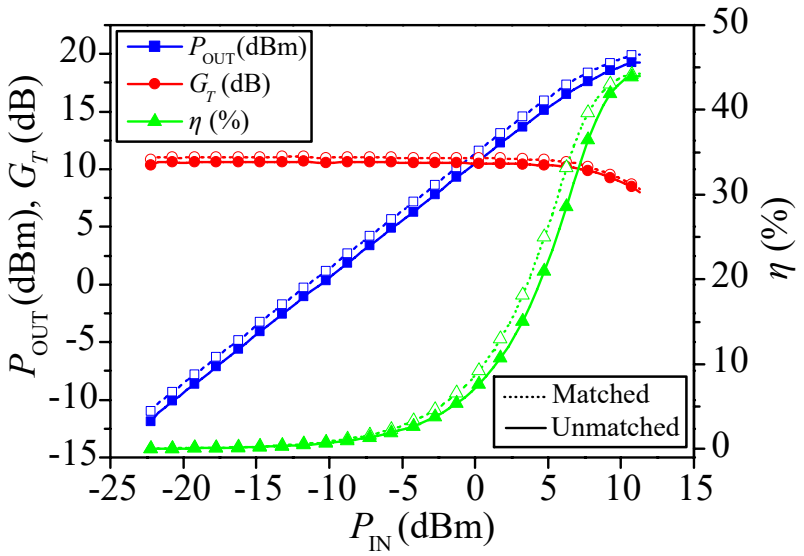


Figure 2.6: Delivered output power P_{OUT}, transducer gain G_{T}, and collector efficiency η, for the available input power P_{IN} in the range from -23 dBm to 11 dBm, for both the unmatched [see Fig. 2.4] and for the maximum output power matching. The base-emitter and collector-emitter DC voltages are 0.94 V and 2.87 V, respectively. The input and output impedances are set to $Z_{\mathrm{S}} = Z_{\mathrm{Sopt}} = 40.8 - j2.5\ \Omega$ and $Z_{\mathrm{L}} = Z_{\mathrm{Lopt}} = 34.7 - j1.45\ \Omega$.

power. The predicted values of output power and collector efficiency from (2.3) and (2.5) equal 17.24 dBm and 39.7%, respectively. On the other hand, the measured maximum linear output power and the corresponding collector efficiency are 16.9 dBm and 30%, respectively. Therefore, there is a discrepancy between the DC load line analysis and load-pull measurements, which renders the source-pull and load-pull analysis crucial for the PA design.

The optimal matching for maximum output power increased the maximum linear output power by 0.86 dB with respect to the unmatched HCBT. Since the setup measures the performance of the DUT only, i.e., it does not take into account the insertion loss of the components of the setup, the actual gain of the matching depends on the topology and design of the matching networks of the designed PA. Therefore, if the insertion loss of the output matching network is higher than 0.86 dB at 2.4 GHz, the matching is not feasible for this transistor and the same performance can be achieved with no matching at the output. The same holds for the input side. This is a great advantage of the analyzed HCBT.

PA classes with higher efficiency

All the preceding results are measured for the bias point set for Class-A operation; neither the collector-emitter voltage nor the collector current waveforms experience clipping up to a maximum linear output power. The collector efficiency of 30% is much lower than the ideal Class-A efficiency of 50% due to the negative impact of the V_{knee} voltage. Increasing the efficiency of operation of the transistor is the most researched area which resulted in many high-efficiency

classes of operation, the most frequently employed being the Class-AB and Class-B.

Ideally, classes AB and B are operating with the collector efficiency of $50\% - 78.5\%$ and 78.5%, respectively, and the sole reason of higher efficiency, with respect to Class-A, is the lower DC power dissipated at the collector [15]. To achieve the collector efficiency of 78.5%, Class-B bias point and load impedance are set so as to cause a half-wave rectified current waveform, whereas the voltage remains the same as in Class-A; a full sine wave. In other words, the DC collector current is set to 0 mA when there is no input signal applied, but the transistor is turned on by the input signal amplitude. Hence, the collector current is of a half-wave rectified waveform. The DC collector current, thus, depends on the amplitude of the input signal and is given by

$$I_{\mathrm{CQ}} = \frac{I_{\mathrm{C}}}{\pi}, \tag{2.23}$$

where $I_{\mathrm{C,max}}$ is the peak value of the collector current. For example, if the peak value is 1 mA, the DC collector current would equal 0.32 mA, whereas for Class-A operation, equals 0.5 mA. This is the main reason of increased efficiency in classes AB and B with respect to Class-A. If driven to maximum output voltage and current values, the collector efficiency of Class-B PA is

$$\eta_{\text{Class-B}} = \frac{\frac{1}{8} I_{\mathrm{Cmax}} V_{\mathrm{CEmax}}}{\frac{1}{2\pi} I_{\mathrm{Cmax}} V_{\mathrm{CEmax}}} = \frac{\pi}{4} \cdot 100\% = 78.5\%. \tag{2.24}$$

Since the DC collector current for Class-AB is somewhere in between the Class-A and Class-B, the collector efficiency of Class-AB operation is in the range from 50% to 78.5%. From (2.5), the previous discussion holds if the output power is the same as in Class-A. Indeed, the output power of the Class-A and Class-B PAs is the same, regardless of the half-wave rectification of the current waveform in Class-B operation. Namely, the collector in Class-AB and Class-B requires parallel resonant circuit of high quality factor at the fundamental frequency in order to short the voltage harmonics generated due to the current waveform to ground. In other words, if the voltage waveform is a pure sine wave of the fundamental frequency f_0, the stated ideal collector efficiencies are achieved. On the other hand, the short-circuit condition for all harmonics is seldom achieved in practical PA design due to the difficulty of implementing a broadband short-circuit with real components; be it lumped or distributed elements. Regardless, the increase in collector efficiency is achieved to some degree solely by decreasing the DC collector current in the linear, small-signal input power range.

To that end, the HCBT is analyzed for lower values of DC collector current of 20 mA and 0 mA, which correspond to Class-AB and Class-B operation, respectively. The same measurement methodology is employed as for the Class-A in the preceding discussion. The optimal load impedances for maximum output power and collector efficiency for Class-A, AB, and B,

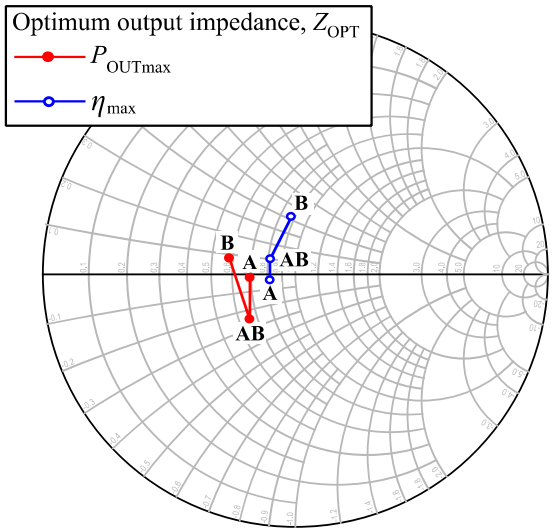


Figure 2.7: Optimal load impedances for maximum output power and collector efficiency for Class-A, Class-AB, and Class-B operation, at 2.4 GHz. The DC collector current in Class A, AB, and B, is set to 55 mA, 20 mA, and 0 mA, respectively, whereas the DC collector-emitter voltage is the same for all three and equals 2.87 V.

are shown in Fig. 2.7 at the fundamental frequency of 2.4 GHz. The optimal impedances for both output power and collector efficiency are again close to 50 Ω, but the difference between the optimum for maximum output power and collector efficiency is larger for Class-AB and Class-B, with respect to Class-A. Thus, it may be more difficult to achieve simultaneously maximal output power and collector efficiency in these classes. Nevertheless, the optimal input impedances are found with the transistor matched by the optimal load impedance for maximum output power. Then, the swept-power measurements are performed and 1-dB compression points are found in each class of operation.

The output power, collector efficiency, and gain in 1-dB compression point (P1dB) are shown in Fig. 2.8. The HCBT is matched by the optimum source and load impedances for maximum output power. As shown in [15], the output power for the three classes is similar and exactly equal for Class-A and Class-B. For Class-AB, the output power even increases somewhat due to the impact of the harmonics at the output. The same behaviour is measured for the analyzed HCBT, namely, the output power in the compression point is 17.7 dBm for both Class-A and Class-B, whereas the transducer gain is 9.62 dB and 6.53 dB, respectively. Ideally, the gain of the Class-B PA is 6 dB lower than the Class-A one, since the transistor should be driven with a 6-dB higher input power to reach the same output power as in Class-A. The reason for this higher input power is the need to increase the amplitude of the input signal twice so that the collector current swings again to the maximum value of I_{Cmax}, as in Class-A. This can be expressed by

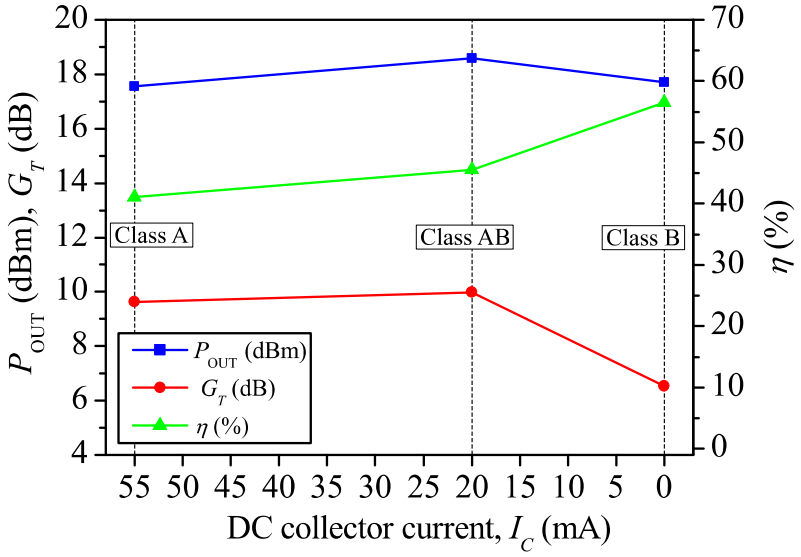


Figure 2.8: Output power P_{OUT}, collector efficiency η, and transducer gain G_{T} in 1-dB compression point (P1dB) for Class-A, Class-AB, and Class-B operation, at 2.4 GHz. The HCBT is matched by the optimum source and load impedances for maximum output power.

$$\frac{P_{\mathrm{IN}}^{\mathrm{B}}}{P_{\mathrm{IN}}^{\mathrm{A}}} = \frac{\frac{1}{2}\frac{(2I_{\mathrm{s}})^2}{R_{\mathrm{s}}}}{\frac{1}{2}\frac{(I_{\mathrm{s}})^2}{R_{\mathrm{s}}}} = 4 = 6\ \mathrm{dB}, \tag{2.25}$$

where $P_{\mathrm{IN}}^{\mathrm{B}}$, $P_{\mathrm{IN}}^{\mathrm{B}}$, I_{s}, and R_{s}, are available input power for Class-A and Class-B, source current amplitude, and source resistance, respectively. Nevertheless, the HCBT achieves the same output power of Class-A mode with only 3 dB lower gain. This behaviour is the result of the knee voltage and the fact that the harmonics are not shorted to ground. The downside is the collector efficiency of 56.5%, which is lower than the ideal value of 78.5%. Regardless, the collector efficiency is increased by 15% for the same output power.

An interesting behaviour is observed for Class-AB, where the output power in P1dB of 18.6 dBm is achieved with the collector efficiency of 46% and gain of 9.98 dB. Although a higher input power is needed for the same output power as in Class-A, the gain also increased by 0.36 dB in Class-AB. This performance exceeds both Class-A and Class-B operation thus presenting the optimum for the maximum current and voltage values I_{Cmax} and V_{CEmax} determined from Fig. 2.3.

The measurements performed so far assume the maximum collector current of 100 mA and maximum collector-emitter voltage of 5 V. To investigate the possibility of providing higher linear output powers of above 20 dBm, the transistor is analyzed for higher DC collector current and collector-emitter voltage of 75 mA and 5.5 V, respectively. Additionally, the measurements provide an indication of robustness of the transistor while operating with high DC and RF currents and voltages, since this point is far into the impact ionization region of the output DC characteristics. The current and voltage in bias point are increased and the optimal source and

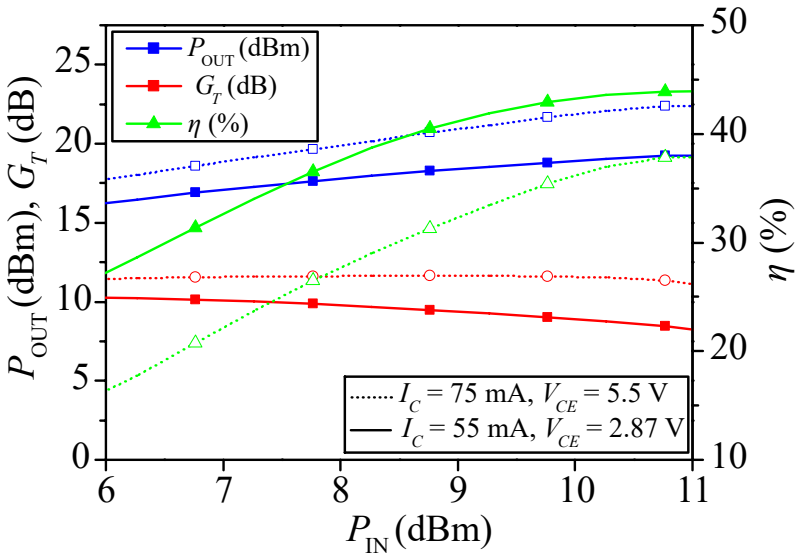


Figure 2.9: Output power P_{OUT}, collector efficiency η, and transducer gain G_{T} as a function of input power P_{IN}, at 2.4 GHz. The HCBT is matched by the optimum source and load impedances for maximum output power. The results shown for two bias points marked with solid (55 mA, 2.87 V) and dashed (75 mA, 5.5 V) lines.

load matching impedances are found, which are $Z_{\mathrm{L}} = 40.9\ \Omega$ and $Z_{\mathrm{S}} = 32.8 - j6.9\ \Omega$. Then the swept-power measurements are performed, which are shown in Fig. 2.9. For the maximum input power of 11 dBm, the HCBT achieves an output power of 22.6 dBm, the collector efficiency of 37.9%, and gain of 10.9 dB. Although the output power and gain are higher with respect to the lower bias point, the collector efficiency is lower by around 5%. Furthermore, the efficiency is even lower in the linear range, where the difference in efficiency is around 10%. Thus, the HCBT can reliably sustain much higher power than 18 dBm, but with a somewhat lower collector efficiency.

2.4 Impact of collector doping on large-signal performance

So far, one HCBT type is analyzed by load-pull and source-pull measurements, but the large-signal performance depends on the technology parameters of the transistor, such as doping profiles and geometry. By varying the technology parameters, the parameters of the transistor relevant for large-signal operation can be tweaked to a desired value, and, in that way, the device can be tailored to a specific PA application, e.g., high-voltage, high-current, high-efficiency, or high-gain PAs. Furthermore, the same technology parameters can be optimized to result in a more robust device for the application in, e.g., military-grade power amplifiers. The HCBT technology offers much flexibility in the device optimization by varying the collector doping profile in order to optimize both the breakdown voltage and maximum collector current; the parameters which determine the performance of the PA to a high degree. Therefore, the impact

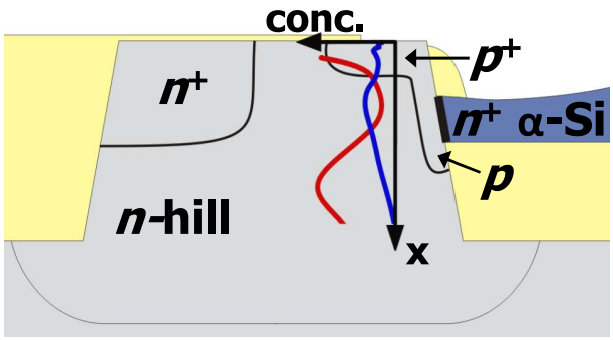


Figure 2.10: Collector doping profiles schematically shown on the simplified cross-section of the HCBT structure. The profiles shown are for the HCBT with a collector doping profiles defined by the CMOS *n*-well step (red curve) and the HCBT with an uniform *n*-collector (blue curve). The doping profile for the HCBT with a low-doped *n*-collector is the same as the one for uniform *n*-collector, except shifted to lower doping concentrations.

of collector doping profile on large-signal operation of HCBT is analyzed, employing the load-pull setup from Fig. 2.1.

The three variants of HCBT are analyzed by load-pull measurements at the fundamental frequency of 0.9, 1.8, and 2.4 GHz. The HCBTs differ in collector doping profile, and they are

- HCBT 1 with an uniformly doped *n*-collector,
- HCBT 2 with the *n*-collector defined by the CMOS *n*-well process step, and
- HCBT 3 with a low-doped *n*-collector.

The collector doping profiles are schematically shown for the three devices in Fig. 2.10. The doping profiles determine to a large extent the characteristics of the three HCBTs. The HCBT 2 has the highest collector doping concentration, whereas the HCBT 3 has the lowest one. The HCBT 1, on the other hand, has a doping concentration between the two. This doping concentration determines both the breakdown voltage and the maximum collector current to which the transistor can be operated.

In terms of RF circuit performance, the HCBT with the uniform *n*-collector demonstrated the most appropriate characteristics for the high-linearity RF mixer design [84]. On the other hand, the noise figure analysis showed that the HCBT with the low-doped *n*-collector is more appropriate for the low-noise amplifier design in terms of the noise-gain trade-off [76]. Furthermore, the circuits designed with low-cost HCBT version, which needs one lithography mask less for the collector doping profile definition, also have competitive characteristics. Thus, different technology parameters result in devices of different RF performance and the optimum is next investigated for large-signal applications.

2.4.1 Transistor electrical parameters

The most important parameters of the three analyzed transistors are shown in Tab. 3.1. The devices are of the same emitter area of $A_{\mathrm{E}} = 45 \cdot (0.1 \cdot 13) = 58.5\ \mu\mathrm{m}^2$. The parameters are ex-

tracted from DC and small-signal RF measurements performed on the on-wafer devices, i.e., the unpackaged devices. Due to the difference in the collector doping concentration, the electrical parameters vary between the devices. The DC current gain in the common-emitter configuration, β, is the highest for HCBT 1 and the lowest for HCBT 3. On the contrary, the HCBT with the highest collector doping concentration, HCBT 2, achieves the highest transition frequency f_T of 35 GHz, which is measured at $V_{CE} = 2$ V. The opposite holds for breakdown voltages; the HCBT 2 has the lowest breakdown voltages BV_{CEO} and BV_{CBO} of 2.8 V and 8.3 V, respectively. The breakdown voltages are the highest for the low-doped HCBT 3, which has BV_{CEO} and BV_{CBO} of 5.2 V and 9 V, respectively. Additionally, the device with lowest collector doping concentration, HCBT 3, has the lowest base-emitter capacitance of 280 fF, which is extracted at $V_{CB} = 1$ V. The transistors have similar BV_{CBO} since the collector-base breakdown occurs in the extrinsic transistor region and is mainly determined by the n^+ -collector/extrinsic base distance, which is the same for all devices. Additionally, the HCBT 3 has the highest collector resistance R_C which results in the highest saturation voltage, i.e., knee voltage V_{knee}. The highest capacitance of 480 fF has the device with the highest doping concentration, HCBT 2. The parasitic electrode resistances of the base and emitter can impact the value of the optimal source impedance, and the stability of the device as well. The highest resistance $R_E + R_B$ of 12 Ω has the HCBT 3. The HCBT 1 has an uniform profile in the intrinsic transistor along the vertical cross-section and its characteristics are in-between the HCBT 2 and HCBT 3 [75].

Table 2.1: Measured electrical parameters of the HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector).

	HCBT 1	HCBT 2	HCBT 3
Emitter area	$45 \cdot (0.1 \cdot 13)\ \mu m^2$		
Peak β	150	120	110
f_T (GHz) ($V_{CE} = 2\ V$)	30	35	18
BV_{CEO} (V)	3.3	2.8	4.8
BV_{CBO} (V)	8.6	8.3	9
C_{BC} (fF) ($V_{CB} = 1$ V)	380	480	280
$R_E + R_B$ (Ω) ($I_C = 20$ mA)	7	8	12

The electrical parameters extracted from small-signal *S*-parameter measurements can serve as an indication of a large-signal performance of the device. For example, a device with higher transition frequency has a higher gain with respect to the device with lower f_T, at the same frequency. Furthermore, a device with higher DC current gain needs lower base current for the same collector current, thus decreasing the DC power dissipation and increasing the collector efficiency in large-signal operation.

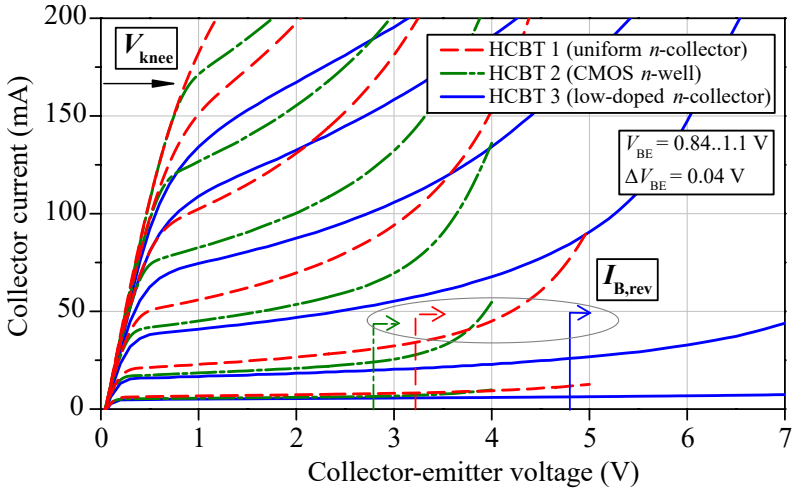


Figure 2.11: Output DC characteristics of HCBT 1 (red dashed curves), HCBT 2 (green dash-dot curves), and HCBT 3 (blue solid curves), with constant base-emitter bias of $V_{\mathrm{BE}} = [0.84 - 1.1]$ V. The onset of the base-current reversal I_{Brev} at $V_{\mathrm{BE}} = 0.84\ V$ shown with the arrows.

2.4.2 DC characteristics

The output DC characteristics are again measured and shown in Fig. 2.11 for the three transistors [85]. The output characteristics are measured for the same base-emitter voltage V_{BE} in the range from 0.84 V to 1.1 V, with the step of 0.04 V. It is clear that the devices differ in the collector current for the same V_{BE}, due to the difference in base width and doping concentration, which then causes the difference in DC current gain β. Since HCBT 3 has the highest breakdown voltage, the output curves are measured up to V_{CE} of 7 V for HCBT 3, whereas for HCBT 1 and HCBT 2, to 5 V and 4 V, respectively. The reason for this is the onset of breakdown region, i.e., the impact ionization and subsequent rapid increase in collector current. This phenomena occurs already for $V_{\mathrm{CE}} \approx 3.5$ V for HCBT 2 and for $V_{\mathrm{CE}} \approx 4.5$ V for HCBT 1. The HCBT 3 experiences gradual increase in collector current up to $V_{\mathrm{CE}} \approx 5.5$ V, and, thus, can be reliably operated to higher collector-emitter voltages than the other two transistors.

The separation between the output characteristics of the same transistor can indicate the presence of some second-order effects, the most important one being the Kirk effect. The Kirk effect reduces the separation between the output curves and, therefore, induces the nonlinearity to the load line in large-signal operation. Since the effect appears gradually for high collector currents, the Kirk effect is usually defined at the current and voltage at which the separation between the curves decreases with respect to the exponential dependence of I_{C} on V_{BE}. This effect occurs for the collector current of around 150 mA in the low-doped device, HCBT 3. On the other hand, the HCBT 2 does not experience this effect for the measured currents of up to 200 mA, due to the high doping of the collector, which pushes the Kirk effect to higher collector currents, as shown in [61]. The HCBT 2 experiences the Kirk effect at the collector current of around 200 mA. Such nonlinearity impacts the load line, and because of that, usually represents

the maximum collector current for a linear operation of the bipolar transistor.

The Kirk effect limits the maximum collector current excursion in large-signal operation, whereas the breakdown voltage limits the collector-emitter voltage. To that end, the onset of base-current reversal, marked I_{Brev}, at the base-emitter voltage of 0.84 V is also measured. The collector-emitter voltage at the point of base-current reversal is the open-base breakdown voltage $\mathrm{BV_{CEO}}$. Since the base-emitter junction is biased with a voltage source, the transistors can be operated reliably even higher than the $\mathrm{BV_{CEO}}$ [86], since the base current created due to the impact ionization can flow out of the base and to the ground.

2.4.3 Load-pull analysis

The transistors HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), are characterized by load-pull measurements using the automated load-pull setup from Fig. 2.1.

Bias points

Firstly, the bias points to be used in load-pull characterization are determined for the three transistors. Since the devices have different breakdown voltages and maximum collector currents, the bias points are chosen such that each device utilizes both the maximum current and voltage swings at the collector.

The DC collector current is determined by analyzing the maximum power gain G_{pmax} of the devices. The definition of the maximum power gain depends on the stability of the measured device; if the active device is unconditionally stable ($K > 1$), a maximum transducer power gain is defined by [14]

$$G_{\mathrm{Tmax}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}), \tag{2.26}$$

whereas for $K < 1$, a maximum stable gain is defined by

$$G_{\mathrm{msg}} = \frac{|S_{21}|}{|S_{12}|}, \tag{2.27}$$

where K is the Rollet's stability factor. Considering the results in Fig. 2.12, the maximum power gain consists of both the maximum transducer power gain and maximum stable gain, depending on the K factor in each bias point. The maximum power gain can be analytically calculated from the electrical parameters of the transistor as

$$G_{\mathrm{pmax}} = \frac{f_{\mathrm{T}}^2}{8\pi C_{\mathrm{BC}} R_{\mathrm{B}} f^2}, \tag{2.28}$$

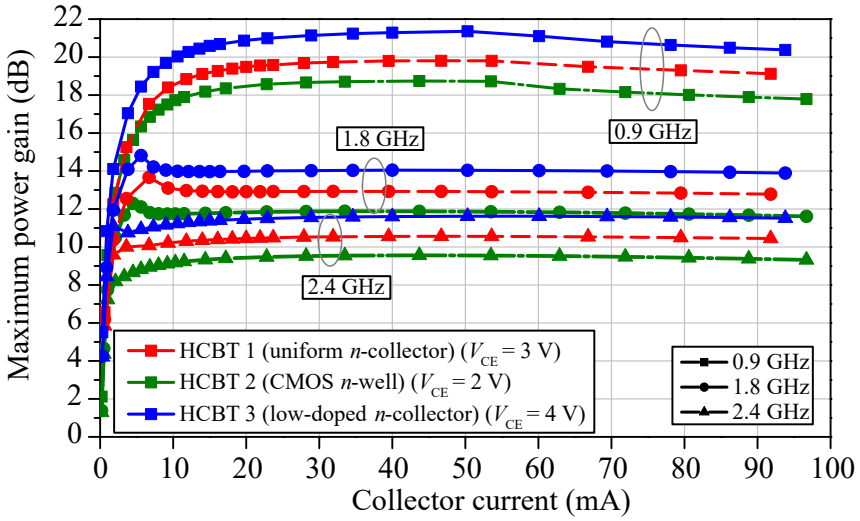


Figure 2.12: Measured maximum power gain as a function of collector current at 0.9 GHz, 1.8 GHz, and 2.4 GHz, of the three HCBT devices: HCBT 1 (uniform n-collector), HCBT 2 (CMOS n-well), and HCBT 3 (low-doped n-collector). The maximum power gain characteristics consist of maximum transducer power gain G_{Tmax} and maximum stable gain G_{msg}.

where f is the operating frequency, whereas the other quantities are given in Tab. 3.1. Since the DC collector current is not a parameter in (2.28), the G_{pmax} is measured as a function of DC collector current for the three devices, and the results are shown in Fig. 2.12. Although the DC collector-emitter voltage is not yet determined, the values of 2 V, 3 V, and 4 V, are selected for the maximum power gain measurement for HCBT 2, HCBT 1, and HCBT 3, respectively. The collector current is swept from 0 mA to 100 mA and the maximum power gain is measured at 0.9 GHz, 1.8 GHz, and 2.4 GHz.

At all three fundamental frequencies, the HCBT 3 exhibits the highest small-signal gain. Namely, at 0.9 GHz, 1.8 GHz, and 2.4 GHz, the HCBT 3 achieves 21.3 dB, 14 dB, and 11.6 dB, respectively, for the collector current of 40 mA. Although this transistor does not have the highest transition frequency f_{T}, it achieves the highest gain due to the smallest base-collector capacitance C_{BC} of 280 fF [see Tab. 3.1]. As can be seen from (2.28), the maximum power gain is a function of the f_{T}^2 and $\frac{1}{C_{\mathrm{BC}}}$, and the prevalent quantity which determines the gain can be both, depending on the characteristics of the device and the operating frequency f. Interestingly, the device with the highest f_{T}, HCBT 2, has the lowest maximum power gain of 18.2 dB, 11.8 dB, and 9.6 dB, at 0.9 GHz, 1.8 GHz, and 2.4 GHz, respectively, for the collector current of 70 mA. For HCBT 1, the parameters f_{T} and C_{BC} are in between the values of HCBT 2 and HCBT 3, resulting in the maximum power gain of 19.9 dB, 12.5 dB, and 10.6 dB, at 0.9 GHz, 1.8 GHz, and 2.4 GHz, respectively, for the collector current of 50 mA.

The performance considering the maximum power gain is stated for 50 mA, 70 mA, and 40 mA, for HCBT 1, HCBT 2, and HCBT 3, respectively. The reason is that these collector currents are the optimum values for the respective transistors, considering the onset of Kirk

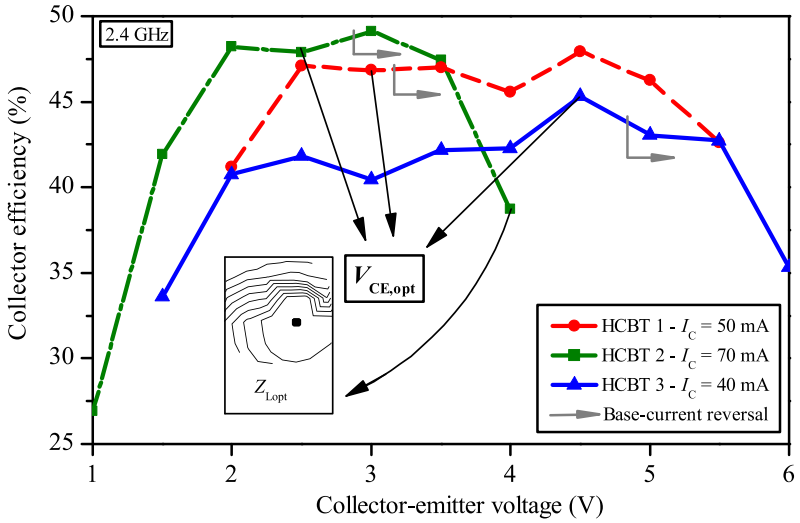


Figure 2.13: Measured collector efficiency in 1-dB compression point for HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low doped *n*-collector), at 2.4 GHz, as a function of DC collector-emitter voltage. The DC collector currents are 50 mA, 70 mA, and 40 mA, for HCBT 1, HCBT 2, and HCBT 3, respectively. The V_{CEopt} is the optimal DC collector-emitter voltage. The arrows mark the base-current reversal. The non-oval load-pull contours due to the pinch-in phenomenon shown in the inset. The $\Gamma_S = \Gamma_{Sopt}$ and $\Gamma_L = \Gamma_{Lopt}$ for each collector-emitter voltage.

effect, which can be inferred to some degree from the output DC characteristics in Fig. 2.11. Although the maximum power gain does not change significantly with DC collector current thus providing mainly flat $G_{pmax}(I_C)$ characteristics and, thus, the maximum collector current could be chosen to achieve as high as possible output power, the DC collector currents are chosen in order to stay away from the Kirk effect and achieve linear operation in large-signal regime. Thus, the currents are conservatively chosen to be 50 mA, 70 mA, and 40 mA, for the respective devices.

Once the DC collector currents are chosen, the DC collector-emitter voltage are selected for each device. Since the currents are determined from small-signal measurements shown in Fig. 2.12, the collector-emitter voltage in bias point is selected by considering the large-signal performance of the devices in the selected bias collector currents. Namely, the DC collector currents are set to 50 mA, 70 mA, and 40 mA for HCBT 1, HCBT 2, and HCBT 3, respectively, and the large-signal performance is measured for increasing DC collector-emitter voltage to find the best bias point for the large-signal performance, as shown in Fig. 2.13. The collector-emitter voltage is increased in step of 0.5 V. For each voltage, swept-power, load-pull, and source-pull measurements are made, to find the optimum source and load matching impedance for maximum output power. Once the transistors are matched with the optimal impedances, the swept-power measurements are again measured and the 1-dB compression point is identified. The collector efficiency is then measured in P1dB and shown in Fig. 2.13. Even though the efficiency is measured, the transistors are matched with the optimum load impedances for maximum output power, since the goal is to extract the maximum output power out of each tran-

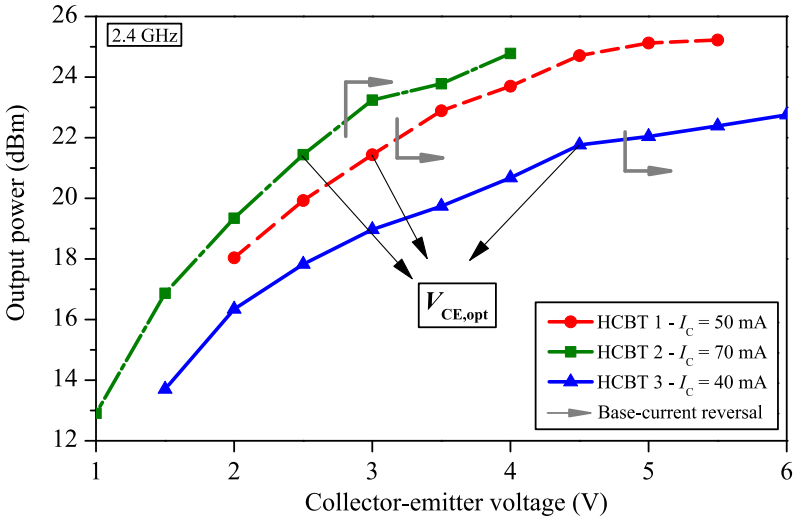


Figure 2.14: Measured output power in 1-dB compression point for HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low doped *n*-collector), at 2.4 GHz, as a function of DC collector-emitter voltage. The bias points are (50 mA, 3 V), (70 mA, 2.5 V), and (40 mA, 4.5 V), for HCBT 1, HCBT 2, and HCBT 3, respectively. The V_{CEopt} is the optimal DC collector-emitter voltage. The arrows mark the base-current reversal. The $\Gamma_S = \Gamma_{Sopt}$ and $\Gamma_L = \Gamma_{Lopt}$ for every collector-emitter voltage.

sistor, but, at the same time, achieve the highest collector efficiency with the transistor matched by Γ_{Lopt}. The range of collector-emitter voltage is different for each device, since the region of maximum collector efficiency occurs for different voltages in the three devices. Therefore, the collector-emitter voltage is set to $[2-5.5]$ V, $[1-4]$ V, and $[1.5-6]$ V, for HCBT 1, HCBT 2, and HCBT 3, respectively.

The collector efficiency characteristics exhibit a voltage range of maximum efficiency, which can be identified for each device; $[2.5-5]$ V, $[2-2.5]$ V. and $[2-5.5]$ V, for HCBT 1, HCBT 2, and HCBT 3, respectively. The drop in collector efficiency for low collector-emitter voltage occurs due to the saturation region. Namely, the load line experiences increasingly smaller voltage and current swing, due to the nonlinearity present when penetrating the saturation region. This results in decrease of collector efficiency when the bias point is in the saturation region. On the other hand, the drop in collector efficiency for high collector-emitter voltage occurs due to the bias point being set in the impact ionization region, wherein the DC collector current increases with increasing input power rapidly. Additionally, the pinch-in phenomenon occurs for high collector-emitter voltages, and it is even visible in the load-pull measurements; the load-pull contours are not oval-shaped, but experience kinks for some load impedance ranges. The two extremes enclose a collector-emitter voltage range of maximum collector efficiency. The maximum collector efficiency are 49%, 47%, and 45%, for HCBT 1, HCBT 2, and HCBT 3, respectively. The results, thus, suggest a weak Class-AB configuration for all three transistors.

The DC collector-emitter voltages for the load-pull analysis are chosen considering the breakdown voltage BV_{CEO}. The breakdown voltage is marked at the collector-emitter voltage of base-current reversal. Since the base-current reversal occurs in the maximum collector

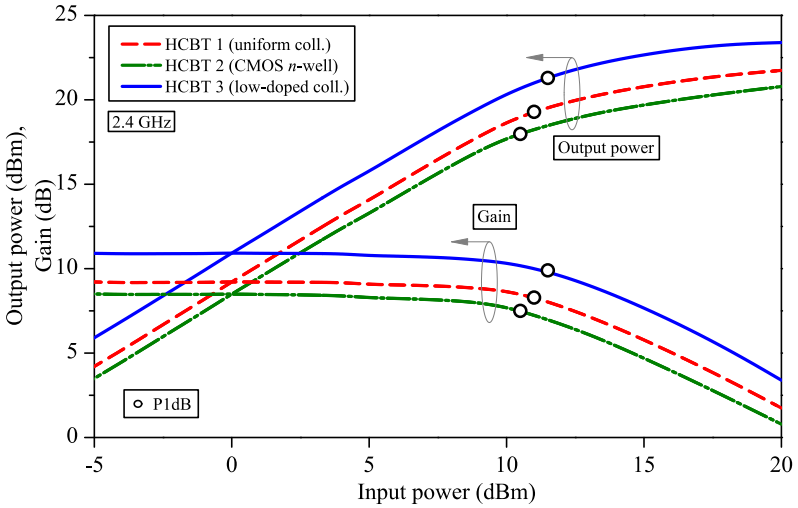


Figure 2.15: Measured output power and transducer gain of HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), at the fundamental frequency of 2.4 GHz, for the source and load impedance of 50 Ω. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

efficiency range, the DC collector-emitter voltage is selected lower than $\mathrm{BV_{CEO}}$, whereas still in the range of maximum collector efficiency. Thus, the DC collector-emitter voltages for the subsequent load-pull analysis are 3 V, 2.5 V, and 4.5 V, for HCBT 1, HCBT 2, and HCBT 3, respectively. Therefore, the DC bias points $\mathrm{Q} = (I_{\mathrm{CQ}}, V_{\mathrm{CEQ}})$ for the three analyzed devices are

- HCBT 1 - (50 mA, 3 V),
- HCBT 2 - (70 mA, 2.5 V), and
- HCBT 3 - (40 mA, 4.5 V).

Additionally, the output power is measured as a function of the DC collector-emitter voltage, as shown in Fig. 2.14, to verify the selection of the DC bias points. Since the DC collector current is constant and the collector-emitter voltage is increased, the output power increases linearly (the *y*-axis is in logarithmic scale). The output power in 1-dB compression point of around 20.4 dBm is achieved for all three transistors in their respective bias points. Furthermore, the output powers of up to 25 dBm can be achieved when operated above the $\mathrm{BV_{CEO}}$, which is a great advantage of bipolar transistors for RF applications [86]. It should be emphasized that the load line swings above the $\mathrm{BV_{CEO}}$, since the DC point is set just below the base-current reversal. Regardless, a reliable operation is achieved for all three transistors.

Swept-power measurements for $Z_{\mathrm{S}} = Z_{\mathrm{L}} = 50\ \Omega$

To find the optimal input power for load-pull analysis, the swept-power measurements are performed for the source and load impedances equal to 50 Ω at the fundamental frequency of 2.4 GHz. The input power is swept from -5 dBm to 20 dBm to cover both the linear and compression regions. Considering the linear region, i.e. the input power range of up to 10 dBm,

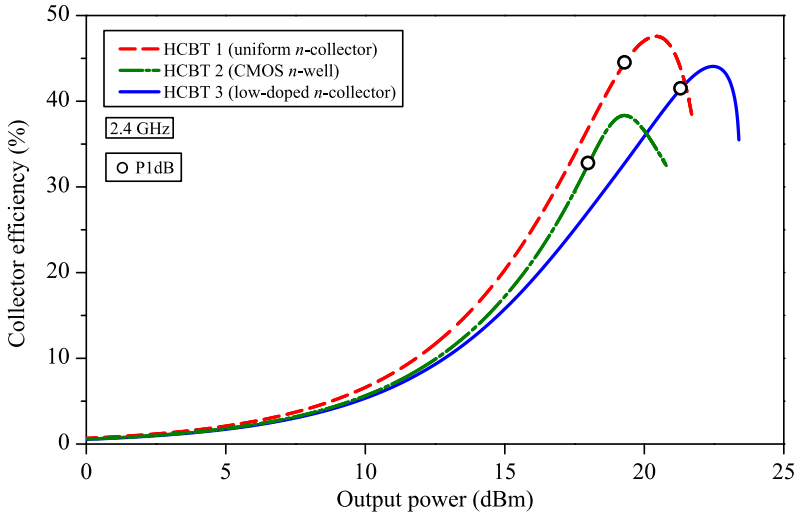


Figure 2.16: Measured collector efficiency of HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), at the fundamental frequency of 2.4 GHz, for the source and load impedance of 50 Ω. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

the relative difference in gain for the three transistors is the same as the one extracted from *S*-parameter measurements in Fig. 2.14, but the absolute values are different since the results from Fig. 2.14 present the performance of the conjugately matched transistors. Yet, the performance in Fig. 2.15 is relatively close to the one of the matched transistors, suggesting that the optimal impedances are again close to 50 Ω. The HCBT 3 exhibits the highest output power and gain of 21.3 dBm and 9.9 dB, respectively, in 1-dB compression point. The transducer gain of HCBT 1 and HCBT 2 is 8.3 dB and 7.5 dB, respectively.

The collector efficiency for the unmatched transistors is shown in Fig. 2.16 at 2.4 GHz. Since the DC collector current varies with the input power in the compression region and the output power saturates, the collector efficiency is a strong function of the bias point, as seen from (2.5). The optimal bias points for the three transistors are different with respect to DC collector current in the small-signal range, and the behaviour in large-signal power range also differs. Namely, the collector efficiency in the linear range is low for all three devices, wherein for the output power of 0 dBm, the efficiency is around 1%. When the input power increases, the devices experience the DC bias point shift due to a change in collector current, and the denominator in (2.5) changes, which causes the collector efficiency change. For the source and load impedances of 50 Ω, the HCBT 1 achieves the highest collector efficiency of 44.5% in P1dB, whereas HCBT 2 and HCBT 3 achieve 32.8% and 41.5%, respectively, but the maximum collector efficiency for the three transistors occurs further into the compression region. Although HCBT 1 achieves the highest efficiency, the HCBT 3 achieves the highest output power, whereas the HCBT 2 achieves the lowest. The difference is due to the chosen optimum bias points and the 50 Ω load line; the HCBT 2 has the smallest voltage swing of around 1.5 V at the collector, which causes the lowest output power in P1dB among the three devices. Nevertheless, the

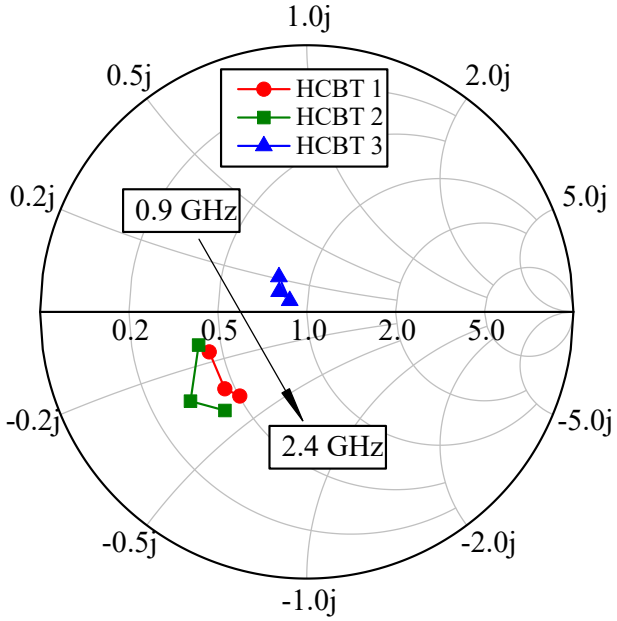


Figure 2.17: Optimal load impedances of HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), at the fundamental frequency of 0.9 GHz, 1.8 GHz, and 2.4 GHz. The source impedance is set to Γ_{Sopt} for each transistor. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

current swing is the highest, but the load line is far from optimal for the HCBT 2. Regarding the output power, the HCBT 3 operates the best with the 50 Ω matching on the output, and it achieves output power of 21.5 dBm, whereas the HCBT 1 and HCBT 2 achieve 19 dBm and 17.6 dBm, respectively. The results suggest that the HCBT 3 has the optimal load impedance close to 50 Ω.

Performance of the matched transistors

Next, the load-pull is performed to find the optimal source and load impedances for the previously determined optimal bias points. The transistors are brought to P1dB for the 50 Ω match, as shown in Fig. 2.16, and the load impedance is first varied but with the 50 Ω source impedance. Once the optimal load impedances are found, the source-pull is performed to maximize the gain of the devices. The optimal load impedances are shown in Fig. 2.17, at the fundamental frequency of 0.9 GHz, 1.8 GHz, and 2.4 GHz. For the optimal bias points, the transistors exhibit optimal impedances near 50 Ω. As suggested by the results shown in Fig. 2.16, the HCBT 3 has the optimal load impedance close to 50 Ω, exhibiting a reactance of only 6.2 Ω at 2.4 GHz. The optimal load resistances for HCBT 1 and HCBT 2 are 25 Ω and 20 Ω, respectively. Furthermore, the optimal load impedances for the HCBT 1 and HCBT 2, lie on the circles of constant resistance, thus, providing the same resistance at all frequencies. The vicinity of the optimal impedance to 50 Ω for the HCBT 3, enables simple matching network design [14]. Such a matching network has a low transformation ratio and the capacitors and

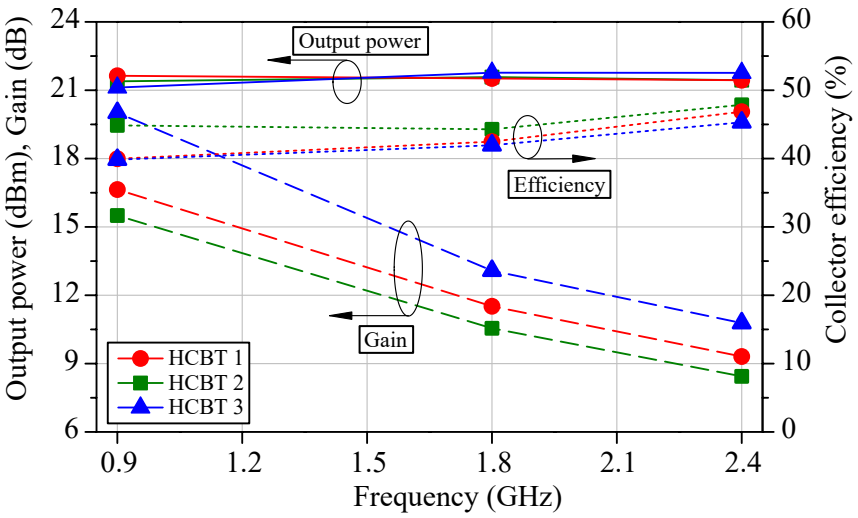


Figure 2.18: Measured output power (solid lines), gain (dashed lines), and collector efficiency (dotted lines), in 1-dB compression point, for HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), at the fundamental frequency of 0.9 GHz, 1.8 GHz, and 2.4 GHz. For each transistor, $\Gamma_S = \Gamma_{Sopt}$ and $\Gamma_L = \Gamma_{Lopt}$. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

inductors of small values, since the terminal impedances are similar, and large bandwidth, as given by

$$\mathrm{BW} = \frac{f_0}{\frac{X}{R}}, \tag{2.29}$$

where f_0, X, and R, are the fundamental frequency, reactance of the matching network, and resistance of the matching network, respectively. Thus, the HCBT 3 can be employed without the matching network at the output and still provide the optimal performance. This further lowers the insertion loss at the output and increases the output power, gain, and collector efficiency, of the power amplifier.

Once the optimal load and source impedances for maximum output power are found, the large-signal performance is measured at all three frequencies. The output power, gain, and collector efficiency in 1-dB compression point are shown in Fig. 2.18. Due to the optimal matching at the output, the output power is around 21.4 dBm for all three transistors. The HCBT 2 has the lowest gain, but the highest efficiency, reaching 47.9% at 2.4 GHz. The HCBT 3 provides the highest gain of up to 20 dB at 0.9 GHz, with the similar output power and collector efficiency performance. The difference in collector efficiency is mainly the result of the slight difference in saturation voltage, which is the lowest for HCBT 2, since it has the highest collector doping concentration. The HCBT 3 exhibits the best overall performance, since it can be employed without a matching network at the output.

To verify this, the large-signal performance at 0.9 GHz, 1.8 GHz, and 2.4 GHz, is measured for the source and load impedances of 50 Ω. The output power of HCBT 3 remains at the

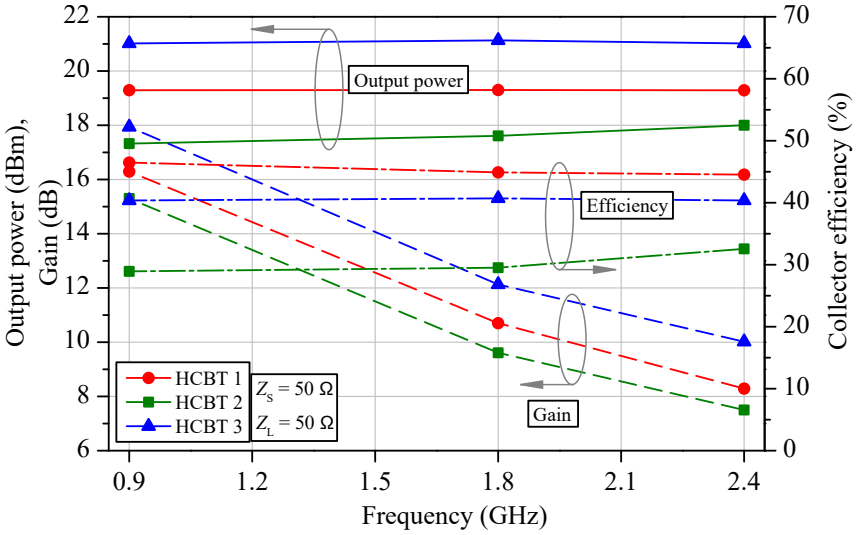


Figure 2.19: Measured output power (solid lines), gain (dashed lines), and collector efficiency (dotted lines), in 1-dB compression point, for HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), at the fundamental frequency of 0.9 GHz, 1.8 GHz, and 2.4 GHz. For each transistor, $\Gamma_S = 50\ \Omega$ and $\Gamma_L = 50\ \Omega$. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

maximum value of 21.4 dBm although the collector is matched by 50 Ω. On the other hand, the output power for HCBT 1 and HCBT 2 drops to around 19.1 dBm and 18 dBm, respectively, which is twice the lower output power with respect to the maximum value. Similarly, the gain decreases by 3 dB for HCBT 1 and HCBT 2, whereas it stays at the maximum value for HCBT 3. Interestingly, the collector efficiency is the highest for the HCBT 1, due to its optimal impedance for maximum collector efficiency being the closest to 50 Ω. Therefore, the HCBT technology enables the optimization of the large-signal characteristics at the device level by varying the collector doping profile.

Although the large-signal performance shown in Fig. 2.18 and Fig. 2.19 is measured for Class-A operation, the collector efficiencies achieved are too high for the Class-A operation in practice. Since the results are shown in the 1-dB compression point, the transistors already experience significant load line distortion, which suggests that the stated performance is for a different class of operation, e.g., Class-AB or overdriven Class-A [15]. To that end, the performance is also investigated for lower output power than the P1dB, in which the assumption of Class-A operation still holds. From such an analysis, a maximum linear output power can be determined, which is usually much lower output power than P1dB.

Maximum linear output power

The maximum linear output power is determined from the behaviour of DC collector current. When in small-signal regime, the collector current is constant and equal to the value set by the base-emitter and collector-emitter voltage sources. Once in compression, the collector current

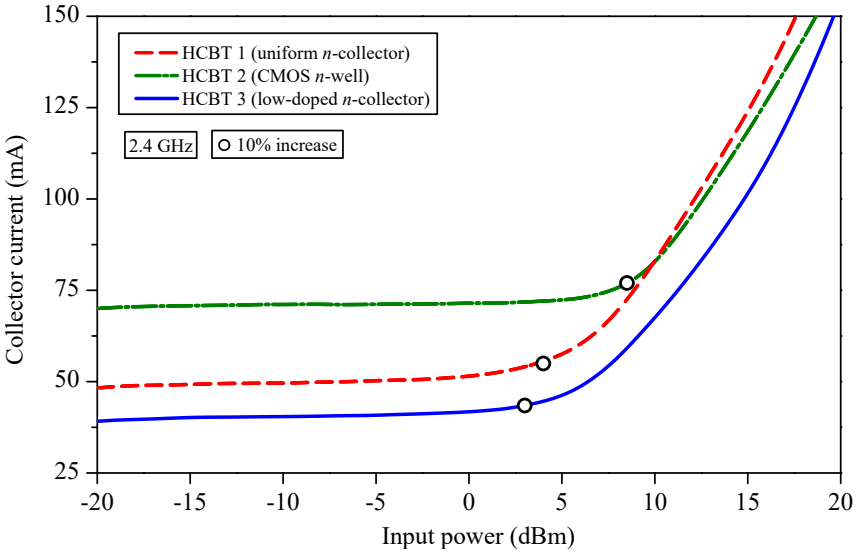


Figure 2.20: Measured DC collector current as a function of input power, for HCBT 1 (uniform *n*-collector, dashed line), HCBT 2 (CMOS *n*-well, dash-dot line), and HCBT 3 (low-doped *n*-collector, solid line), at the fundamental frequency of 2.4 GHz. For each transistor, $\Gamma_S = \Gamma_{Sopt}$ and $\Gamma_L = \Gamma_{Lopt}$. The bias points are: HCBT 1 (50 mA, 3 V), HCBT 2 (70 mA, 2.5 V), and HCBT 3 (40 mA, 4.5 V).

RF waveform experiences distortion. The distortion incurs the shift in DC collector current, e.g., an increase in DC current for the transition from Class-A to Class-AB operation. Therefore, this shift is identified for the three analyzed transistors matched by the optimal matching impedances shown in Fig. 2.17. More precisely, a relative increase in DC collector current of 10% is defined as a point of maximum linear output power.

The DC collector current as a function of input power is shown in Fig. 2.20 at the fundamental frequency of 2.4 GHz, wherein the 10% increase in DC current is marked. Since the collector current monotonically increases, the waveforms at the transistors terminals experience a distortion which causes a DC bias point shift. This shift can be due to the distortion both on the input or output. Regardless, the result is the increase in DC collector current in the compression region. The 10% increase point is right at the onset of significant DC current increase, but lower than P1dB. Thus, in this point, the transistors are more linear than in P1dB. Furthermore, the values are not the same for the three transistors since the small-signal values are set to their optimal DC collector current values. Namely, for HCBT 2 the DC collector current significantly increases for the input power higher than 7 dBm, whereas for HCBT 1 and HCBT 3, for input power higher than 4 dBm and 3 dBm, respectively. The results suggest that the HCBT 2 operates linearly up to higher output powers than the other two transistors. To verify the assumption, the large-signal performance is measured for the input power of 10% DC collector current increase.

The output power, gain, and collector efficiency, are measured for HCBT 1, HCBT 2, and HCBT 3, and shown in Fig. 2.21 for input power of 4 dBm, 7 dBm, and 3 dBm, respectively. As shown also in Fig. 2.18, the gain is the lowest among the three transistors for the HCBT 3,

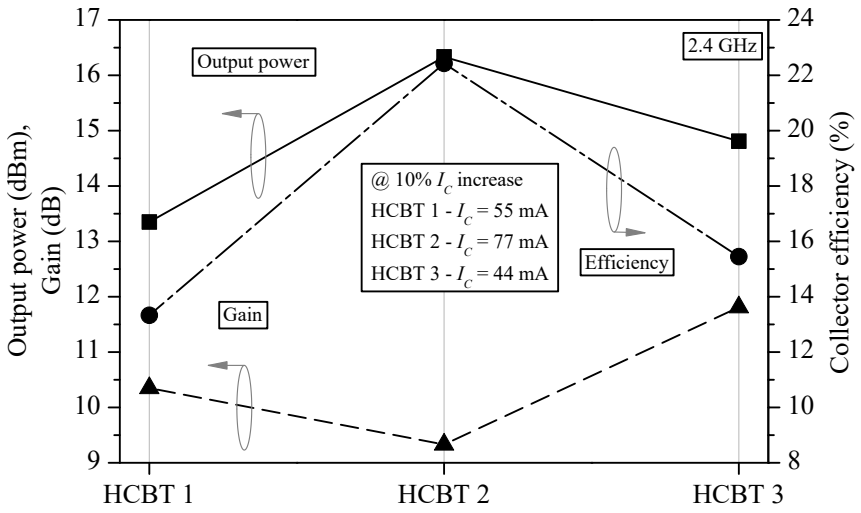


Figure 2.21: Measured output power, gain, and collector efficiency, for HCBT 1 (uniform *n*-collector), HCBT 2 (CMOS *n*-well), and HCBT 3 (low-doped *n*-collector), for the input powers of 4 dBm, 7 dBm, and 3 dBm, respectively. For each transistor, $\Gamma_S = \Gamma_{Sopt}$, $\Gamma_L = \Gamma_{Lopt}$, and $f_0 = 2.4$ GHz. The bias points are: HCBT 1 (55 mA, 3 V), HCBT 2 (77 mA, 2.5 V), and HCBT 3 (44 mA, 4.5 V).

equalling 9.5 dB, whereas the gain for HCBT 1 and HCBT 3 is 10.5 dB and 11.8 dB, respectively. On the other hand, the collector efficiency is the highest for the HCBT 2, and equals 22.4%, whereas for HCBT 1 and HCBT 3 equals 13.3% and 15.5%, respectively. Thus, the HCBT 2 operates with almost twice the efficiency than the other two transistors in the point of maximum linear power. Additionally, the HCBT 2 achieves the highest output power of 16.3 dBm. Thus, considering linearity, the HCBT 2 exhibits the best overall performance. Therefore, the maximum linear powers of the three transistors in the selected optimum bias points are

- HCBT 1 - $P_{LIN} = 13.4$ dBm,
- HCBT 2 - $P_{LIN} = 16.3$ dBm, and
- HCBT 3 - $P_{LIN} = 14.8$ dBm.

The reason for the large difference in performance in the point of maximum linear power is explained to some extent by observing the load lines for the output power P_{LIN}. Since a load line is described by

$$i_C(v_{CE}), \tag{2.30}$$

where i_C and v_{CE} are total collector current and total collector-emitter voltage, respectively, it can be analytically calculated by measuring or calculating the i_C and v_{CE}. Measurement of such quantities at RF demands a different measurement setup, but the calculation is straightforward when the load impedance, output power, and bias point, are known. From Fig. 2.20 and Fig. 2.21, all three quantities are measured, which enables the calculation of the load lines for the three transistors in the point of maximum linear output power.

If the output power and load impedance are known, the collector current amplitude can be calculated starting from the complex power as a function of the load impedance:

$$\mathbf{S} = \frac{I_C^2 \mathbf{Z}_{\mathrm{Lopt}}}{2}, \tag{2.31}$$

where $\mathbf{S}$, I_C, and $\mathbf{Z}_{\mathrm{Lopt}}$ are complex power, collector current amplitude, and optimal load impedance, respectively. Since

$$\mathbf{Z}_{\mathrm{Lopt}} = R_{\mathrm{Lopt}} + jX_{\mathrm{Lopt}}, \tag{2.32}$$

the real power P can be expressed by

$$P = \Re(\mathbf{S}) = \frac{I_C^2}{2} R_{\mathrm{Lopt}}, \tag{2.33}$$

where R_{Lopt} is a real part of the load impedance. Since real power is measured, the I_C can be found from (2.33). Once the current is known, the collector-emitter voltage can be found from

$$V_{CE} = \sqrt{2PR_{\mathrm{Lopt}}}, \tag{2.34}$$

where V_{CE} is the collector-emitter voltage amplitude. The phase angle θ between the current and voltage is given by

$$\tan\theta = \frac{X_{\mathrm{Lopt}}}{R_{\mathrm{Lopt}}}, \tag{2.35}$$

which then enables the construction of the load lines according to (2.30).

The load lines for the three transistors are shown in Fig. 2.22 for the maximum linear output power. The load lines are shown on top of the DC $I-V$ curves for the HCBT 3 for a reference. The load lines are oval-shaped curves due to the load reactance X, which is different for the three transistors. As suggested by the results shown in Fig. 2.21, the largest load line is the one of the HCBT 2, extending all the way from the cut-off to the saturation region. Contrary, the transistor with the lowest output power, HCBT 3, has the load line which does not encroach the saturation region, but extends only down to 3 V. In other words, the analysis suggests that the output power of HCBT 3 is low due to the larger impact of Kirk effect due to the low-doped collector. Additionally, the slope of the HCBT 3 load line is the closest to 50 Ω, and the one of HCBT 3 and HCBT 1 is higher due to the lower real part of the optimal load impedance.

Even though the load lines of the HCBT 1 and HCBT 3 do not look like optimal ones, since they do not extend to the saturation region and thus do not utilize the entire voltage swing available, these are the load impedances for which maximum output power is achieved. Therefore,

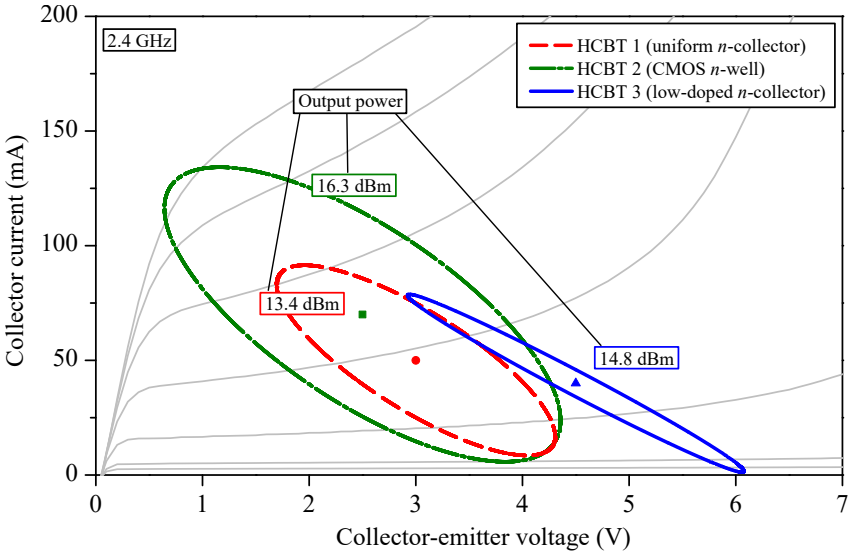


Figure 2.22: Calculated load lines, for HCBT 1 (uniform *n*-collector, dashed line), HCBT 2 (CMOS *n*-well, dash-dot line), and HCBT 3 (low-doped *n*-collector, solid line), for the input powers of 4 dBm, 7 dBm, and 3 dBm, respectively. For each transistor, $\Gamma_S = \Gamma_{Sopt}$, $\Gamma_L = \Gamma_{Lopt}$, and $f_0 = 2.4$ GHz. The bias points are: HCBT 1 (55 mA, 3 V), HCBT 2 (77 mA, 2.5 V), and HCBT 3 (44 mA, 4.5 V).

the transistors experience different effects which limit the load line trajectory, and the effects are the result of the different collector doping profiles. Due to the differences in the three devices, different performance is achieved which enables the optimization of the power amplifier performance on the device level. Namely, employing an HCBT with low-doped *n*-collector , it is straightforward to achieve high output power and gain, whereas by employing HCBT with CMOS *n*-well, a high linearity can be achieved with high collector efficiency. Additionally, an HCBT with uniform *n*-collector provides the compromise between the two, providing the best overall solution in applications where the output power, gain, collector efficiency, and linearity, are equally important.

Chapter 3

Linear operating area of horizontal current bipolar transistor

The performance of a power amplifier is directly influenced by the performance of the transistor used. To maximize the performance of a transistor in large-signal operation, it is advantageous to have access to the time-domain waveforms at the terminals of the transistor. Such an information enables one to optimize the load line in order to achieve better exploitation of the transistor's capabilities for power amplifiers. Since the output of the transistor defines the load line in large-signal operation, a measurement setup and methodology for a time-domain waveform measurement at the collector reference plane are developed and utilized to define the area of linear large-signal operation for the horizontal current bipolar transistor.

3.1 Linear operating area of a bipolar transistor

The advent of large-signal measurement setups, with the ability to measure voltage and current time-domain waveforms at the transistor reference planes [87, 88, 89, 90, 91, 92], enabled both device technology [93] and circuit [94] optimization. Likewise, such a setup can be employed to determine the maximum voltage and current amplitudes at the input and output of the transistor [95, 96], which is an important information for both device reliability and PA design. While the maximum swing is usually related to the absolute maximum ratings of the transistor, it has been shown that bipolar transistors can operate reliably well above their maximum ratings [97, 98]. On the other hand, finding the linear operating area relevant for Class-A PA and many other RF transceiver circuits cannot be achieved from maximum voltage and current ratings nor from DC characteristics.

Bipolar transistor linearity depends on multiple effects that can distort the RF waveforms and cause a gain decrease, e.g., saturation voltage, Kirk effect, self-heating, or impact ionization [99, 100], which are not directly visible from the DC $I-V$ plots. In some cases, these

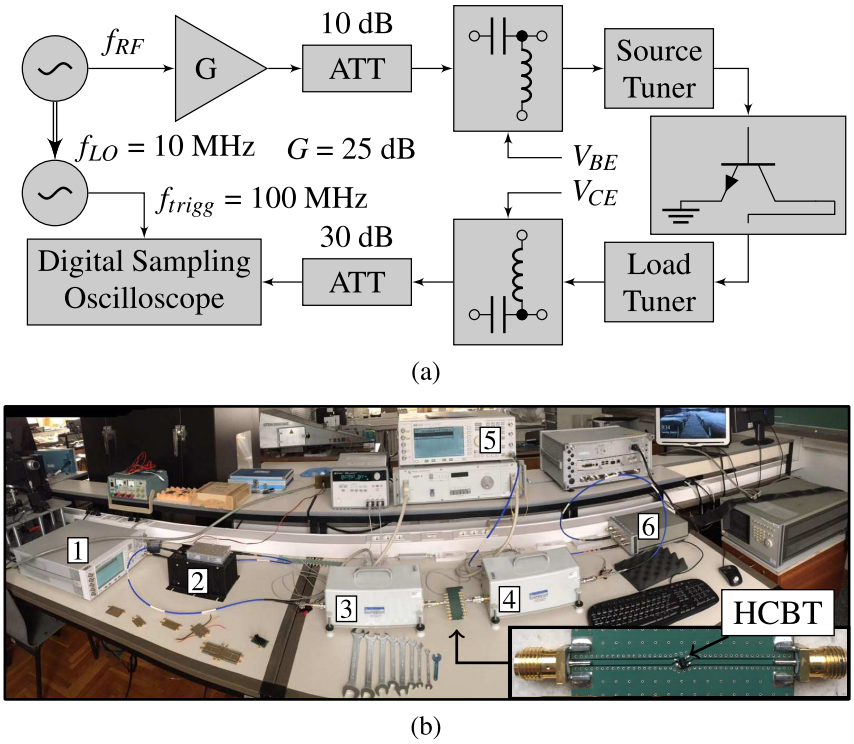


Figure 3.1: (a) Block diagram and (b) photograph of the measurement setup. The setup consists of: signal generator (1), which sets the input power level, preamplifier (2), automated source (3) and load (4) mechanical tuners based on a slab line and a slug, triggering signal generator (5), and digital sampling oscilloscope (6). The inset in (b) shows the test fixture fabricated on a 1-mm-thick FR4 substrate, where a coaxial to coplanar waveguide transitions are also shown.

effects can be analytically calculated and taken as the RF swing limit [100] or inferred from the DC bias point shift [101]. Nevertheless, neither approach gives a direct observation of the voltage and current limits relevant to the maximum swing in linear operation.

Since the nonlinear effects in bipolar transistors are hard to analytically account for, the impact of such effects is best investigated by dedicated measurement setup which enables the measurement of time-domain waveforms at transistor's terminals. The time-domain information encompasses the influence of all nonlinear phenomena in bipolar transistors which impacts the large-signal operation, i.e., output power, gain, collector efficiency, bias current and voltages, and linearity.

3.1.1 Measurement setup

The block diagram and a photograph of the measurement setup which enables time-domain waveform measurement at the collector terminal is shown in Fig. 3.1. The setup comprises two signal generators; the top one provides the input RF signal, whereas the bottom one outputs the trigger signal for the digital sampling oscilloscope (DSO - HP54120) [102]. The oscilloscope is the component of the setup which enables the measurements of the voltage time-domain waveform at the collector terminal of a DUT. This oscilloscope employs the principle of sub-

sampling to capture radiofrequency voltage waveforms. The only requirement is that the signals being measured are periodic in time, i.e., are repeatable. This requirement stems from the sub-sampling principle; the waveform is not constructed during one period of the signal, as is the case for real-time measurements, but the complete signal is constructed over multiple periods. Usually, each period, one sample of the signal is taken, which enables the oscilloscope to operate effectively with much lower sampling frequency than of the signal being measured. The signal generators share the same local oscillator (LO) reference of 10 MHz, for the synchronization. Additionally, the trigger signal is provided for the oscilloscope which is synchronized to the top signal generator providing the input signal. Such configuration ensures the correct trigger signal which is shifted by a fraction of the input signal's period with each full period. Thus, the triggering generator must be synchronized with the input signal or some samples of the waveform may be skipped and the waveform would not be fully constructed regardless of the measurement period. The trigger signal is set to 100 MHz, which is a divisor of the fundamental frequencies at which the measurements are performed in the subsequent analysis.

The input signal is provided by E4433B ESG-D signal generator [103], which exhibits maximum controllable output power of 14 dBm. To enable higher input powers for the analyzed transistors, at the output of the top signal generator a preamplifier is added. The preamplifier provides the gain of 25 dB for all frequencies of interest. Although such a gain would result in the maximum input power of 14 dBm + 25 dB = 39 dBm, which is too high for the analyzed transistors, the output of the preamplifier now can be followed by the 10 dB attenuator. The attenuator lowers the maximum output power of the preamplifier to a value of 29 dBm, which is still more than enough for the analyzed transistors, but enables the increase of the output return loss of the preamplifier. This return loss should be as high as possible since the output of the preamplifier is a termination for the source tuner and, thus, impacts the accuracy of the source impedance synthesized by the tuning block of the source side. The preamplifier is ZHL-5W-422+ component from Mini-circuits [104], which has a fairly low output return loss of around 3.5 dB at 2.4 GHz, i.e., the output impedance is far from 50 Ω. By using the 10-dB attenuator, the output return loss is increased to

$$\mathrm{RL}_{\mathrm{preamp}} = 3.5 + 20 = 23.5 \text{ dB}, \tag{3.1}$$

where the 20-dB increase is due to the signal passing the attenuator twice. This value provides much closer output impedance to 50 Ω and does not incur a large mistake due to the approximation of the preamplifier's impedance being equal to 50 Ω. Similarly, a 30-dB attenuator is added to the input of the oscilloscope to increase its input return loss. Such a high attenuation also serves to stay below the maximum power rating of the oscilloscope's input, which is 0 dBm.

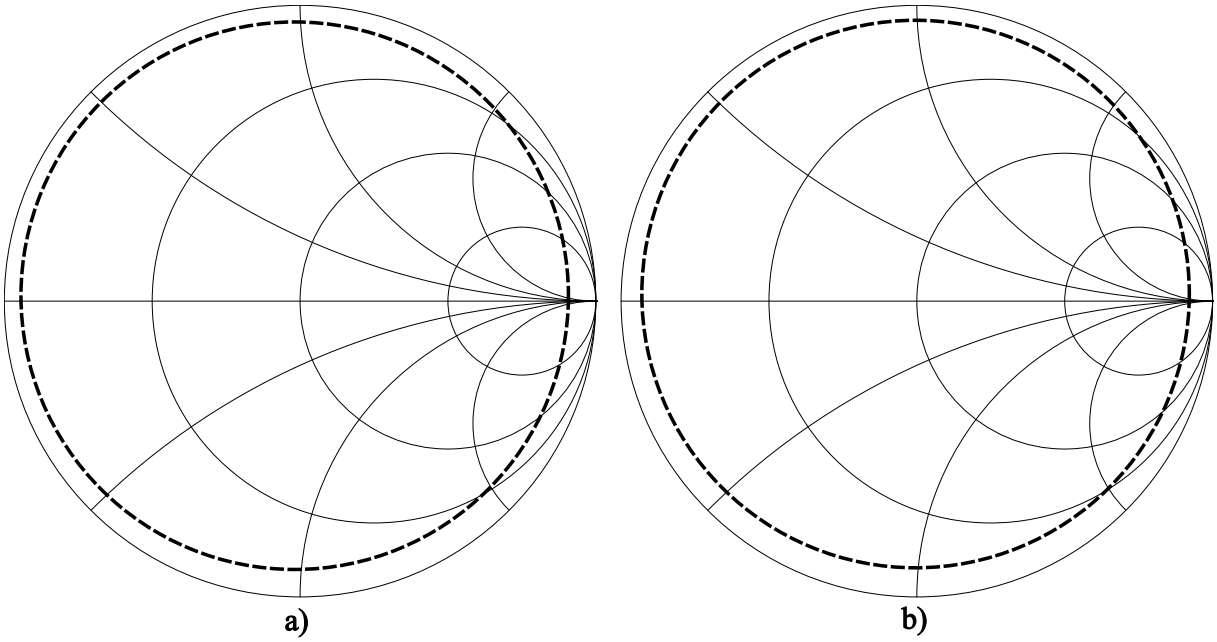


Figure 3.2: Tuning range at the fundamental frequency of (a) 1.8 GHz and (b) 2.4 GHz of the source and load tuners. The impedance (reflection coefficient) tuning range at $f_0 = 1.8$ GHz/2.4 GHz is $|\Gamma| < 0.88/0.87$.

Tuning range

The source and load tuners enable impedance synthesis at the terminals of the DUT. The accuracy depends on the accuracy and repeatability of the tuners. Additionally, the minimum and maximum impedances which can be synthesized heavily depend on the insertion loss of the components between the DUT and the tuners. In this setup, those components are the source and load halves of the test fixture along with the microstrip-to-coaxial connectors which interface the fixture and the tuners. An ideal tuner enables the synthesis of a reflection coefficient at the edge of the Smith chart, i.e., $|\Gamma| = 1$, but due to the insertion loss of the test fixture, the tuning range is somewhat smaller. If $\mathbf{S}^{\mathrm{hf}}$ is the *S*-matrix of the half-fixture at 1.8 GHz, given by

$$\mathbf{S}^{\mathrm{hf}} = \begin{bmatrix} 0.047 + j0.157 & -0.338 - j0.913 \\ -0.338 - j0.913 & -0.0594 - j0.140 \end{bmatrix}, \tag{3.2}$$

then the load reflection coefficient is given by

$$\Gamma_{\mathrm{L}} = S_{11}^{\mathrm{hf}} + \frac{S_{12}^{\mathrm{hf}} S_{21}^{\mathrm{hf}} \Gamma_{\mathrm{tuner}}}{1 - S_{22}^{\mathrm{hf}} \Gamma_{\mathrm{tuner}}}, \tag{3.3}$$

where Γ_{L} and Γ_{tuner} are the synthesized load reflection coefficient and the reflection coefficient at the tuner reference plane, respectively. If, for example, a short ($\Gamma_{\mathrm{L}} = -1$) is to be synthesized at the DUT reference plane, the tuner is set to $\Gamma_{\mathrm{tuner}} = -1$, whereas the resultant load reflection coefficient at the reference plane of the DUT is

$$\Gamma_{\mathrm{L}} = 0.854 - j0.357 \Rightarrow |\Gamma_{\mathrm{L}}| = 0.93, \tag{3.4}$$

which, if the resistance is assumed, corresponds to

$$R_{\mathrm{L}} = 1.8\ \Omega, \tag{3.5}$$

where R_{L} is the resistance at the reference plane of the DUT. The tuning range of the measurement setup is, thus, shown in Fig. 3.2 for 1.8 GHz and 2.4 GHz. The Smith charts show the regions of possible impedances at the reference plane of the DUT. At 1.8 GHz, the lowest maximum reflection coefficient magnitude is 0.88, whereas at 2.4 GHz is 0.87. These values correspond to the angle of the reflection coefficient of around 270° for both frequencies. The range of impedances which are synthesizable by the setup is large enough for the analyzed transistors, which exhibit optimum impedances in the vicinity of 50 Ω.

Reference plane shift

To enable the measurement of time-domain voltage waveforms at the specific reference plane of the measurement setup, a reference plane is shifted from the oscilloscope's input to the terminals of the DUT. This shift is usually performed in the frequency domain by *S*-matrix deembedding, but the quantity measured by the setup is a time-domain voltage waveform and, therefore, a transformation to frequency domain is necessary.

The oscilloscope measures samples of the voltage v_{osc} at its input in M samples, which can be transformed to the frequency domain by employing discrete Fourier Transform:

$$V_{\mathrm{osc}}^{(n)} = \frac{1}{M} \sum_{m=0}^{M-1} v_{\mathrm{osc}} \left(\frac{mT}{M} \right) \exp \left(-\frac{j2\pi nm}{M} \right), \tag{3.6}$$

where $V_{\mathrm{osc}}^{(n)}$ is a Fourier series of the measured voltage v_{osc}. The n defines the harmonic number and T the sampling period, according to

$$n = 1, 2, 3, \tag{3.7}$$

$$T = \frac{2\pi}{\omega}. \tag{3.8}$$

As shown in (3.7), the setup captures the fundamental frequency, second, and third harmonic of the measured voltage waveform. The second and third harmonic accurately describe the nonlinearity of the transistor for the most popular classes of operation, such as Class-A/AB/B.

Thus, only these two harmonics are taken into account in the subsequent measurements.

The reference plane shift is made according to [88], where the measured voltage $V_{\mathrm{osc}}^{(n)}$ is first transformed to the travelling wave $b_{\mathrm{osc}}^{(n)}$ as

$$b_{\mathrm{osc}}^{(n)} = \frac{V_{\mathrm{osc}}^{(n)}}{\sqrt{2Z_0}}. \tag{3.9}$$

where Z_0 is a system impedance of 50 Ω. Then, the reference plane is shifted to the output terminal of the DUT, i.e., the collector of the HCBT, by calculating the incident and reflected travelling waves at the collector $a_0^{(n)}$ and $b_0^{(n)}$, for each n separately, as

$$b_0^{(n)} = \frac{b_{\mathrm{osc}}^{(n)}}{S_{21}^{\mathrm{hf}(n)}}, \tag{3.10}$$

$$a_0^{(n)} = S_{11}^{\mathrm{hf}(n)} b_0^{(n)}. \tag{3.11}$$

The voltage and current at the collector $V_0^{(n)}$ and $I_0^{(n)}$, respectively, are then calculated as

$$V_0^{(n)} = \sqrt{2Z_0}\left[a_0^{(n)} + b_0^{(n)}\right], \tag{3.12}$$

$$I_0^{(n)} = \sqrt{\frac{2}{Z_0}}\left[a_0^{(n)} - b_0^{(n)}\right]. \tag{3.13}$$

The time-domain domain waveforms of the voltage and current at the collector v_0 and i_0 are given by

$$v_0\left(\frac{mT}{M}\right) = \sum_{n=-N}^{N} V_0^n \exp\left(\frac{j2\pi nm}{M}\right), \tag{3.14}$$

$$i_0\left(\frac{mT}{M}\right) = \sum_{n=-N}^{N} I_0^n \exp\left(\frac{j2\pi nm}{M}\right), \tag{3.15}$$

where $V_0^{(-n)}$ and $I_0^{(-n)}$ are complex conjugates of $V_0^{(n)}$ and $I_0^{(n)}$, respectively.

Although the calculation shown takes into account the S-parameters of the half-fixture, the same procedure enables the deembedding of the package, if its equivalent schematic is known. The voltage and current time-domain waveforms are then obtained at the transistor die pad, thus eliminating the influence of the package.

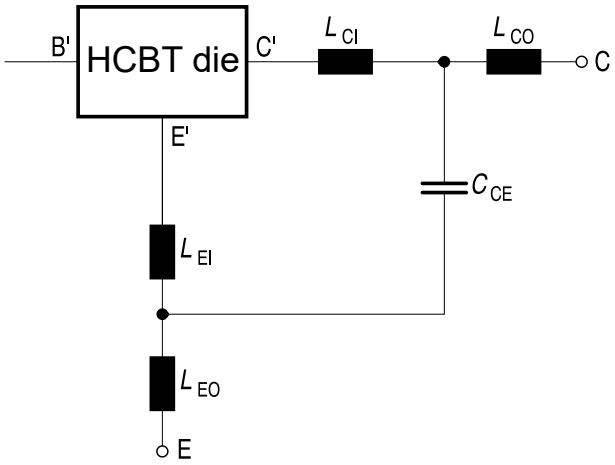


Figure 3.3: Equivalent schematic of the load side of the 4-pin SOT-343 package.

Package equivalent schematic

The load side of the package is modelled to enable the reference plane shift from the collector package pin to the collector die pad. The equivalent schematic is developed according to the information acquired from the packaging process, which enable relatively accurate estimation of the parasitic inductances and capacitances of the package. The package schematic is shown in Fig. 3.3 and the component values in Tab. 3.1.

Table 3.1: Parameters of the equivalent schematic of the package shown in Fig. 3.3.

L_{CI}	0.6 nH
L_{CO}	0.6 nH
L_{EI}	0.2 nH
L_{EO}	0.05 nH
C_{CE}	140 fF

The L_{CI} and L_{EI} are inductances of the collector and emitter bond wires, respectively, whereas the L_{CO} and L_{EO} are the inductances of the collector and emitter package pins, respectively. Since the package has two emitter leads, which are bonded to by two parallel bond wires, the inductances of the emitter as significantly smaller than the collector ones. Additionally, the C_{CE} is a capacitance between the collector and emitter package pins. The reference plane is, therefore, shifted further from $C-E$ to $C'-E'$ according to (3.6) - (3.15).

3.1.2 Measurement methodology

The linear operating range of a bipolar transistor is limited by the nonlinearities occurring due to the physics of the transistor. More precisely, the maximum collector-emitter voltage is limited by the breakdown voltage, the maximum collector current is limited by the Kirk effect. Although the collector current for which the Kirk effect occurs does not present a reliability

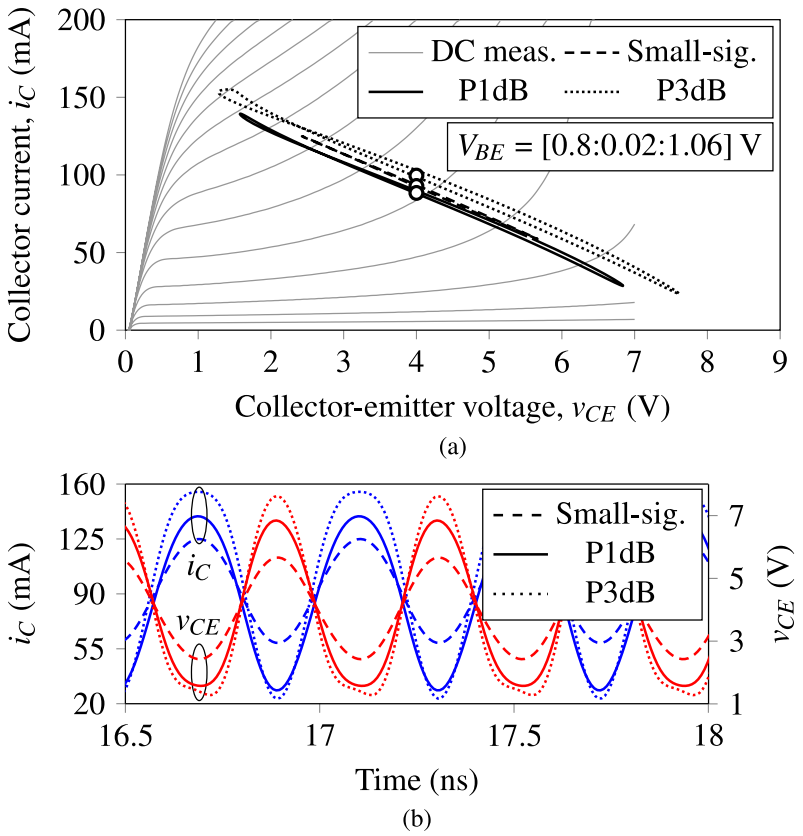


Figure 3.4: (a) Output DC $I_C - V_{CE}$ curves and measured 50-Ω dynamic load lines at the collector die pad for three input power levels: 5 dBm (small signal), 10.3 dBm (P1dB), and 14 dBm (P3dB) at 2.4 GHz. The bias points (○) differ due to self-bias caused by the waveform compression. (b) Collector current (blue) and collector–emitter voltage (red) waveforms.

concern for the transistor, it incurs a nonlinearity to the voltage and current waveforms at the collector. Therefore, the maximum collector current for the linear operation is determined for the HCBT.

To determine the boundaries of linear operation, the nonlinearities are probed by the methodology illustrated by the three example load lines, given by $i_0(v_0)$, in Fig. 3.4a, which are measured for the HCBT with $A_E = 58.5\ \mu m^2$. The figure shows three load lines measured for different input power levels, namely, 5 dBm (small-signal), 10.3 dBm (P1dB), and 14 dBm (P3dB), where the latter is measured in 3-dB compression point. The load impedance for all three load lines is the same and equal to $Z_L = 50 + j0\ \Omega$. By increasing the input power, the transistor transitions from the linear (small-signal) regime to the large-signal regime, which correspond to the P1dB and P3dB load lines. As is visible from the P1dB and P3dB load line, the distortion occurs in the high-current part of the load line, but not in the low-current part; the nonlinearity causing the distortion is the voltage swing penetrating the saturation region. Due to this distortion, the gain compression occurs, hence, the load line P1dB and P3dB are measured in compression. The bias point and load impedance are chosen such that there is no distortion in the low-current part of the load line. In this way, the cause of the gain compression is solely

due to the Kirk effect, which isolates this nonlinear phenomena and enables the mapping of the boundary of linear operation in the output DC characteristics. Although the load impedance is of zero imaginary component, the load line shown a certain imaginary component since they are not straight lines. This is due to the harmonics being terminated by arbitrary load impedances determined by the load tuner at the harmonic frequencies. Thus, the harmonics are measured but are not controlled during the impedance tuning at the fundamental frequency.

The collector current and collector-emitter voltage waveforms at the collector die pad reference plane, i_0 and v_0, respectively, are shown in Fig. 3.4b. Since the input power is increased from small-signal to P3dB, both voltage and current amplitudes are the largest in P3dB. Additionally, since the HCBT is in a common-emitter configuration, the voltage and current are shifted by π. The distortion is visible for both voltage and current waveforms; the distortion occurs only for the high-current/low-voltage half-wave. Therefore, the gain compression is the result of the load line penetrating the saturation region. Thus, by ensuring that the distortion of a load line occurs in one region of the output DC plane at the time, the regions of nonlinear phenomena and the linear operating range can be identified for the HCBT, for the same level of nonlinearity, e.g., 1-dB gain compression.

3.1.3 Linear operating area and maximum output power

Analyzed HCBT

The analyzed device is an HCBT with an emitter area of $A_{\mathrm{E}} = 58.5\ \mu\mathrm{m}^2$ packaged in a four-pin SOT-343 package with the two emitter leads grounded in a common-emitter configuration, as shown in Fig. 3.1b. The peak f_{T} of 18 GHz occurs at the collector current of 25 mA at $V_{\mathrm{CE}} = 2\ V$. Furthermore, the transistor has a low-doped collector [77, 85], which provides higher breakdown voltages of $\mathrm{BV_{CEO}} = 4.8\ V$ and $\mathrm{BV_{CBO}} = 9\ V$, enabling operation up to higher voltages than the HCBT with an uniform *n*-collector.

Measurement results

The boundary of linear operating range is determined for the HCBT and shown in Fig. 3.5a, at the fundamental frequency of 1.8 GHz and 2.4 GHz. The bias points and load resistances are chosen such that the clipping, termed hard-limitation, occurs only in the high-current half-wave. Four bias points with the load resistance in the range from 5 Ω to 150 Ω cover the entire boundary of compression enclosing the linear operating region. For each load line, the input power is increased and the P1dB is found. The collector current and collector-emitter voltage are then captured and the load line is drawn. Therefore, the boundary of compression is the result of the load lines exhibiting hard-limitation to a level of P1dB gain compression. Although the hard-limitation is a result of different physical phenomena in the HCBT depending on the

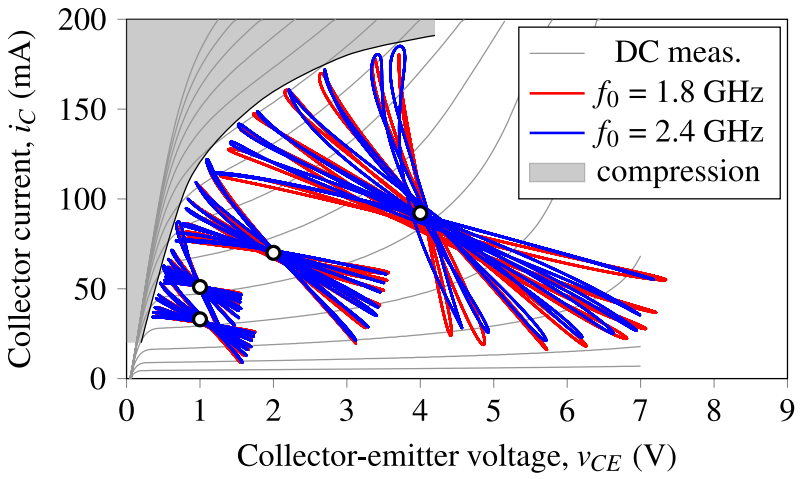


Figure 3.5: Measured load lines in P1dB for the load resistances in the range from 5 Ω to 150 Ω at the fundamental frequency f_0 of 1.8 GHz and 2.4 GHz. Bias points (○) represent average DC collector current since the current slightly differs among the load lines due to self-bias. Compression occurs in the shaded area.

collector current value, it is nevertheless a continuous boundary which comprises the two main effects of hard-limitation; the saturation region and the Kirk effect. The hard-limitation due to the penetration into the saturation region occurs for the collector current values of up to 100 mA, whereas for higher currents the Kirk effect becomes dominant causing, in effect, an increase of the knee voltage relevant for the power amplifier design. For collector-emitter voltages of higher than 4 V, the boundary saturates to the value of around 190 mA. Therefore, the maximum collector current for the linear operation of HCBT is determined by the Kirk effect, and not by the maximum current rating relevant for the reliability of the device. Between the saturation region and the Kirk effect, there is a continuous transition region which is due to the increasing impact of the Kirk effect. The shown boundary, therefore, defines the value of the knee voltage for power amplifier design, and presents a degree of freedom for the circuit designer; for high-currents the knee voltage increases rapidly due to the Kirk effect. The boundary approximates to a straight line for currents lower than 100 mA where the impact of saturation region is dominant, but deviates significantly from the DC output characteristics for higher current. Interestingly, the effects described are not visible from the DC output characteristics. The measured linear operating range is relevant since the power amplifiers are readily designed with the P1dB being the maximum output power, regardless of the input signal applied; for higher output powers, the PA is overly nonlinear and difficult to linearize employing the most sophisticated linearization techniques.

If now the maximum collector-emitter voltage swing is set to 9 V, the measured boundary of compression enables the determination of the load line for maximum output power. A simplified analysis is shown in Fig. 3.6, wherein the load lines are drawn for different load resistances and the output power with the corresponding collector efficiency is calculated for

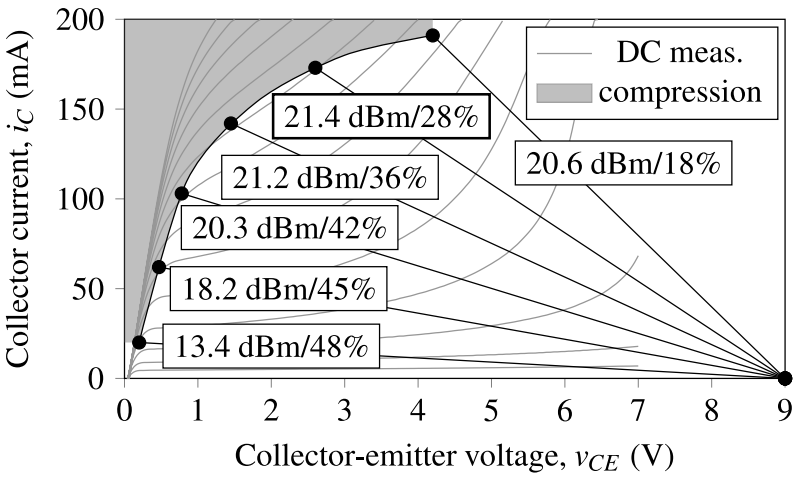


Figure 3.6: Analytical load lines with calculated output power and collector efficiency in P1dB for various load resistances with the knee voltage set by the boundary shown in Fig. 3.5. Compression occurs in the shaded area.

each. Increasing the maximum collector current, the knee voltage increases according to the boundary of compression and, thus, the output power is influenced by two contradicting effects; the increase of the collector current swing and the increase of the knee voltage, with the former increasing, and the latter decreasing the output power. The result of this is the existence of the bias point and load impedance combination for which the HCBT achieves the maximum output power in P1dB. Further increase in bias point results in lower output power regardless of the load impedance. For the analyzed HCBT, the maximum output power would be 21.4 dBm if the load resistance is assumed. The simplified analysis assumes that the entire voltage and current swing can be covered by the pure-resistance load lines, but, due to the measurements being performed at collector die pad reference plane, the optimal load impedance is an impedance with a non-zero imaginary part. Nevertheless, the conclusions about the maximum output power are still valid if the load impedances are set to the optimal values. Along with the output power values for each load line, the collector efficiency is also calculated, which exhibits a decrease with the increasing maximum collector current. This is expected, since the collector efficiency is influenced by two effects which both decrease the efficiency; the increase of the knee voltage and increase of the bias current and voltage. The HCBT in maximum output power bias point achieves 28% collector efficiency, whereas 0.2 dB lower output power achieves significantly higher efficiency of 36%. The latter option is surely a more probable point of operation for the transistor, but the applications in which a transistor area is to be maximally utilized and the efficiency is not a critical parameter, might exploit the maximum output power bias point.

The optimal load impedances are shown in Fig. 3.7 for different bias points in 1-dB compression point. The maximum collector-emitter voltage is set to 9 V, which is the BV_{CBO} breakdown voltage. The real part of the load impedance is varied to set the slope of the load line, whereas the imaginary part is varied to achieve the maximum output power. In other words, the

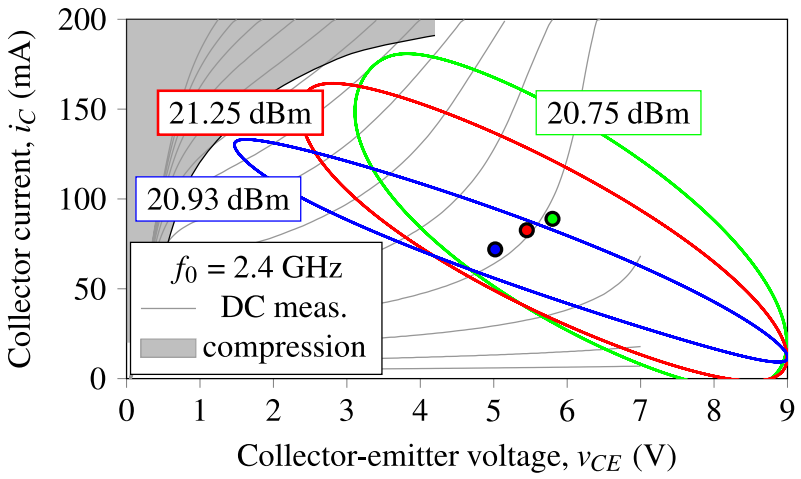


Figure 3.7: Measured load lines for maximum output power in 1-dB compression point for three bias points and load impedances at $f_0 = 2.4$ GHz. Bias points and load impedances are (5.8 V, 88 mA), (5.45 V, 83 mA), and (5 V, 72 mA) and $25 + j20\ \Omega$, $35 + j20\ \Omega$, and $60 + j20\ \Omega$, respectively.

imaginary part of the impedance is a non-zero value since the parasitics of the transistor need to be cancelled by this reactance. Regardless, the load lines exhibit the increase in the knee voltage defined by the measured boundary from Fig. 3.5, thus confirming the simplified analysis presented in Fig. 3.6. Interestingly, the reactance of the optimal impedance is equal to 20 Ω for all three bias points, suggesting that the nonlinear parasitics of the HCBT do not change in the bias points near the one for maximum output power. This further confirms that the HCBT operates reliably and predictably even though the bias point is already in the breakdown region of the output DC characteristics. The HCBT achieves the maximum output power of 21.25 dBm and collector efficiency of 30%, for the bias point (5.45 V, 83 mA) and maximum collector-emitter voltage of 9 V. Further increase in bias decreases the output power and collector efficiency to 20.75 dBm and 23%, respectively, due to the dominating impact of the increased knee voltage. The lowest bias point results in the highest collector efficiency of 34% but with a somewhat lower output power of 20.93 dBm.

Therefore, given a boundary of compression which encloses the area of linear operation of a bipolar transistor, an optimal load line for maximum output power can be found. The optimal load line results in the maximum output power in 1-dB compression point whereas further increase in bias decreases the output power. The boundary, therefore, also defines the maximum collector current swing for the linear operation of the transistor, which is lower than the maximum collector current rating of the transistor relevant for the reliability of the device. For the applications in which a given transistor die area should be exploited for the maximum output power, the boundary of compression enables the determination of the optimal bias and load impedance combination. The analyzed HCBT operates reliably in the bias point of maximum output power, providing constant bias collector current and output power over time.

3.2 Impact of load line hard-limitation on bias point

In the context of a circuit design, a bipolar transistor differs with respect to metal-oxide-semiconductor (MOS) devices in the base DC current value. Namely, the bipolar transistor requires a non-zero base DC current I_B in order to set a non-zero collector DC current I_C, where the two are related by

$$\beta = \frac{I_C}{I_B}, \tag{3.16}$$

where β is a DC current gain in a common-emitter configuration. Once set, the bias current values do not change their values during the small-signal operation; if no waveform distortion is present, the bias point remains constant. On the other hand, when load line hard-limitation occurs, the bias point may change significantly with respect to the point defined in the small-signal input power range.

Even the ubiquitous linear classes AB and B experience such a bias point shift when operated in the large-signal regime, i.e., in the gain compression power range. Since the hard-limitation is a function of the input power, which is a function of the nature of the input signal, the bias point change is a strong function of the modulation of the input signal. This bias point shift is readily accounted for during the circuit design phases, since the input signal is known beforehand. But, if the maximum output power needs to be achieved for the bipolar transistor at hand, and the operation near the boundary of compression is expected, the bias point behaviour is hard to predict without measuring the load lines in the large-signal operation. This is because the effects of the Kirk effect in the high-current regime, or the impact ionization in the high-voltage regime, is difficult to account for without the extremely accurate nonlinear transistor modelling of these second-order physical effects. To that end, the impact of large-signal operation near the boundary of compression on the bias point change is investigated for the HCBT by load-pull measurements and simulations.

3.2.1 Base bias configurations

The bias point behaviour depends on the circuit configuration used to apply the bias to the bipolar transistor [105]. The most common way to bias the collector-emitter circuit of the bipolar transistor operating in the power amplifier, is by a voltage source. On the other hand, the base-emitter circuit offers flexibility in the biasing configuration; a bias can be set by a voltage or current source. The difference between the two is the resistance seen by the base looking toward the source at DC.

The bias configuration for a bipolar transistor operating in the common-emitter configuration is shown in Fig. 3.8. The common-emitter configuration takes the input signal to the base

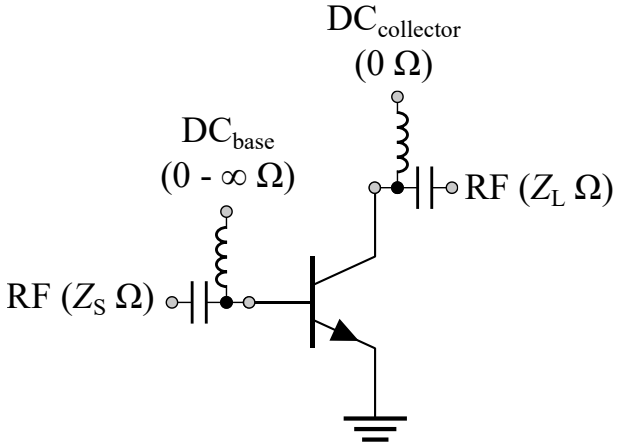


Figure 3.8: Simplified bias network of a bipolar transistor in the common-emitter configuration. The impedances seen by the transistor at RF and DC also shown.

and the output signal out of the collector electrode. The impedances seen at RF by the base and collector are determined by the matching networks, which are designed according to the optimal matching impedances acquired from load-pull and source-pull measurements. These impedances, Z_S and Z_L, are in the range from 20 Ω to 70 Ω for the HCBTs of the emitter areas suitable for the applications in handheld devices. On the other hand, the resistances seen by the base and collector at DC are determined by the nature of the bias networks employed for the bias voltage or current application. Namely, the collector-emitter is usually biased by a voltage source, whereas the base-emitter junction readily contains relatively large value resistance of around tens of kiloOhms to set the desired base-emitter voltage and current. The impact ionization in the collector-base junction at high voltages creates additional current component which can flow out of the base or emitter for 0 Ω or ∞ Ω resistance in the base bias network, respectively. This resistance, furthermore, defines the abrupt increase in collector current in the output DC characteristics. The two are the extreme cases when the transistor is biased with voltage or current source, but, usually, a bipolar transistor has a non-zero resistance in the base-emitter circuit at DC.

In other words, the base resistance in the base-emitter circuit determines the breakdown voltage, which attains a value between the open-base and open-emitter breakdown voltages, BV_{CEO} and BV_{CBO}, respectively, which is termed BV_{CER}. The matter is further complicated due to the bias point shift in large-signal operation. Namely, if the base-emitter junction is biased by a voltage source, the large-signal operation incurs a shift of the base current at DC, along with the corresponding shift of the collector current. Furthermore, the DC collector current can be changed by a large-signal operation at both the input and output. Therefore, this shift in bias point in large-signal operation, i.e. with a load line hard-limitation present, is analyzed for the HCBT with a CMOS *n*-well collector.

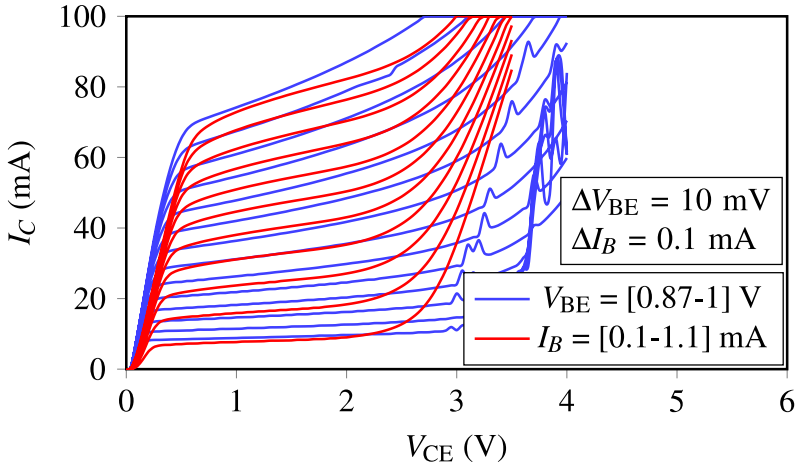


Figure 3.9: Measured output characteristics for the HCBT with CMOS n-well ($A_E = 31.2\ \mu m^2$) in c-V_{BE} and c-I_B bias configuration. The breakdown region is higher for c-V_{BE} biasing due to the 0 Ω resistance at DC in the base-emitter circuit.

Analyzed HCBT

A low-cost HCBT, with a CMOS n-well collector [106] is analyzed. Its measured common-emitter output characteristics are shown in Fig. 3.9 for both the constant base current (c-I_B) and constant base-emitter voltage (c-V_{BE}) bias configuration. The open-base breakdown voltage for this device is $BV_{CEO} = 2.9$ V, which is measured in (c-V_{BE}) configuration at the base current reversal point. Due to the difference in base-emitter circuit bias configuration, the impact ionization region in the output DC characteristics occurs for higher collector-emitter voltage for the c-V_{BE} case. Regardless, the c-V_{BE} configuration exhibits instabilities in DC measurements for voltages higher than BV_{CEO}. These instabilities are the result of the pinch-in phenomenon in bipolar transistors [85]. The presence of instabilities and the higher breakdown voltage for the c-V_{BE} configuration are measured at DC and the effect on the current and voltage at RF is unknown from DC measurements. Therefore, the impact of load line swing above the breakdown voltage is also analyzed by measuring the bias point shift.

Measurement methodology

To investigate the impact of large-signal operation on bias point, the bias point and load impedance are set such that the hard-limitation occurs in only one region of the output DC characteristics at the time. In such a way, the impact of each region separately, namely, cut-off, saturation, and impact ionization regions, can be analyzed. Three example load lines are shown in Fig. 3.10. To cause the hard-limitation of the load line in the cut-off region, the collector DC current is set low, whereas for the saturation region it is set high and the collector-emitter voltage low. The enable the collector-emitter voltage swing above the BV_{CEO}, the collector-emitter DC voltage is set just below the breakdown voltage, so that only the RF swing penetrates the impact ionization region. This eliminates the bias shift due to impact ionization at DC. Due to the hard-limitation,

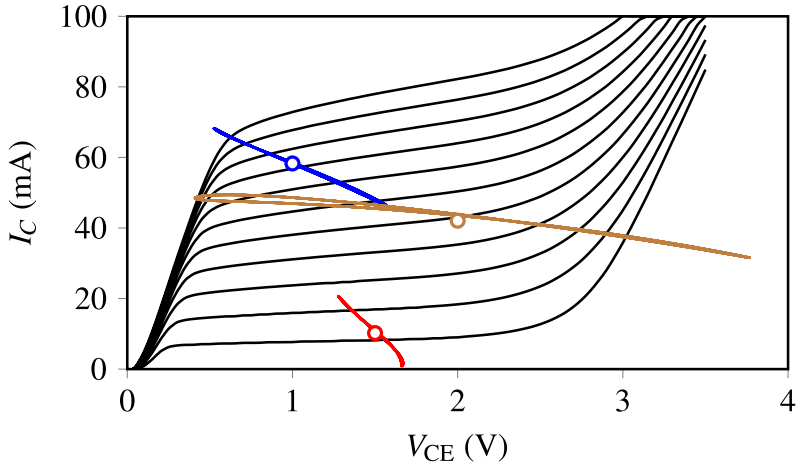


Figure 3.10: Measurement methodology to analyze the impact of large-signal operation on bias point for the HCBT, showing three example load lines exhibiting hard-limitation in different regions of the output DC characteristics: cut-off; saturation; collector-emitter voltage swing above BV_{CEO}. The output DC characteristics are shown for the c-I_B case for reference.

the distortion of the collector current and collector-emitter voltage waveforms occurs, which then modifies the DC values of the current and voltage, causing the bias shift. The input power is swept from the smalls-signal to large-signal regime and the bias currents and voltages are measured.

Hard-limitation in cut-off

The load lines in 1-dB compression point (P1dB) for c-V_{BE} and c-I_B configurations showing hard-limitation in the cut-off region are shown in Fig. 3.11a along with the output characteristics from Fig. 3.9. To ensure that the hard-limitation occurs in the cut-off and not in the saturation, the load impedance is set to 20 Ω, whereas the source impedance is set to 50 Ω. For the c-V_{BE} bias, the DC collector current I_{CQ} increases with the input power from the small-signal value of 13 mA to 51 mA in P1dB [see Fig. 3.11c], which is the result of the nonlinearity on the input side. More precisely, due to the hard-limitation at the input, DC base current I_{BQ} increases [see Fig. 3.11d]. The confirmation is also visible from Fig. 3.11c where the transducer gain G_T is still flat in the power range of I_{CQ} increase ($-10 < P_{IN} < 5$ dBm). Therefore, in this power range, there is no gain compression due to hard-limitation at the output. On the other hand, even though the hard-limitation in the cut-off for c-I_B biasing is evident from Fig. 3.11b, I_{CQ} is relatively constant and even decreases slightly by 0.5 mA in compression. For c-I_B, the hard-limitation at the output tends to increase the I_{CQ} whereas the reducing V_{BEQ} tends to decrease it, maintaining I_{CQ} constant [see Fig. 3.11c,d]. The V_{BEQ} decreases from 0.874 V to 0.85 V in P1dB, whereas for even higher P_{IN}, decreases and for $P_{IN} = 9$ dBm reverses the polarity. For the chosen bias point, the behaviour forces the c-I_B configuration to compress for approximately 13 dB lower input power than the c-V_{BE} bias, which provides much larger linear operating range

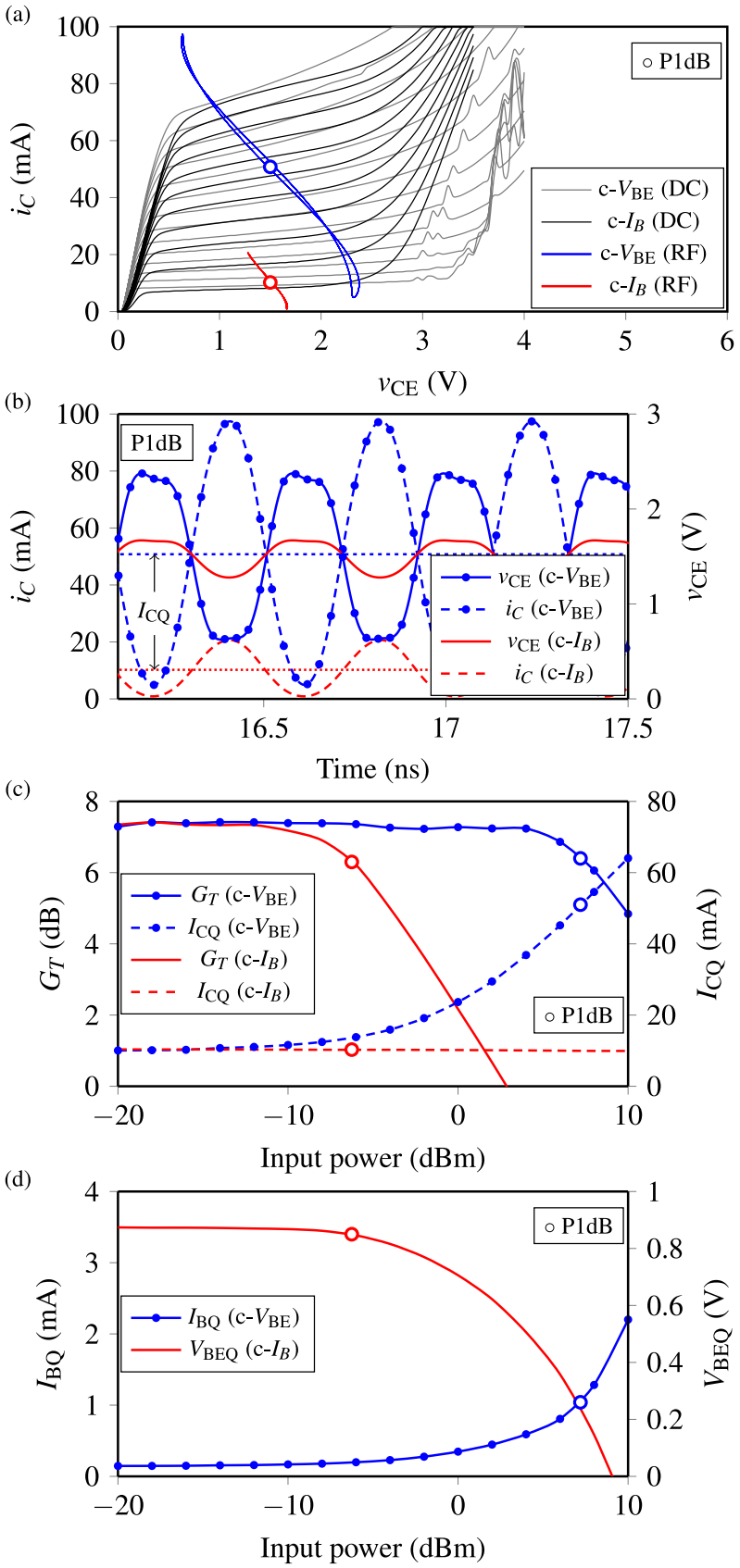


Figure 3.11: Measured (a) load lines in P1dB, (b) v_{CE} and i_C waveforms, (c) transducer gain G_T and DC collector current I_{CQ}, and (d) DC base current I_{BQ} and DC base-emitter voltage V_{BEQ}, in c-V_{BE} and c-I_B bias configuration for the hard-limitation in the cut-off. The load impedance is $Z_L = 20\ \Omega$. The DC points are set to result in the same initial $I_{CQ} = 13$ mA.

in c-V_{BE} configuration, although, the range can be improved by increasing the initial I_{BQ}. This larger operating range is, nevertheless, useful if the bias network is properly designed so as to support this I_{CQ} change with a modulated signals of a few-100 MHz frequency.

Hard-limitation in saturation

To investigate the same characteristics but with the hard-limitation occurring in the saturation region, the I_{CQ} in the small-signal range is increased to 58 mA and the load impedance is set to 50 Ω. The results are shown in Fig. 3.12 and they suggest an opposite behaviour with respect to hard-limitation in the cut-off, namely, the small-signal power range is now 1 dB larger for c-I_B bias configuration. Due to the decrease of I_{CQ} from the small-signal value of 58 mA to 51 mA in P1dB, the c-I_B load lines are effectively mitigating the saturation region thus enabling higher linear operating power range [see Fig. 3.12a], which is analogous behaviour to the c-I_B load line shown in Fig. 3.11a. The I_{CQ} is nearly constant for c-V_{BE} bias since the I_{BQ} increase at the input and I_{CQ} decrease due to the hard-limitation at the output tend to compensate each other. The nearly constant I_{CQ} for the c-V_{BE} bias, on the other hand, facilitates the hard-limitation in saturation region and, thus, the gain compression. Again, the same behaviour the c-I_B bias shows in Fig. 3.11. Additionally, for the c-I_B bias and for $P_{IN} = 5$ dBm, I_{CQ} changes the slope of decrease since the load line enters the cut-off region as well and the hard limitation occurs both in the cut-off and saturation. To confirm this, a load line in 3-dB compression point (P3dB) is shown in Fig. 3.12a, which shows that the I_{CQ} decrease shifted the load line near the cut-off region, facilitating the hard-limitation in the cut-off too. Although the bias point used for this analysis is not interesting from the point of PA design, the ultimate linear operating range is determined by the interplay of the nonlinearities arising from hard-limitation in the cut-off and saturation.

Operation above breakdown voltage

Large-signal operation where the voltage swings above the breakdown voltage BV_{CEO} is also of great importance for PAs, since the bipolars are readily employed above the breakdown voltage ratings. To that end, the same bias configurations, c-I_B and c-V_{BE}, are compared for the case where voltage v_{CE} swings approximately 1 V above BV_{CEO} [Fig. 3.13a], wherein the bias current I_{CQ} is set to 39 mA and the load impedance to 200 Ω. The operation with c-V_{BE} bias is similar to the operation with hard-limitation in the cut-off [see Fig. 3.11]. Interesting behaviour is measured for c-I_B bias, where the I_{CQ} has a large peak in P1dB at 53 mA and a subsequent sharp drop to about 30 mA, after which a slower decrease is observed [see Fig. 3.13c]. The decrease is a consequence of the limitation at the saturation, as shown in Fig. 3.12, whereas the increase is attributed to the avalanche taking place due to RF swing above BV_{CEO}. Similar behaviour is already reported in SiGe HBTs [107]. Additionally, around P1dB, c-V_{BE} and c-I_B

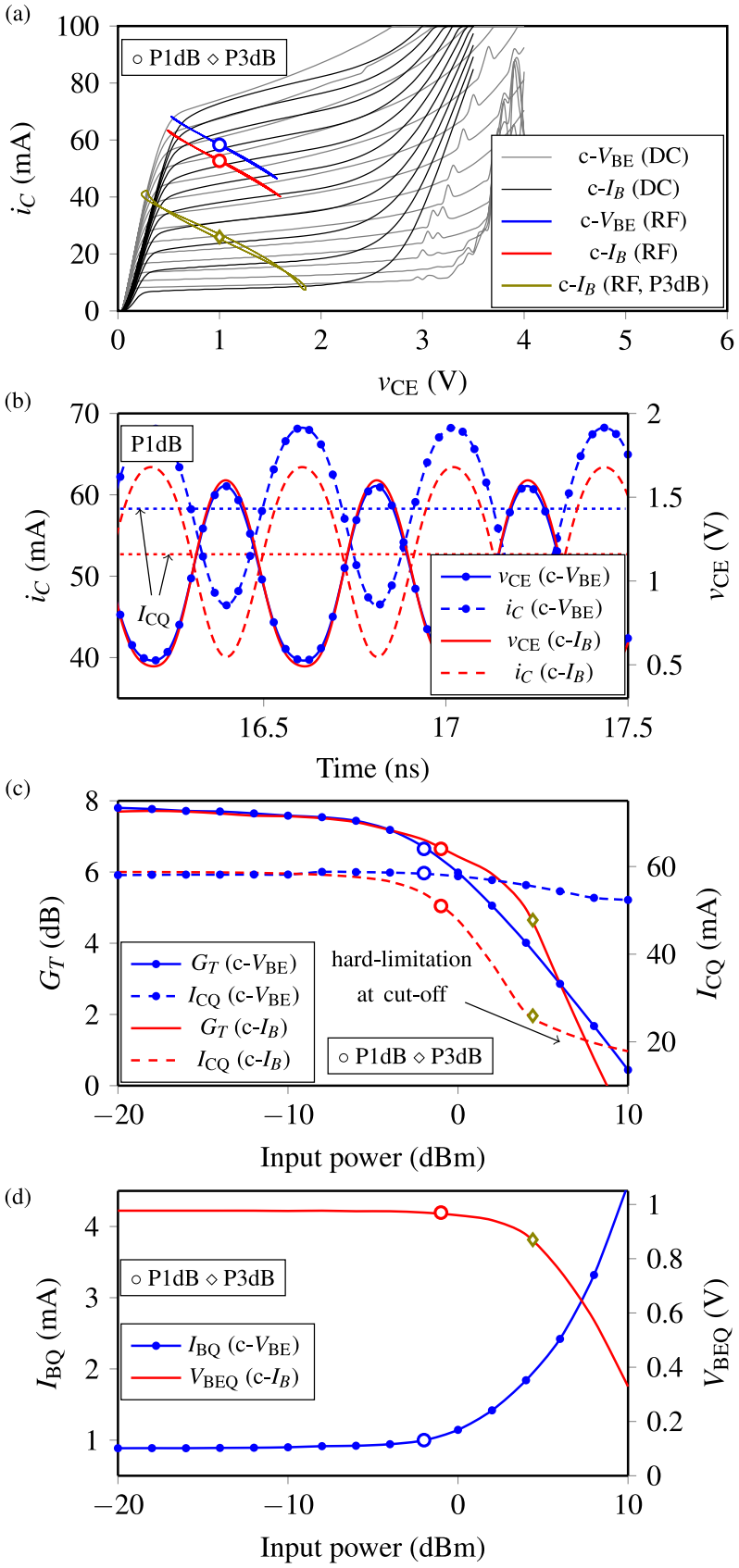


Figure 3.12: Measured (a) load lines in P1dB, (b) v_{CE} and i_C waveforms, (c) transducer gain G_T and DC collector current I_{CQ}, and (d) DC base current I_{BQ} and DC base-emitter voltage V_{BEQ}, in c-V_{BE} and c-I_B bias configuration for the hard-limitation in the saturation. The load line in 3-dB compression point (P3dB) is added for c-I_B biasing to illustrate the hard-limitation in both the saturation and cut-off. The load impedance is $Z_L = 50\ \Omega$.

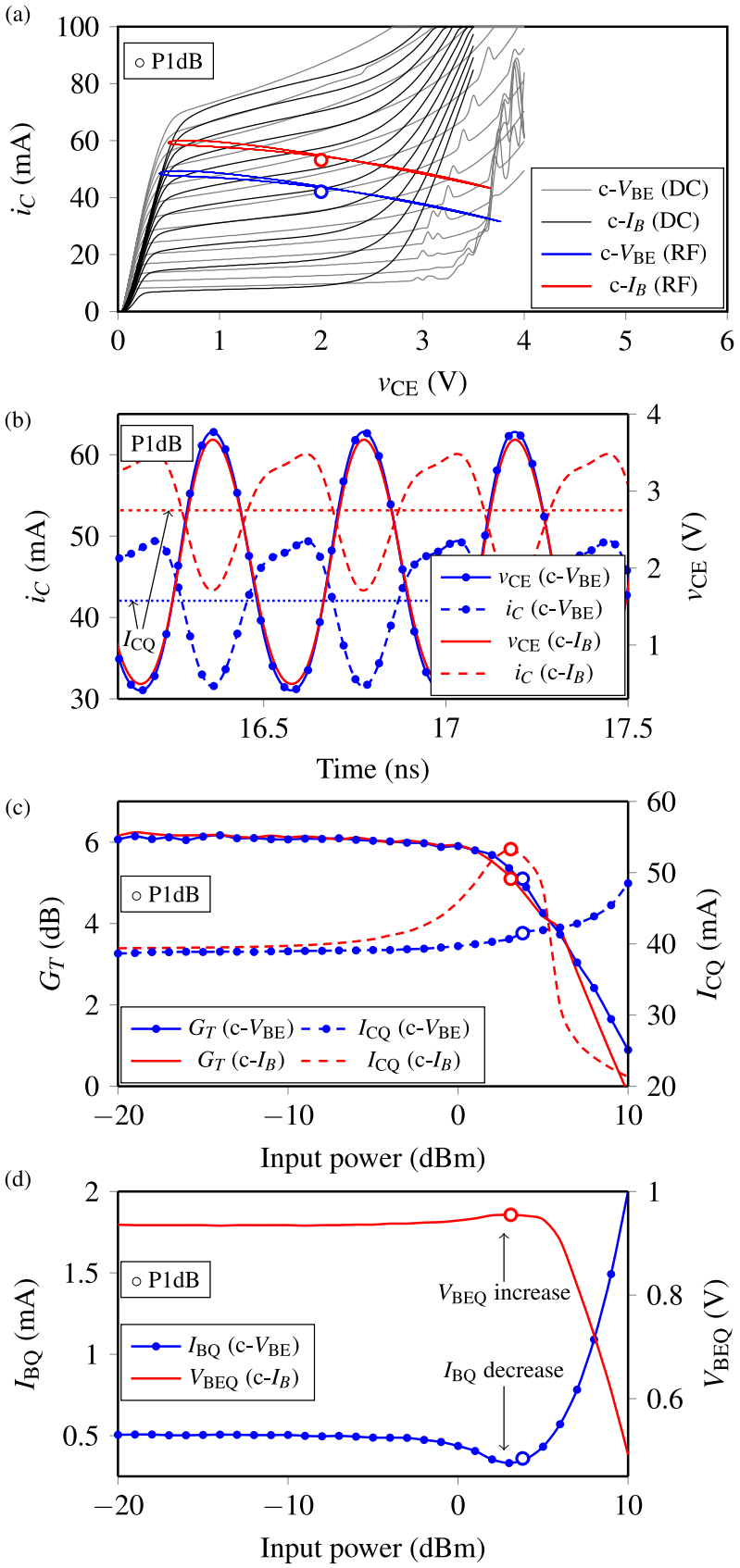


Figure 3.13: Measured (a) load lines in P1dB, (b) v_{CE} and i_C waveforms, (c) transducer gain G_T and DC collector current I_{CQ}, and (d) DC base current I_{BQ} and DC base-emitter voltage V_{BEQ}, in c-V_{BE} and c-I_B bias configuration for operation above BV_{CEO}. The load impedance is $Z_L = 200\ \Omega$. The DC points are set to result in the same initial $I_{CQ} = 39$ mA.

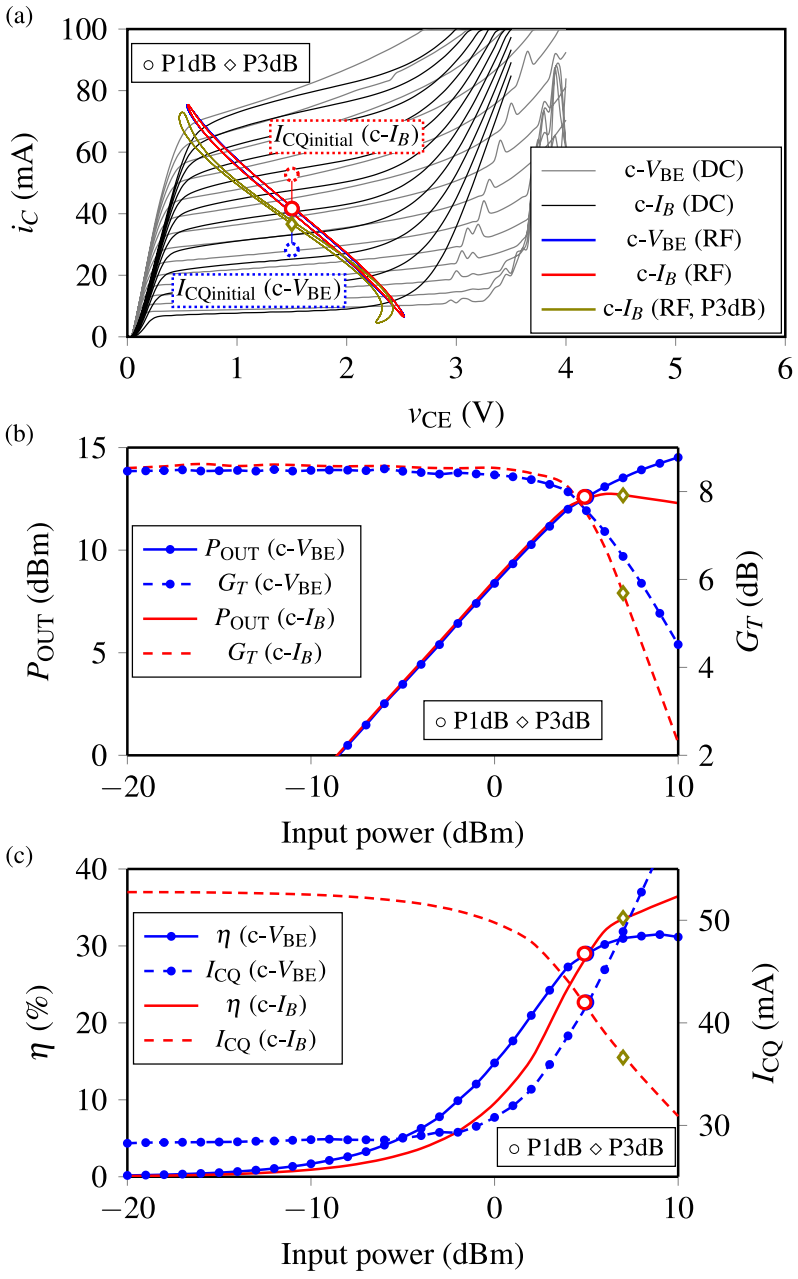


Figure 3.14: Measured (a) load lines in P1dB, (b) v_{CE} and i_C waveforms, (c) transducer gain G_T and DC collector current I_{CQ}, and (d) DC base current I_{BQ} and DC base-emitter voltage V_{BEQ}, in c-V_{BE} and c-I_B bias configuration for the same targeted output power P1dB of 12.6 dBm. The load impedance is $Z_L = 30\ \Omega$.

show an I_{BQ} decrease of 1.4 mA and V_{BEQ} increase of 20 mV, respectively. Both configurations provide similar P1dB for the chosen bias and load impedance.

Target output power

Finally, the comparison between the bias configurations is done for the same targeted output power in 1-dB compression point, which is one of the most important parameters during for power amplifier design. The V_{BEQ} and I_{BQ} in the small-signal range, for the c-V_{BE} and c-I_B, respectively, are selected such that the resulting P_{OUT} in P1dB is the same for the two configurations. Also, the conservative bias point and load impedance are selected such that the voltage swing does not approach BV_{CEO} breakdown. The Fig. 3.14a shows the two load lines for the resultant output power of $P_{OUT} = 12.6$ dBm, wherein the two configurations are configured differently due to the different behaviour of I_{CQ} in the compression, namely, for c-V_{BE} and c-I_B the I_{CQ} in the small-signal range is set to 28 mA and 53 mA, respectively [see Fig. 3.14a,c]. The I_{CQ} increase in c-V_{BE} and decrease in c-I_B configuration enables both to reach the same bias point (I_{CQ}, V_{BEQ}) = (41 mA, 1.5 V) in P1dB.

As shown in Fig. 3.14b, both configurations show the same output power and gain characteristics up to P1dB, with the c-I_B exhibiting an output power decrease and sharper gain roll-off with input power above P1dB. This is the result of hard-limitation on both ends of the load line for c-I_B configuration, as illustrated again by the load line in P3dB [see Fig. 3.14a], while the I_{CQ} increase enables the c-V_{BE} configuration to avoid the hard-limitation in the cut-off [see Fig. 3.11]. Also, the collector efficiency in P1dB is the same for both configurations [see Fig. 3.14c]. The main difference is approximately 5% higher collector efficiency for the c-V_{BE} configuration in the $0 < P_{IN} < 5$ dBm range due to the lower initial I_{CQ} and, thus, lower DC dissipation. Thus, the c-V_{BE} provides a better overall solution to target a specified output power in the operation below the BV_{CEO}.

3.2.2 Analysis by simulation

For both cases the bias point varies mainly due to the nonlinearity present in the base-emitter circuit, which then impacts the hard-limitation at the output. The cause of this shift is difficult to pinpoint without observing the time-domain waveforms at the input. To that end, the two cases of hard-limitation previously measured are additionally analysed by small-signal and large-signal simulations employing the nonlinear compact model of the HCBT.

The difficulty arises when considering the nature of the 50-Ω signal generator at the input, or, for that matter, of any other impedance visible from the base looking towards the generator, which is determined by the input matching network. The type of the generator, i.e. a voltage or current RF source, is dependent on both the matching network impedance and the

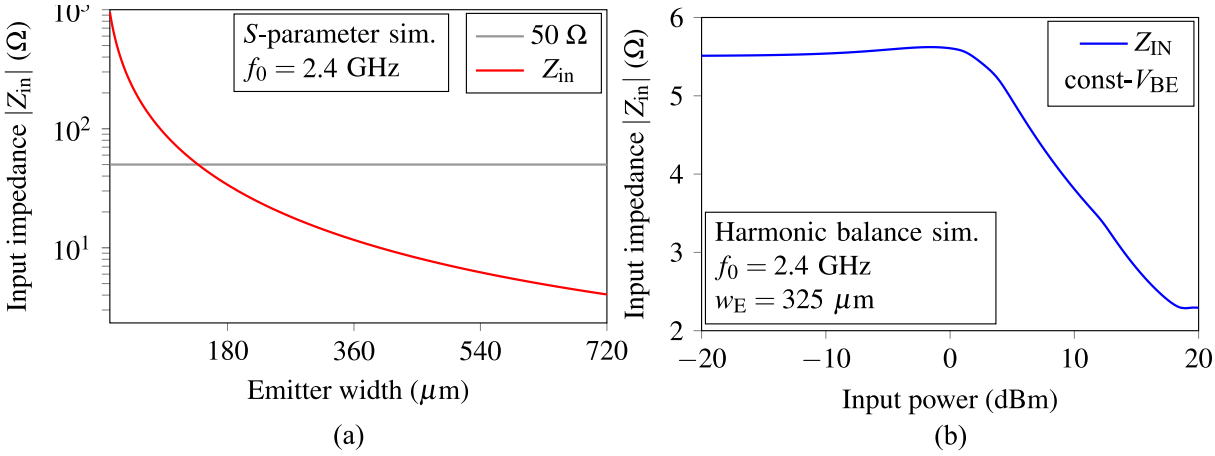


Figure 3.15: Simulated (a) small-signal input impedance as a function of the emitter width w_E and (b) large-signal input impedance as a function of input power for the HCBT of $w_E = 352$ μm, in the constant-V_{BE} configuration. The fundamental frequency f_0 is 2.4 GHz. The bias point is $(V_{BEQ}, V_{CEQ}) = (0.865\text{ V}, 1.5\text{ V})$.

input impedance of the transistor. More precisely, it is not possible to assume a voltage or current source without knowing the input impedance of the transistor at a desired fundamental frequency f_0 and input power P_{IN}. Thus, the cause of the bias point shift is difficult to identify if the impedance of the generator and the input impedance of the transistor are similar; in that case, the assumption of a pure-sine-wave base-emitter voltage or base current is invalid. This is illustrated by the subsequent *S*-parameter and harmonic balance (HB) simulations.

Firstly, the change of both small-signal and large-signal input impedance of the HCBT is simulated as a function of emitter width w_E and input power P_{IN}, respectively, as shown in Fig. 3.15. The fundamental frequency $f_0 = 2.4$ GHz and the internal impedance of the generator is assumed to be 50 Ω (unmatched transistor). The input impedance decreases with the emitter width for a given f_0, and for a specific value (150 μm) reaches 50 Ω, which is equal to the generator impedance [see Fig. 3.15a]. For large widths of around 700 μm, the input impedance drops to only few Ohms; in this case, a 50-Ω source can be regarded as a current source. The opposite holds for small emitter widths, i.e. a voltage source can be assumed. If the change of input impedance is simulated as function of input power for a given emitter width (325 μm), the Z_{in} equals the small-signal value of 5.5 Ω in the small-signal input power range and drops to around 2 Ω for $P_{in} = 20$ dBm, as shown in Fig. 3.15b. Therefore, the role of the generator depends on the input impedance of the HCBT at a given input power. This fact makes it difficult to predict to cause of the hard-limitation on the input. Regardless, for a 325-μm-wide HCBT, the input impedance is below 6 Ω in the entire input power range, thus, the generator more closely resembles a current generator, wherein the base current is a pure sine wave and the base-emitter voltage experiences the nonlinearity which causes the bias point shift.

To confirm the previous analysis, the time-domain waveforms of base current and base-emitter voltage are simulated for the two extreme cases in 1-dB compression point; $w_E =$

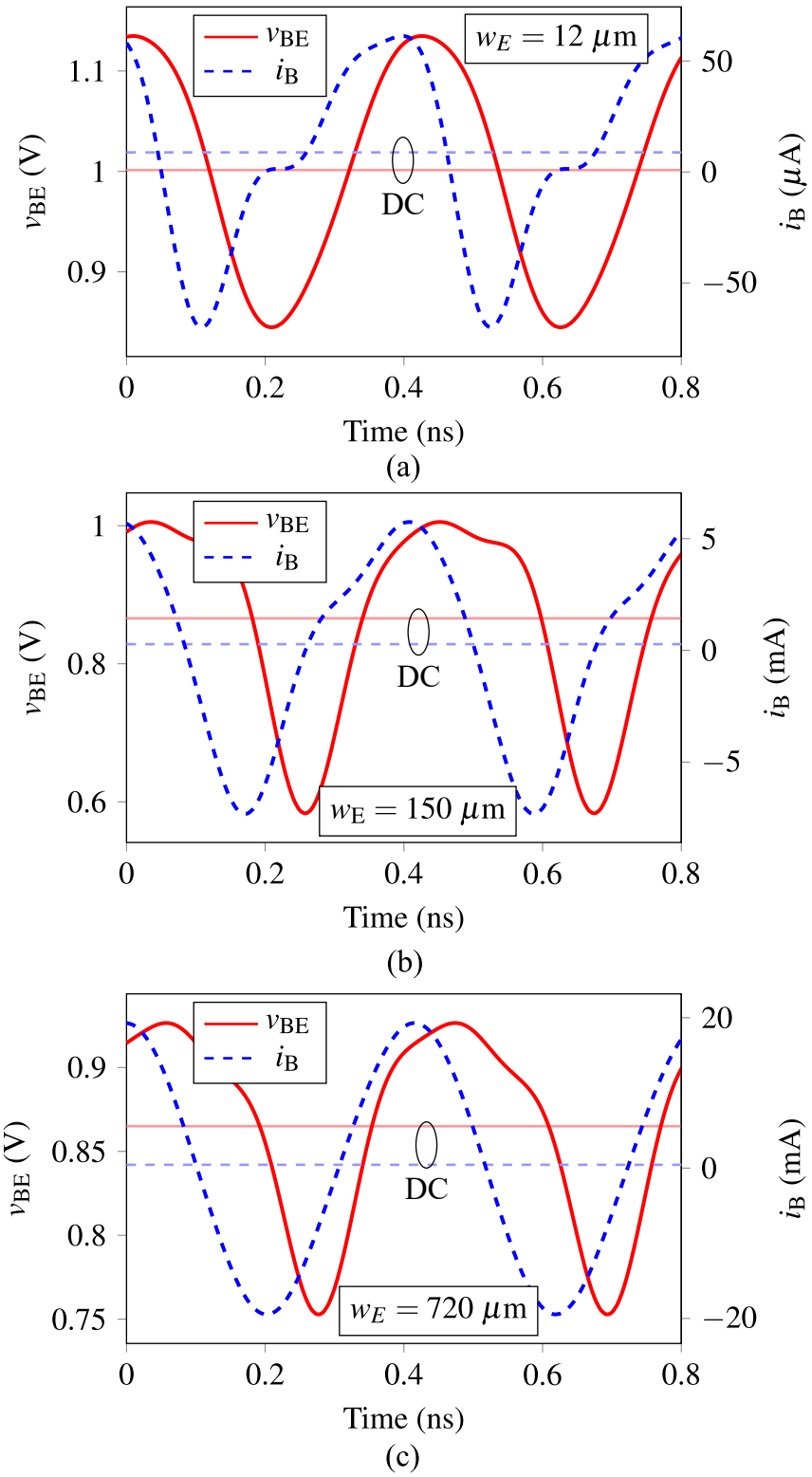


Figure 3.16: Simulated base current and base-emitter voltage time-domain waveforms for the emitter widths of (a) 12 μm, (b) 150 μm, and (c) 720 μm, for constant-V_{BE} configuration ($V_{CE} = 1.5$ V). The fundamental frequency is 2.4 GHz, and the generator internal impedance is 50 Ω.

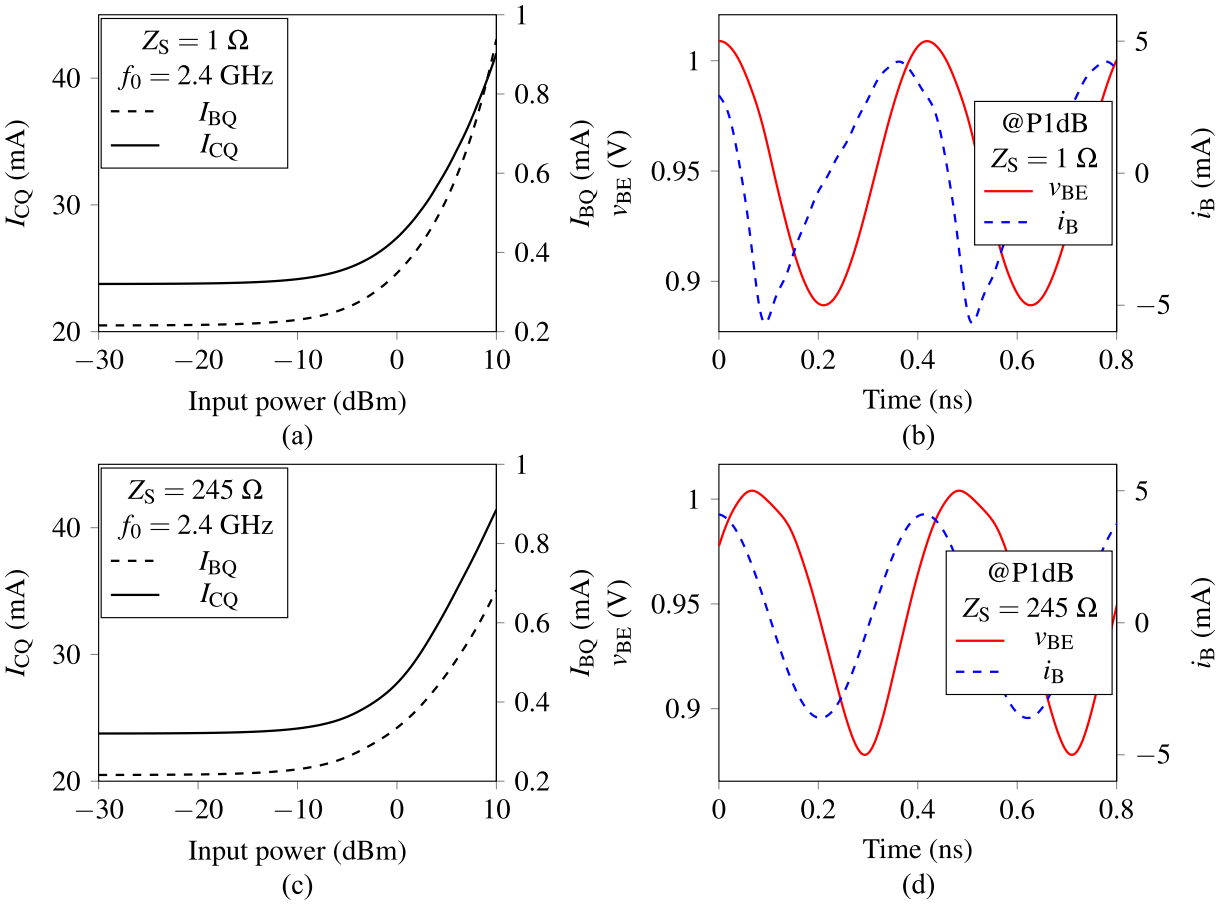


Figure 3.17: Simulated (a) DC base current I_{BQ} and collector current I_{CQ}, and (b) input time-domain waveforms v_{BE} and i_B, for $Z_S = 1\ \Omega$. Simulated (c) DC base current I_{BQ} and collector current I_{CQ}, and (d) input time-domain waveforms v_{BE} and i_B, for $Z_S = 245\ \Omega$. Load impedance is 50 Ω and the bias configuration is constant-V_{BE}.

12 μm and $w_E = 720\ \mu$m [see Fig. 3.16a,c]. Additionally, the case when the internal generator impedance is equal to the input impedance is also shown in Fig. 3.16b. Since for the $w_E = 12\ \mu$m case the generator can be regarded as a voltage source, the base-emitter voltage is a replica of the pure sine wave voltage of the generator, whereas the nonlinearity is present in the base current waveform. On the other hand, since the input impedance is lower than the internal generator impedance for the $w_E = 720\ \mu$m, the base current is a sine wave and the hard-limitation is present in the base-emitter voltage waveform. For the case when the impedances are equal ($w_E = 150\ \mu$m), there is a similar amount of distortion present in both voltage and current waveforms and it is not possible to determine which one causes a voltage and/or current bias value shift. Since the bias point shift in large-signal operation is a result of the hard-limitation of the waveforms on the input, the resulting shift is a complicated function of the transistor's terminal impedances and the internal impedance of the generator.

Equivalent case is where the impedance of the source varies for a given transistor in a chosen bias configuration. This case is somewhat more relevant for the circuit design since the source impedance is determined by the input matching network, which is the result of a desired circuit

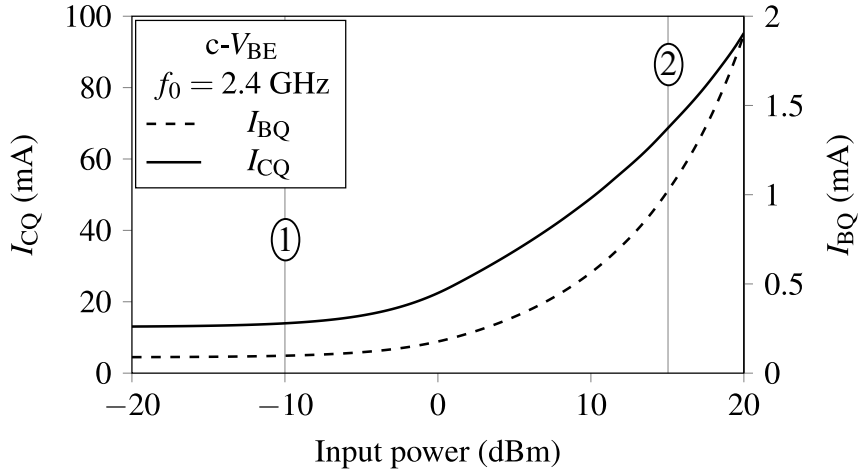


Figure 3.18: Simulated DC base current I_{BQ} and collector current I_{CQ} for the HCBT with the emitter width of 325 μm and for the c-V_{BE} biasing. The bias point (in the small-signal range) is $(I_{CQ}, V_{CEQ}) = (13\text{ mA}, 1.5\text{ V})$. The numbers are references for the simulation in Fig. 3.19.

performance, i.e., an input match for either gain, linearity, and/or efficiency. Thus, the HCBT with $w_E = 150\ \mu$m is simulated for two extreme source impedances of 1 Ω and 245 Ω, wherein the impedances are chosen such as to result in the same gain. The load impedance is 50 Ω and the bias configuration is constant-V_{BE}. The DC base and collector currents and input time-domain waveforms are shown in Fig. 3.17. As expected, for low source impedance, the base-emitter voltage is a sine wave, whereas the base current is distorted, as shown in Fig. 3.17b. The opposite holds for the high source impedance in Fig. 3.17d. Since the load line at the output is the same for both cases, the load line undergoes equal hard-limitation and has the same impact on the bias point. The DC collector current behaves the same in both cases, whereas the base current increases more gradually for the $Z_S = 245\ \Omega$ case [see Fig. 3.17c]. But regardless of the nature of the hard-limitation present on the input, the effect is almost the same; both base and collector DC current increase. Additionally, it is evident that there is no benefit with respect to linearity between the two cases, namely, the gain compression region occurs for the same input power. But, a relatively small difference in performance is expected due to a slight difference in DC base current behaviour [see Fig. 3.17a,c].

Hard-limitation in cut-off

To investigate the cause of the bias shift, the time-domain waveforms in the base-emitter circuit are simulated for the cases of hard-limitation in the cut-off and saturation, for both the constant-V_{BE} and constant-I_B. The case of hard-limitation in the cut-off region is simulated for the HCBT of the same emitter width as the measured device, i.e., $w_E = 325\ \mu$m. Firstly, the behaviour of DC base and collector currents is simulated, as shown in Fig. 3.18. The simulation results are qualitatively equal to the measurements, i.e., there is an increase of both the I_{BQ} and I_{CQ} with the input power [see Fig. 3.18]. Additionally, there is a change of slope of I_{CQ} for the input power

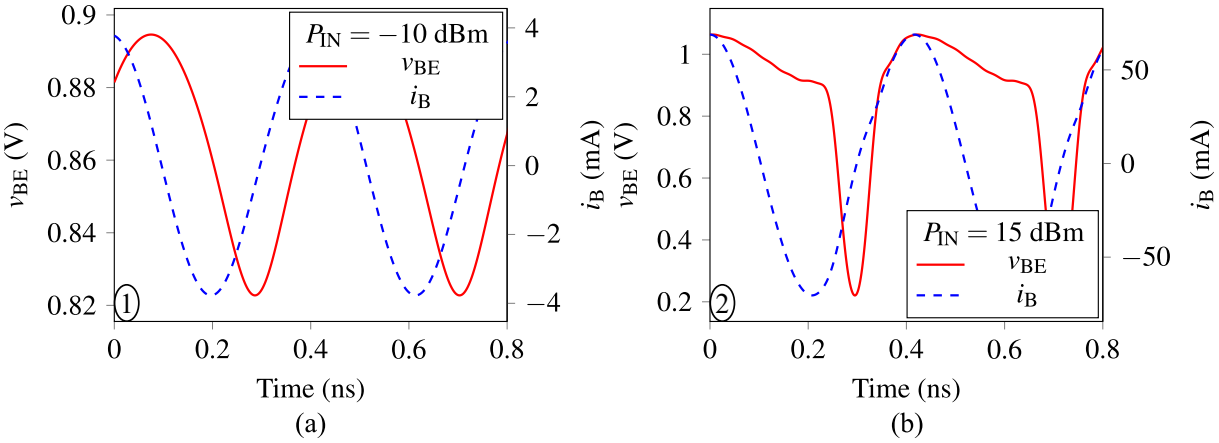


Figure 3.19: Simulated base-emitter voltage v_{BE} and base current i_B for the input power of (a) -10 dBm and (b) 15 dBm, for the hard-limitation in the cut-off and c-V_{BE} biasing. The bias point (in the small-signal range) is $(I_{CQ}, V_{CEQ}) = (13\text{ mA}, 1.5\text{ V})$. $Z_L = 20\ \Omega$; $Z_S = 50\ \Omega$.

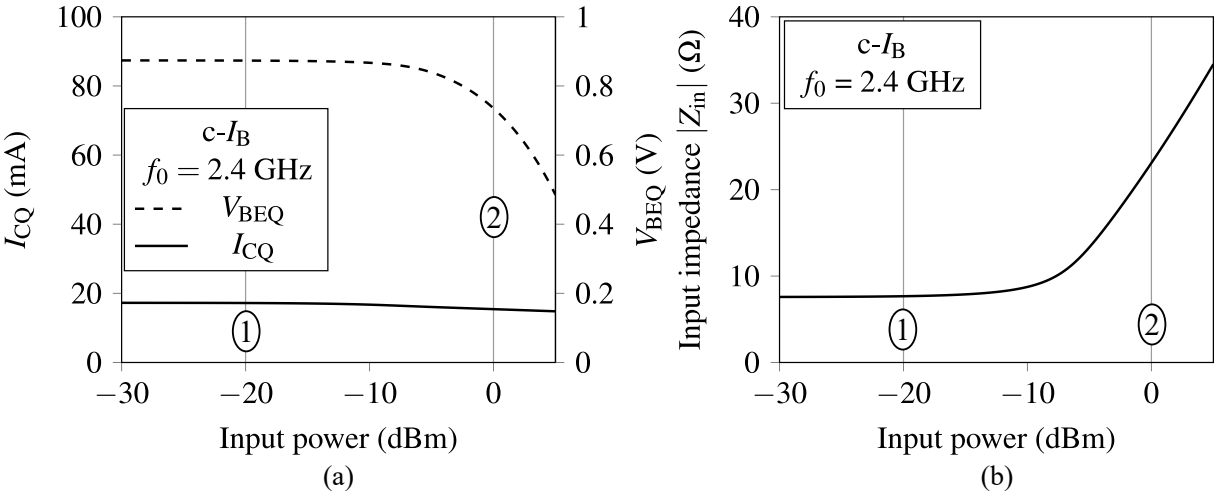


Figure 3.20: Simulated (a) DC base-emitter voltage V_{BE} and collector current I_{CQ}, and (b) input impedance Z_{IN} as a function of input power, for the HCBT with the emitter width of 325 μm and for the c-I_B biasing. The bias point (in the small-signal range) is $(I_{CQ}, V_{CEQ}) = (13\text{ mA}, 1.5\text{ V})$. The numbers are references for the simulations of Fig. 3.21.

higher than around 12 dBm. To find out the cause of the current increase, the base-emitter voltage and base current are simulated in two interesting points shown in Fig. 1.17, namely, in the small-signal region [$P_{IN} = -10$ dBm - (1)] and the range of I_{CQ} increase [$P_{IN} = 15$ dBm - (2)]. The time-domain waveforms are shown in Fig. 3.19. Since the input impedance of the simulated device is much lower than the internal generator impedance of 50 Ω [see Fig. 3.15a], the generator is regarded as a current source, which explains the base current sine wave for both input power levels. The hard-limitation is present mainly in the base-emitter voltage waveform, as shown in Fig. 3.19b. Thus, the nonlinearity of the v_{BE} waveform is the cause of the bias point shift shown in Fig. 3.18.

The same simulations are performed for the biasing with a current source (c-I_B), as shown in Fig. 3.20 and Fig. 3.21. The behaviour of DC base-emitter voltage and collector current is

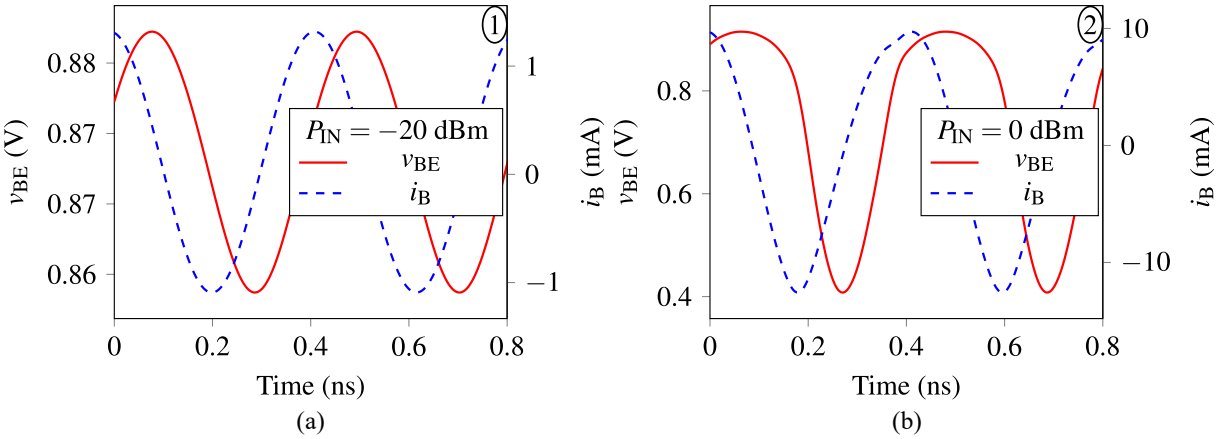


Figure 3.21: Simulated base-emitter voltage v_{BE} and base current i_B for the input power of (a) -20 dBm and (b) 0 dBm, for the hard-limitation in the cut-off and c-I_B biasing. The bias point (in the small-signal range) is $(I_{CQ}, V_{CEQ}) = (13\text{ mA}, 1.5\text{ V})$. $Z_L = 20\ \Omega$; $Z_S = 50\ \Omega$.

qualitatively the same as the measured one from Fig. 3.11. Namely, the V_{BEQ} decreases, whereas the I_{CQ} remains relatively constant, with the increase in input power. Nevertheless, the input impedance of the transistor now increases to around 20 Ω for $P_{IN} = 0$ dBm, which is relatively close to the internal impedance of the generator of 50 Ω. The result is a distortion of both the base-emitter voltage and base current in large-signal regime, as shown in Fig. 3.20b. Thus, the input impedance decreases with input power for the c-V_{BE} biasing [see Fig. 3.15a], whereas it increases for the c-I_B. The hard-limitation at the input impacts the bias point shift at the output in a complicated manner, since neither the voltage nor the current on the base-emitter side are pure sine waves. Nevertheless, the simulations confirm the measurements performed and they further illustrate the complex nature of the DC and RF interaction in the bipolar transistor in large-signal operation.

Hard-limitation in saturation

The hard-limitation in the saturation region is also simulated to analyze the cause of the bias point shift in the compression region for both bias configurations. The bias point and load impedance are set the same as in the measurements of Fig. 3.12, i.e., (I_{CQ}, V_{CEQ}) = (58 mA, 1 V) and $Z_L = 50\ \Omega$. The DC base and collector currents are simulated as a function of input power in Fig. 3.22a. Although the hard-limitation at the output occurs in the saturation region, the DC currents behave the same as for the case of hard-limitation in the cut-off, which is additional confirmation that the base-emitter circuit is responsible for the bias point shift at the output. Once again, the input impedance is simulated to verify that the generator acts for this case as a current generator, which is visible in Fig. 3.22b. The time-domain waveforms of the base-emitter circuit are shown in Fig. 3.23. Again, the base current is a pure sine wave, whereas the distortion occurs in the base-emitter voltage waveform. The simulations for the c-I_B are shown in Fig. 3.24 and Fig. 3.25. Both DC collector current and base-emitter voltage decrease

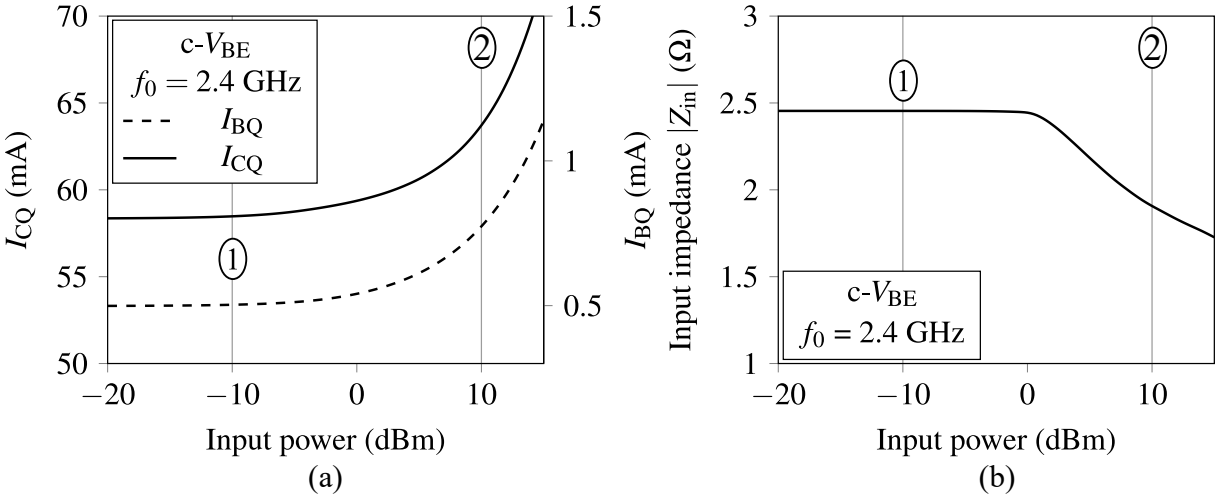


Figure 3.22: Simulated (a) DC base current I_{BQ} and collector current I_{CQ}, and (b) input impedance Z_{IN} as a function of input power, for the HCBT with the emitter width of 325 μm and for the c-V_{BE} biasing and hard-limitation in the saturation region. The bias point (in the small-signal range) is (I_{CQ}, V_{CEQ}) = (58 mA, 1 V). The numbers are references for the simulations of Fig. 3.23.

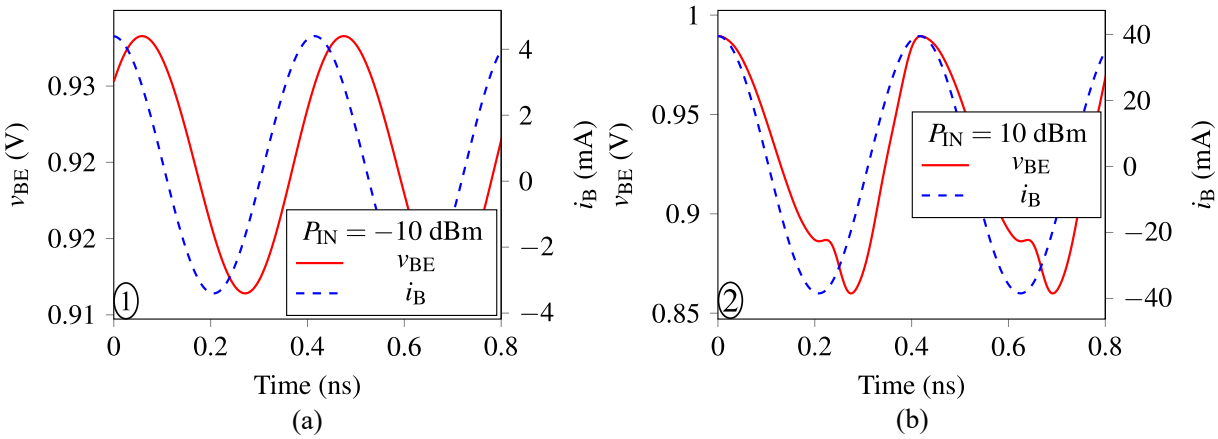


Figure 3.23: Simulated base-emitter voltage v_{BE} and base current i_B for the input power of (a) -10 dBm and (b) 10 dBm, for the hard-limitation in the saturation and c-V_{BE} biasing. The bias point (in the small-signal range) is (I_{CQ}, V_{CEQ}) = (58 mA, 1 V). $Z_L = 50$ Ω; $Z_S = 50$ Ω.

with input power in large-signal range, the same result as the measurements shown in Fig. 3.12. The input impedance increases, but it equals 5 Ω at higher input power of 10 dBm, which is still much lower impedance than the impedance of the generator. Thus, the base current is a pure sine wave for both input power levels, as shown in Fig. 3.25.

The impact of large-signal operation on bias point of Horizontal Current Bipolar Transistor (HCBT) is shown by measuring dynamic load lines at the fundamental frequency of 2.4 GHz using calibrated time-domain load-pull setup. It is shown that the hard-limitation at the cut-off provides larger linear operating range for c-V_{BE} bias compared to c-I_B bias, but a smaller linear range with the hard-limitation in the saturation. A 5% higher collector efficiency is measured in the back-off range for c-V_{BE} bias while targeting the same P1dB output power in both bias configurations. The results provide a useful information for the power amplifier design since

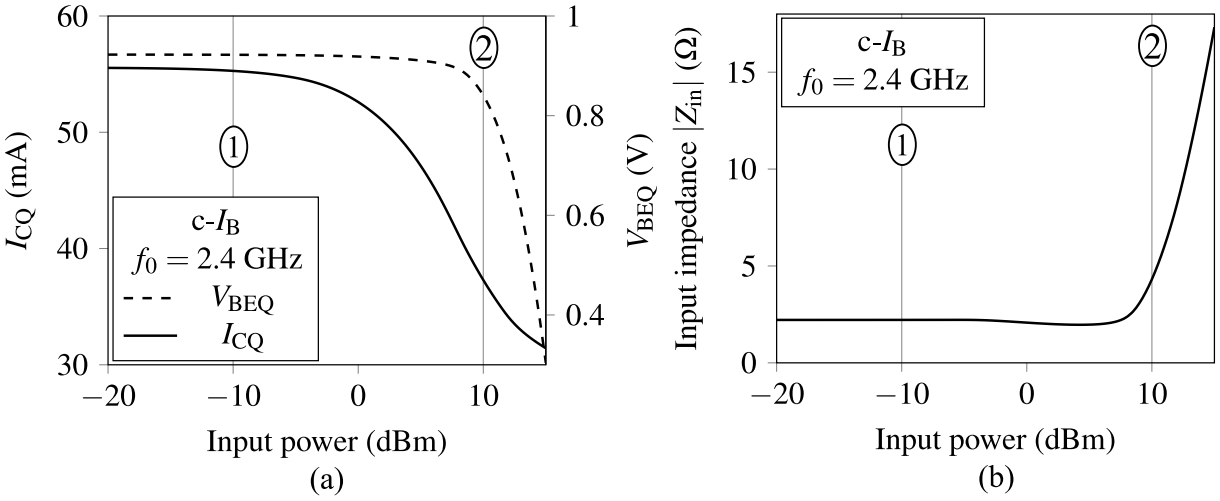


Figure 3.24: Simulated (a) DC base current I_{BQ} and collector current I_{CQ}, and (b) input impedance Z_{IN} as a function of input power, for the HCBT with the emitter width of 325 μm and for the c-V_{BE} biasing and hard-limitation in the saturation region. The bias point (in the small-signal range) is (I_{CQ}, V_{CEQ}) = (58 mA, 1 V). The numbers are references for the simulations of Fig. 3.22.

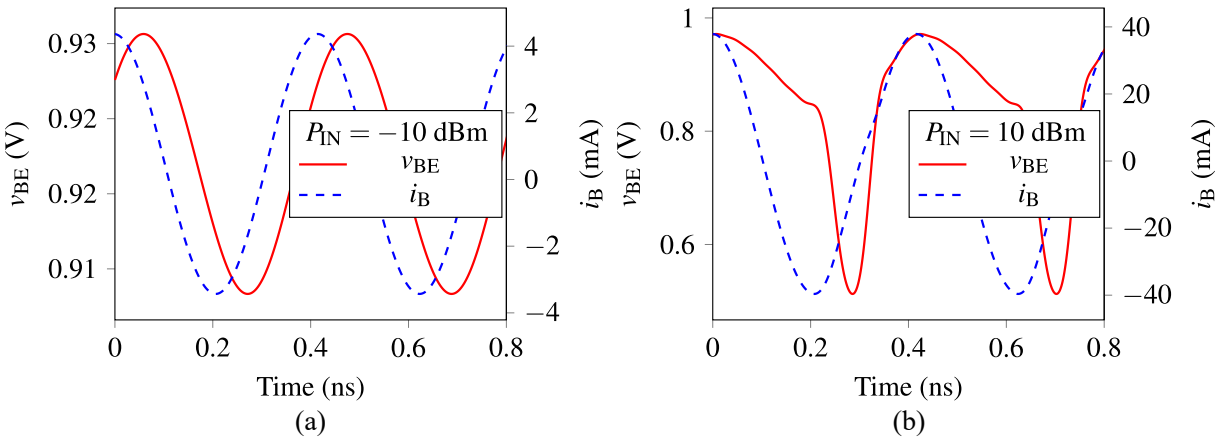


Figure 3.25: Simulated base-emitter voltage v_{BE} and base current i_B for the input power of (a) -10 dBm and (b) 10 dBm, for the hard-limitation in the saturation and c-I_B biasing. The bias point (in the small-signal range) is (I_{CQ}, V_{CEQ}) = (58 mA, 1 V). $Z_L = 50\ \Omega$; $Z_S = 50\ \Omega$.

the performance depends on the bias point in large-signal operation. By facilitating the equal amount of hard-limitation at the saturation and cut-off regions, an optimized Class-A operation can be achieved wherein there is no bias point shift due to the cancellation of the two distortion mechanisms.

The linear operating range of the HCBT is bounded by the compression boundary, which arises due to the Kirk effect taking place at high collector currents. The behaviour of Kirk effect cannot be inferred from the DC measurements and, therefore, a time-domain waveforms measurement at GHz frequencies are a useful tool to map the boundary of linear operating range for a BJT or a MOS transistor. The boundary impacts the bias point in large-signal operation, and this impact is analyzed for the HCBT by both the measurements and harmonic balance simulations. Due to the change of input impedance of the transistor with input power, the

input generator acts as a current or voltage source, depending on the relative difference between the input impedance and internal generator impedance. Although there is a hard-limitation of different collector-emitter voltage and collector current half-waves at the output for the c-V_{BE} and c-I_B biasing configurations, both cases provide equal bias point behaviour in large-signal operation; which confirms the fact that the shift is mainly attributed to the nonlinearity present in the base-emitter circuit. The findings are of an importance for the optimization of operation in Class-A regime, wherein a proper bias point and load/source impedances need to be found to achieve a desired linearity and avoid the shift in bias point, which deteriorates the efficiency and output power.

Chapter 4

Doherty power amplifier

Since the efficiency is becoming the most important parameter of a power amplifier employed in wireless communications, different circuit architectures are proliferating which combine many simpler power amplifiers into a more complex and high-efficiency architectures. Such a circuit is significantly more efficient, but, on the other hand, less linear. Nevertheless, high efficiency is usually aimed for during the power amplifier design, whereas the linearity is corrected for in the digital domain. Furthermore, radiofrequency power amplifiers are the components consuming the highest amount of power both in mobile handsets and base stations, in the former determining the life span of a battery, whereas in the latter, increasing the cost of the cooling system. The goal is to amplify signals with high fidelity while operating with high efficiency, in order to increase the life span of the battery and/or reduce the cooling costs. Additionally, with the advent of wideband communication standards, power amplifiers need to maintain high efficiency over the entire signal modulation bandwidth, and, if possible, over more than one frequency band. The main culprit is the large Peak-to-Average-Power-Ratio (PAPR) of a wideband signal to be amplified, since PAs operate with maximum efficiency only for a single input power level.

4.1 Active load modulation

Doherty PA consists of two amplifiers, carrier PA and peaking PA, wherein the peaking PA actively modulates the load impedance of carrier PA in order to keep it optimally matched in the back-off power range [15], as shown in Fig. 4.1a. In the most common configuration, the carrier PA is biased in Class AB mode and peaking PA is biased in Class C mode. The input power is equally split at the input, and, therefore, this configuration is called a symmetrical Doherty power amplifier. There are two distinct points of operation of a symmetrical Doherty PA; full output power and 6-dB output power back-off.

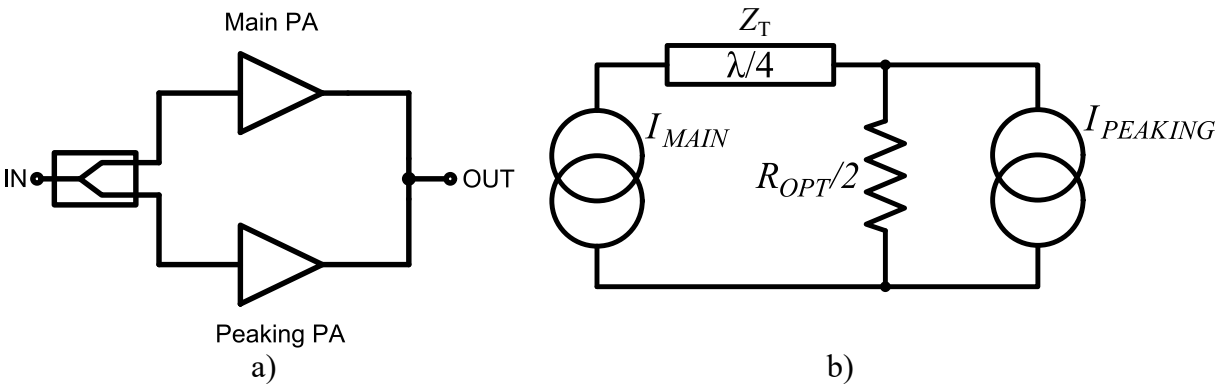


Figure 4.1: (a) Block diagram and (b) simplified schematic of a symmetrical Doherty power amplifier.

4.1.1 Full output power

At full output power, main and peaking PA operate at their peak output power, which is equal since the two are fed the equal input signal. The two amplifiers are designed such as to be equal at maximum output power, in order for each to provide equal output power. The output signals are then combined at the output. As shown in Fig. 4.1a, the outputs of the amplifiers are directly connected, with no signal combiner, thus, the outputs are not isolated from each other. This is to enable the main action of the Doherty amplifier; an active load modulation.

The carrier PA sees an impedance which is a function of the output signal of the peaking PA. The concept is explained by the simplified schematic shown in Fig. 4.1b. The two outputs are connected in parallel with the termination resistance R_{OPT}. If the quarter-wave transformer is neglected at first, the two current sources are connected in parallel with the load resistor, and the resistance seen by the output of the carrier PA is [15]

$$Z = \frac{R_{\mathrm{OPT}}}{2}\left(1+\frac{I_2}{I_1}\right), \tag{4.1}$$

where $I_1 = I_{\mathrm{MAIN}}$ and $I_2 = I_{\mathrm{PEAKING}}$ are the output currents of the main and peaking PAs, respectively. Therefore, at full output power, the two output currents are the same and equal to $I_{\mathrm{max}}/2$, where the I_{max} is the maximum output current swing of the amplifiers. Then, according to (4.4), the main PA sees

$$Z_{\mathrm{full}} = R_{\mathrm{OPT}}, \tag{4.2}$$

which means that it is terminated by the optimal impedance R_{OPT}. Similarly, the peaking PA also sees R_{OPT} since the two PAs provide the same output power at full drive.

4.1.2 6-dB output power back-off

When the input signal power is reduced from the full drive, the main PA termination impedance changes, which is in effect a load-pull of the main PA by the output of the peaking PA. If the quarter-wave transformer of characteristic impedance Z_{T} is placed between the output of the main PA and the load, the impedance seen by the output of the main PA is

$$Z = \frac{2Z_{\mathrm{T}}^2}{R_{\mathrm{OPT}}\left(1 + \frac{I_2 Z_{\mathrm{T}}}{V_1}\right)}, \tag{4.3}$$

where V_1 is the voltage across the output of the main PA. Therefore, when the input drive decreases, the current I_2 also decreases, which, according to (4.3), increases the impedance Z. Accordingly, the output power also decreases, and at some point the peaking PA is completely shut off due to the Class-C biasing. If the characteristic impedance of the quarter-wave transformer is chosen equal to R_{OPT}, according to (4.3) the main PA is terminated by

$$Z_{\mathrm{OPBO}} = 2R_{\mathrm{OPT}}, \tag{4.4}$$

where Z_{OPBO} is the load of the main PA in output power back-off power range when the peaking shuts off. The output power when the peaking PA shuts off is four times lower, since the output power of main PA is two times lower. Therefore, the point when the peaking PA shuts off is at 6-dB output power back-off (OPBO). The impedance at this input power value is twice the impedance at full drive. Therefore, the main PA is terminated by $2R_{\mathrm{OPT}}$ at 6-dB OPBO, whereas by R_{OPT} at full drive. This causes equal output voltage of main PA at both 6-dB back-off and full drive. Furthermore, in the entire 6-dB power back-off range, the output voltage of the main PA is constant, regardless of the decreasing output current I_1 and I_2. Although the output current of the main PA I_1 decreases in the back-off range, the output voltage V_1 remains constant, which causes the efficiency to stay at the maximum value in the back-off range also. The efficiency as a function of input power level, if the Class-B main PA is assumed, is given by

$$\eta = \frac{\pi}{2} \frac{\left(\frac{v_{\mathrm{in}}}{V_{\mathrm{max}}}\right)^2}{3\left(\frac{v_{\mathrm{in}}}{V_{\mathrm{max}}}\right) - 1}, \tag{4.5}$$

which gives the efficiency of $\pi/4$ at two input voltage levels; V_{max} at full drive, and $V_{\mathrm{max}}/2$ at 6-dB output power back-off.

The efficiency as a function of input power is shown graphically on the Fig. 4.2. At full drive and 6-dB back-off, the Doherty achieves maximum efficiency of 78.5% (if Class-B operation

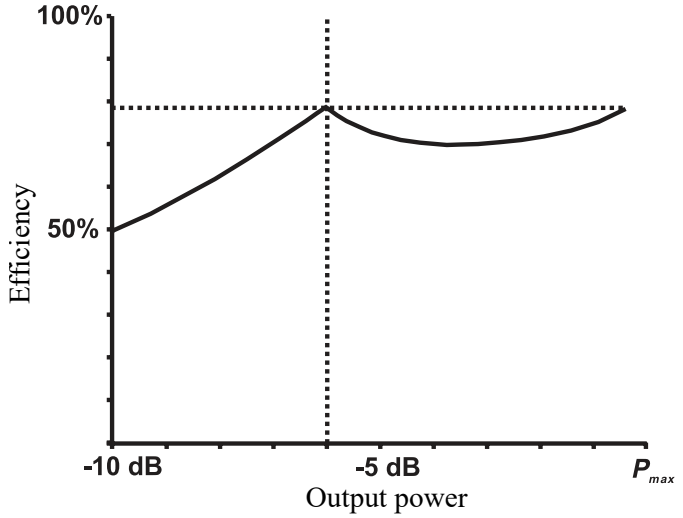


Figure 4.2: Efficiency as a function of output power of a symmetrical Doherty power amplifier.

is assumed). In the back-off range from 6-dB up to $P_{\max}$, there is a slight efficiency drop of a few percent. This is the result of the efficiency of the peaking PA, which is lower than the maximum for a power lower than $P_{\max}$. This causes the overall efficiency of the Doherty to be slightly less than the maximum in the back-off range. Therefore, the symmetrical Doherty PA exhibits maximum efficiency at both 6-dB back-off and full drive, which is suitable for modulated signals of 6-dB PAPR.

4.2 Load-pull analysis

The analysis presented so far assumes ideal current sources for the outputs of the main and peaking amplifiers, whereas the amplifiers have finite output impedance. Furthermore, this output impedance is a nonlinear function of input power and, thus, the optimal matching impedances for both 6-dB back-off and full drive are best found by load-pull measurements.

Load-pull setup, employing automated mechanical impedance tuners [82], is used to find the optimal output matching impedances for the HCBT device with $A_{\mathrm{E}} = 31.2\ \mu\mathrm{m}^2$ at 2.4 GHz. Optimal impedances at both full power and 6-dB OPBO are shown in Fig. 4.3. Load-pull analysis is performed for Class-AB biased HCBT, with a collector current and collector-emitter voltage of 20 mA and 2.87 V, respectively. At full output power, both PAs work at maximum power of $P_{\mathrm{MAX}} = 19.5$ dBm and collector efficiency of 46%, which are measured for Z_{OPT1}.

At 6 dB output power back-off, peaking PA is turned off whereas the main PA provides $P_{\mathrm{MAX}} - 3$ dBm output power. Simultaneously, efficiency should be as high as possible, with the peak at 6-dB OPBO. Therefore, the load-pull is performed again to find the impedance for maximum collector efficiency with $P_{\mathrm{MAX}} - 3 = 16.5$ dBm.

The two measured optimal load impedances Z_{OPT1} and Z_{OPT2} are the analogous to the optimal load resistances R_{OPT} and $2R_{\mathrm{OPT}}$, respectively, from the analysis of sec. 4.1. The active

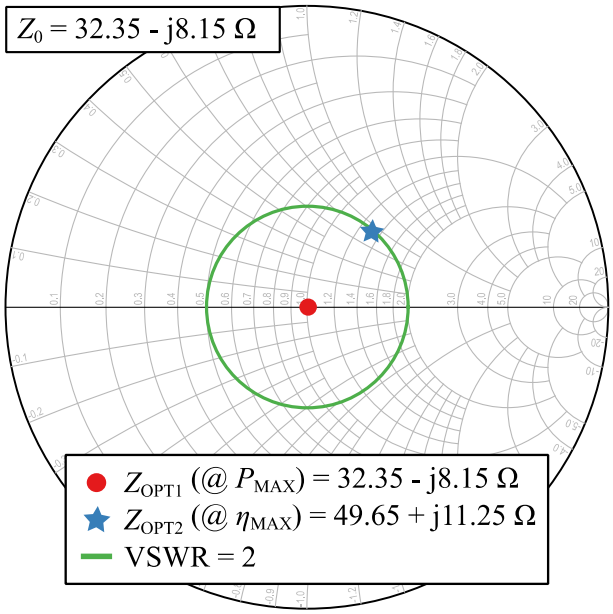


Figure 4.3: Matching impedances for maximum output power and maximum collector efficiency of the HCBT with $A_E = 31.2\ \mu m^2$ measured using load-pull setup. The load impedance is transformed from Z_{OPT1} at full power to Z_{OPT2} at 6-dB OPBO. The impedance for maximum efficiency is chosen on the VSWR = 2 circle centered on $Z_{OPT1} = Z_0$.

load-pull modulates the Z_{OPT1} at full drive to Z_{OPT2} at 6-dB back-off. Therefore, the output of the main PA should be presented with Z_{OPT2} at 6-dB back-off, whereas at full drive, both main and peaking PAs should see Z_{OPT1}.

4.3 Matching network design

4.3.1 Main PA output matching network

The role of peaking PA is to modulate the load impedance presented to main PA. This modulation sets the load impedance to 50 Ω at full drive, where both PAs contribute equal output power. Thus, the main amplifier's output matching network (OMN) should transform 50 Ω to Z_{OPT1}. The matching network employing ideal transmission lines is shown in Fig. 4.4a. The necessary transformation from 50 Ω to Z_{OPT1} is achieved by using transmission lines TLIN1 and TLIN2 with the electrical length of 29° and 21.5°, respectively. On the other hand, at 6-dB back-off, the load impedance is 25 Ω since the load is not modulated by the peaking PA, which is turned off at this power level. The system impedance of 50 Ω is transformed to 25 Ω employing quarter-wave transmission line of $Z_0 = 35.35$ Ω. In order to keep the main PA at the maximum possible efficiency in the back-off, the TLIN3 is added to match the output of the main PA to Z_{OPT2} at 6-dB back-off. Since the characteristic impedance of TLIN3 is 50 Ω, the main PA does not change the match of the peaking amplifier at full power since the load impedance at full power is also 50 Ω. The network is optimized in electromagnetic (EM) sim-

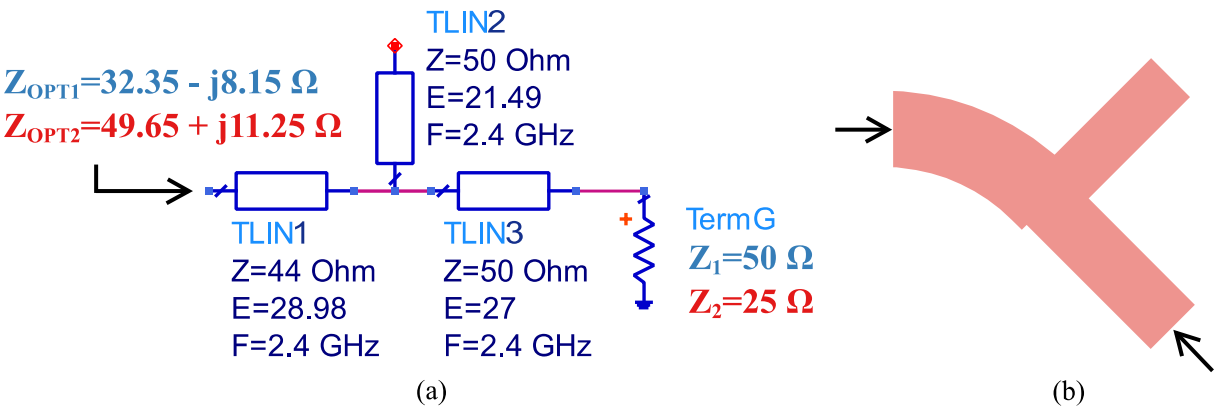


Figure 4.4: Output matching network of main PA. (a) TLIN1 and TLIN2 transform the load impedance at full output power ($Z_1 = 50\ \Omega$) to Z_{OPT1}. With TLIN3 added, the load impedance $Z_2 = 25\ \Omega$ is transformed to Z_{OPT2} at 6-dB output power back-off. (b) Layout of the output matching network with curvature added to facilitate power combining at the output.

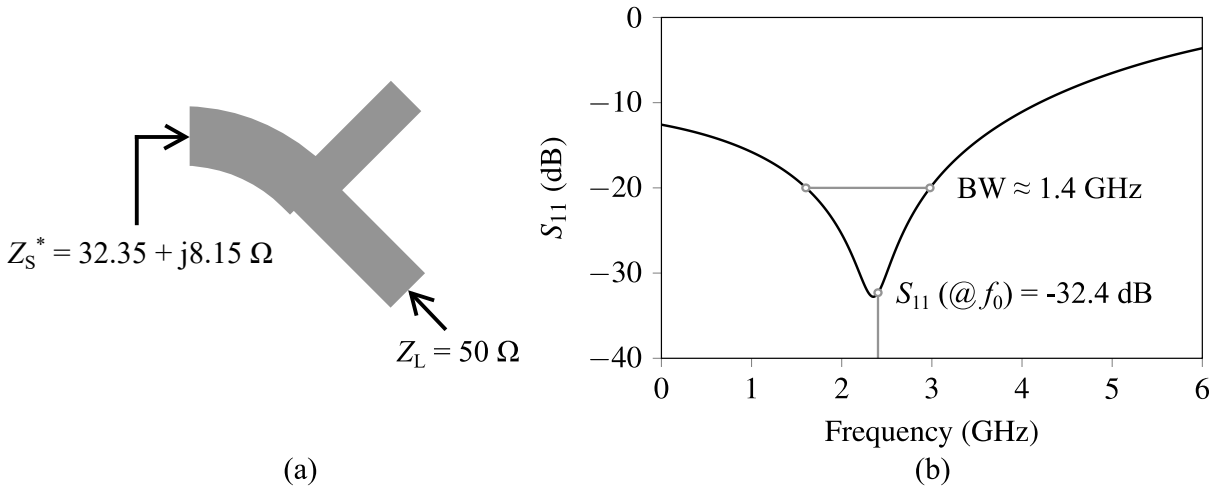


Figure 4.5: The characteristics of the main PA output matching network at full drive. (a) Layout for the EM simulation, and (b) EM-simulated input reflection coefficient S_{11} for $Z_S = 32.35 - j8.15\ \Omega$ and $Z_L = 50\ \Omega$.

ulator. The layout of the main amplifier's output matching network is shown in Fig. 4.4b. The TLIN1 is made with a slight curvature which is to facilitate the connection of the outputs of the main and peaking PAs.

The performance of the output matching network of the main PA transistor is shown in Fig.4.5 in the full output power point, i.e., wherein the peaking PA is fully on. Thus, the load termination is equal to 50 Ω and the optimal output matching impedance of the main PA is the Z_{OPT1} from Fig. 4.4b. The EM-simulated input reflection coefficient of the output matching network shown in Fig. 4.4b, wherein the source impedance is equal to a complex-conjugate of Z_{OPT1} and $Z_L = 50\ \Omega$ [see Fig. 4.5a], is shown in Fig 4.5b. Due to the optimal matching impedance being relatively close to 50 Ω for this HCBT, a wideband is achieved by employing a simple matching network layout. Namely, the S_{11} is lower than -20 dB over the bandwidth of around 1.4 GHz, whereas at the design frequency of 2.4 GHz, the matching is excellent

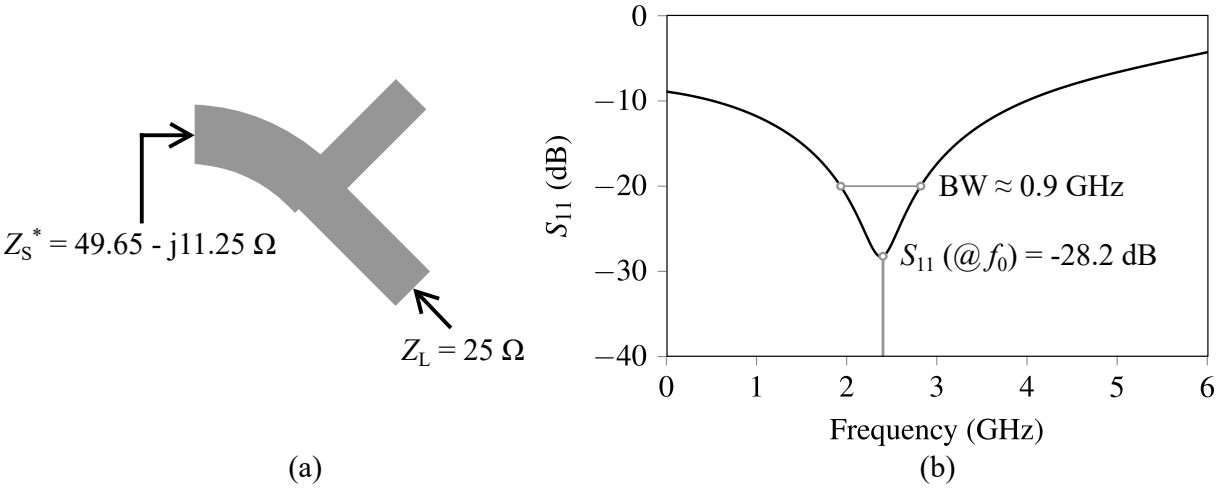


Figure 4.6: The characteristics of the main PA output matching network at full output power. (a) Layout for the EM simulation, and (b) EM-simulated input reflection coefficient S_{11} for $Z_S = 49.65 + j11.25$ Ω and $Z_L = 25$ Ω.

($S_{11} = -32.4$ dB).

The same network is simulated with $Z_S = Z_{OPT}$ and $Z_L = 25$ Ω, which is point of 6-dB output power back-off. In this point, the load impedance drops to 25 Ω due to the active load modulation of the peaking PA. Again, a relatively wide bandwidth of 0.9 GHz is achieved with $S_{11} = -28.2$ dB at the f_0. The performance is somewhat lower with respect to the 50-Ω-load shown in Fig. 4.5, since now a third line, TLIN3 [see Fig. 4.4a], does the impedance transformation along with TLIN1 and TLIN2. Thus, the electrical length of the output matching network is larger and, additionally, the resistive loss is higher, which degrades the match at the fundamental frequency.

4.3.2 Peaking PA output matching network

At full output power, the peaking PA provides the same power as the main PA, thus it should be matched to its optimal impedance for P_{MAX} output power, thus, the output matching network is the same as the one of the main PA. Additionally, the third line TLIN3 is also added although it is not necessary at the output of the peaking PA. Such arrangement provides equal phase shift at the output in both the main and peaking branches of the Doherty PA. Furthermore, input matching network is designed as a complex-conjugate match and is the same for both amplifiers. For output power up to 6-dB back-off, only main PA provides output power while peaking PA is turned off. Maximum efficiency in this power region is achieved at 6-dB OPBO with the main PA matched by Z_{OPT2}. Since the outputs of the PAs are connected in parallel, the impedance of peaking PA should be as high as possible so as not to change the load impedance, which is equal to 25 Ω. For this purpose, the small-signal output impedance is extracted from *S*-parameter measurements of HCBT in Class-C bias, which is set by the base-emitter voltage, collector

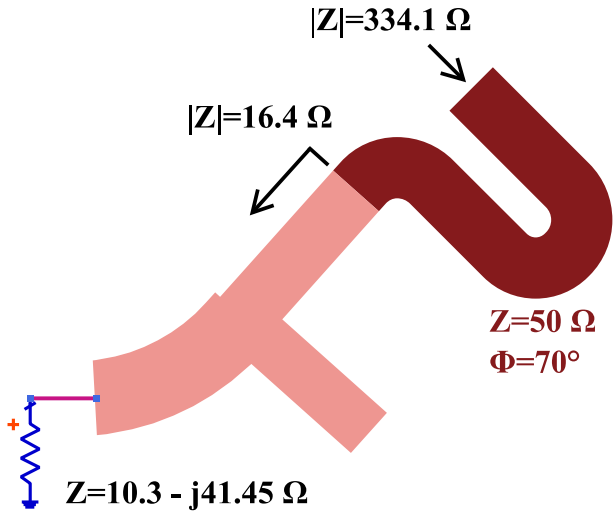


Figure 4.7: Layout of the output matching network of peaking PA. Matching network is the same as the one of main PA except the 50-Ω transmission line used for the impedance transformation.

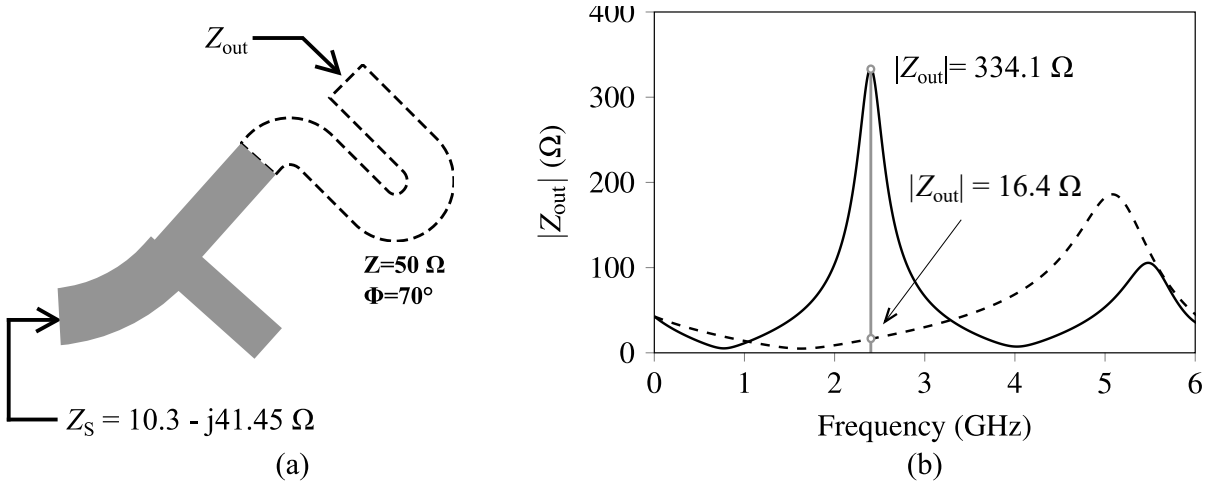


Figure 4.8: The characteristics of the peaking PA output matching network at 6-dB output power back-off. (a) Layout for the EM simulation (dashed is the additional 70° phase shift line), and (b) EM-simulated magnitude of the output impedance Z_{out} for $Z_S = 10.3 - j41.45$ Ω.

current, and collector-emitter voltage of 0 V, 0 mA, and 2.87 V, respectively. Measured output impedance at 2.4 GHz is $10.3 - j41.45$ Ω, the absolute value of which equals 42.7 Ω. With the output matching network, impedance is very low, equalling 16.4 Ω, as shown in Fig. 4.7. Therefore, the output impedance of peaking PA is low at the frequency of operation and would lower the 25 Ω at the output significantly thus degrading the efficiency at 6-dB back-off level. To maximize the output impedance of the peaking PA in the off-state, a 50-Ω phase shift line is placed after the matching network to transform the impedance to the maximum possible value, which resulted in 334.1 Ω. Because of the added line, additional phase shift of 70° is introduced at the output of the peaking PA branch.

The performance of the peaking PA matching network is again simulated by EM simulations, as shown in Fig. 4.8. Similar to the TLIN3 line of the output matching network of the

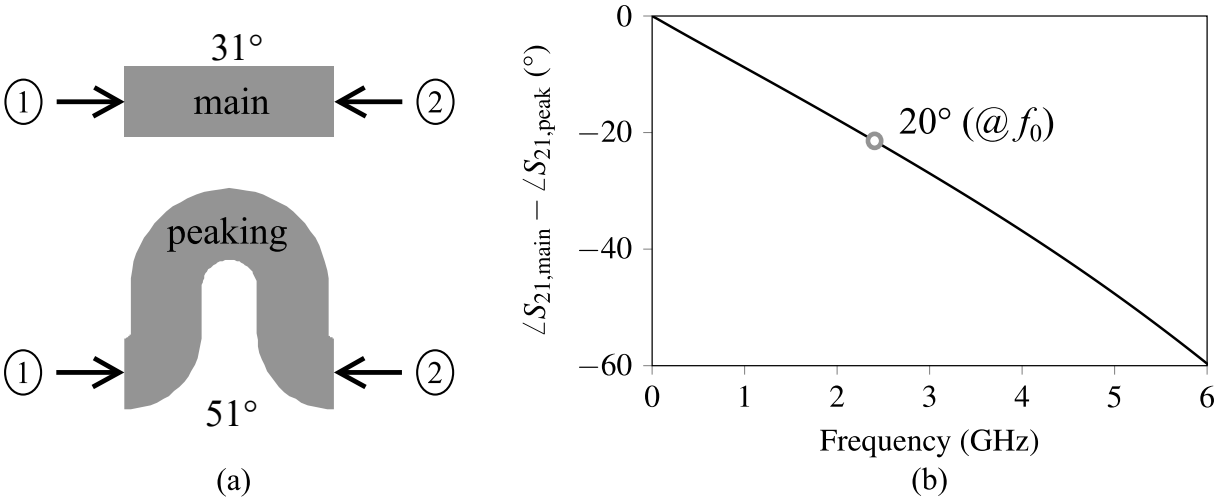


Figure 4.9: The characteristics of the phase shift lines on the input. (a) Layout for the EM simulation, and (b) EM-simulated difference between the phases of the transmission coefficients S_{21}, $\angle S_{21,\text{main}} - S_{21,\text{peak}}$.

main PA, the additional phase shift line is of $Z_0 = 50\ \Omega$, so that it is effectively non-existent in the point of full drive where $Z_\text{L} = 50\ \Omega$. The Fig. 4.8 shows the simulated impedance looking from the output towards the peaking PA for the matching network with and without the additional 50-Ω phase shift line. As mentioned previously, by adding an additional 70° phase shift line, the output impedance increases from 16.4 Ω to 334.1 Ω. Since the electrical length of the phase shift line is relatively large, the bandwidth of the high-impedance region is narrow, which is the main bottleneck for the bandwidth of this Doherty PA. At full drive, the peaking PA behaves the same as the main PA since their matching networks are equal.

4.3.3 Input signal split and phase shift

Input power is split using 3-dB hybrid coupler with 90° phase shift between the output signals, wherein the 90°-signal is brought to the input of main PA. Since the output signals of the main PA and peaking PA must be in-phase at the combining point, additional phase shift, introduced by the impedance transformation at the output of the peaking PA, is countered by phase shift lines at the input. Phase shift lines with $Z_0 = 50\ \Omega$ are placed at the input of the main and peaking branches, with 31° and 51° phase shift, respectively, thus equalizing the phase shift in both branches and enabling in-phase addition of the signals at the combining point.

Again, the performance of the phase shift lines is simulated by employing EM simulations, as shown in Fig. 4.9. As shown in Fig. 4.9a, the phase shift line of the main amplifier is meandered in order to achieve the effective physical length of the peaking line, which facilitates the component placement on the board. The excess phase difference of 20° between the main and peaking paths is cancelled with these two lines, which provide counter-phase shift of the same value at the fundamental frequency of 2.4 GHz [see Fig. 4.9b]. Both lines are of a characteristics impedance of 50 Ω so that minimal loss is added at the input.

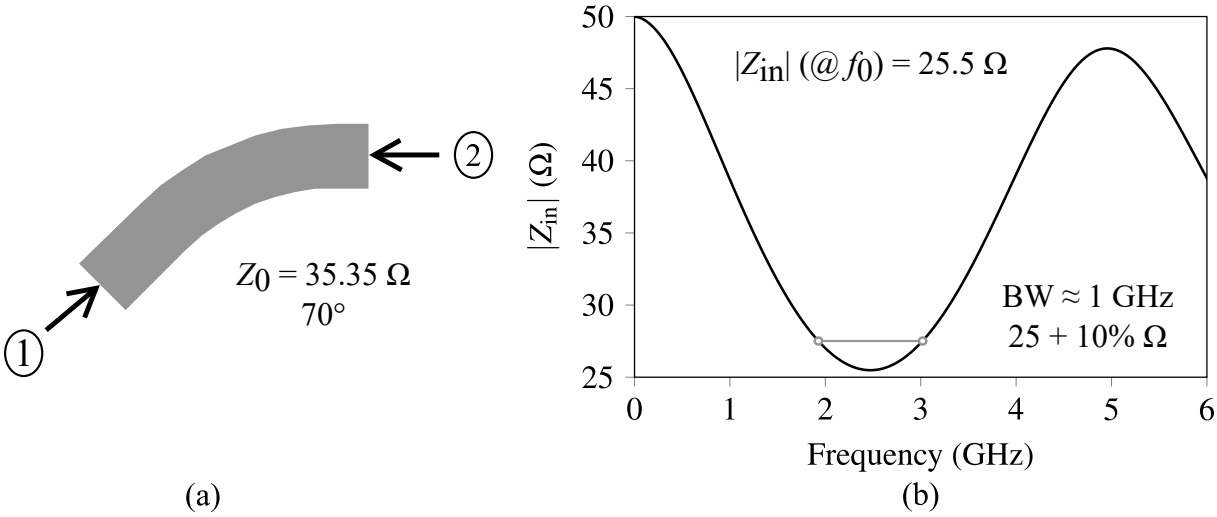


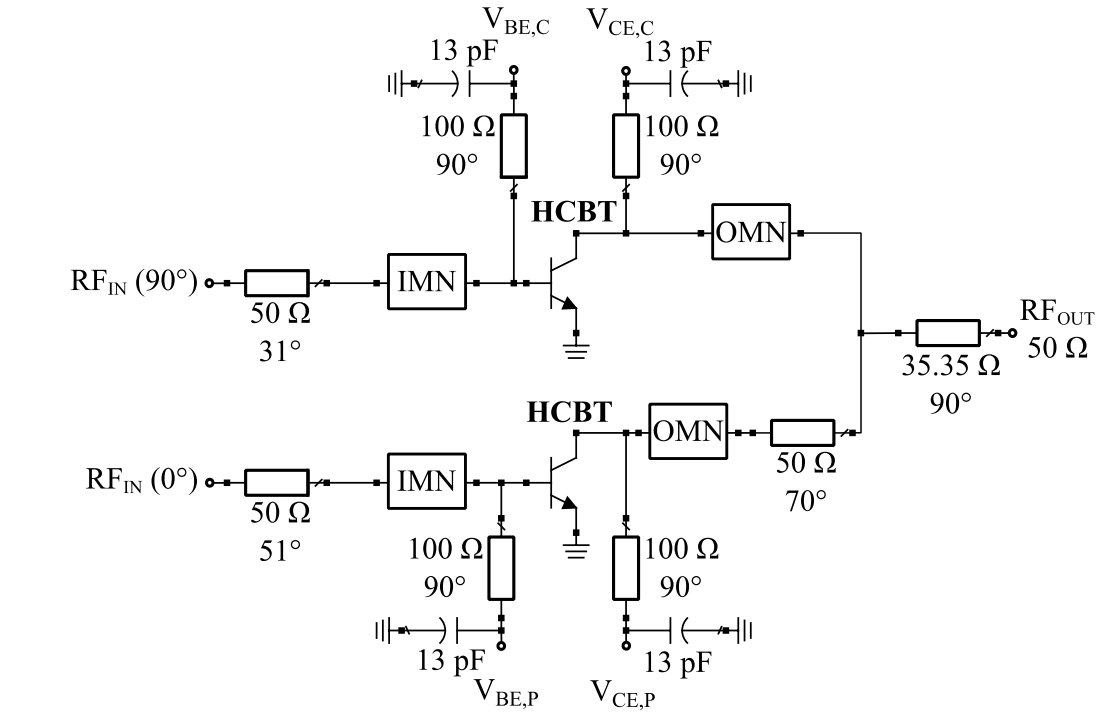
Figure 4.10: The characteristics of the phase shift lines on the input. (a) Layout for the EM simulation, and (b) EM-simulated difference between the phases of the transmission coefficients S_{21}, $\angle S_{21,\text{main}} - S_{21,\text{peak}}$.

4.3.4 Output quarter-wave transformer

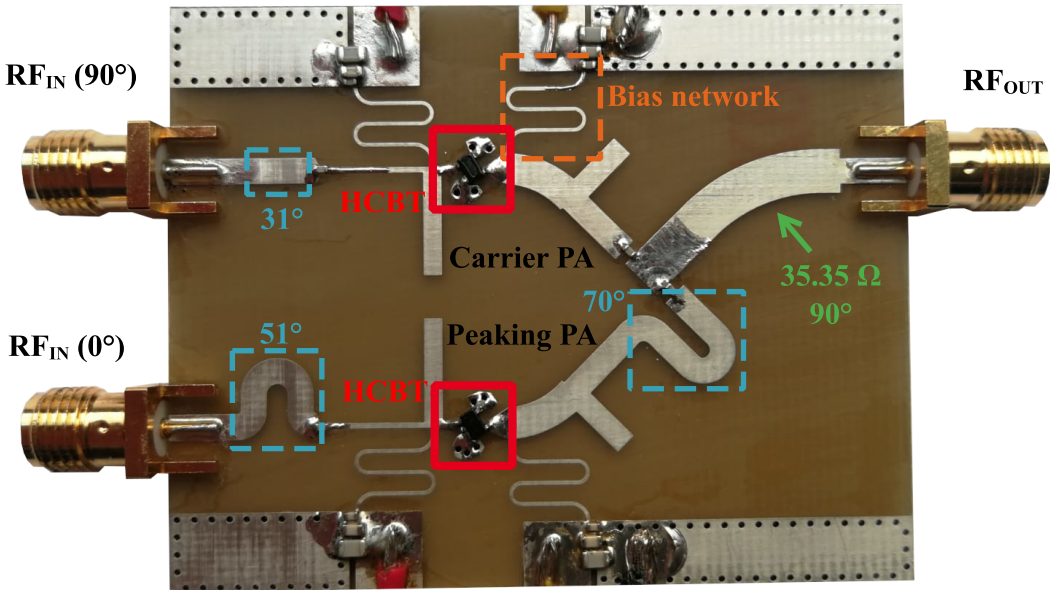
To enable the impedance transformation, the system impedance of 50 *Omega* is transformed to 25 Ω by employing a quarter-wave transformer with $Z_0 = \sqrt{Z_{\text{in}} Z_{\text{out}}} = 35.35\ \Omega$. The performance of the network is also important since a broadband load of 25 Ω is mandatory in this design to enable a proper active load modulation of the main amplifier. The $25 +/- 10\%\ \Omega$ input impedance is maintained over the bandwidth of close to 1 GHz, as shown in Fig. 4.10b. Thus, this confirms the fact that the bandwidth of the peaking output matching network is a bottleneck which limits the frequency performance of the Doherty PA. Similary to the layout of the phase shift lines, the quarter-wave transformer is made with a curvature to enable a symmetrical connection to the output matching networks of the main and peaking PA through the DC blocking capacitors.

4.4 Implementation

The schematic of the Doherty PA is shown in Fig. 4.11a, whereas the implemented amplifier is shown in Fig. 4.11b. Two emitter pins of the transistors of main and peaking PAs are grounded using plated-through vias. Matching networks, bias networks, and phase shift lines, are designed in microstrip transmission line technology and the performance is optimized using electromagnetic simulator using the parameters of the FR4 substrate. Bias networks are implemented using quarter-wave lines at the base and collector along with 13-pF capacitors providing RF short at 2.4 GHz. Coupling capacitors, employed at the input and at the combining point, are used at their series resonant frequency to ensure the lowest possible impedance at the operating frequency. Base and collector bias connections of the main and peaking PAs are separated



(a)



(b)

Figure 4.11: (a) Schematic and (b) fabricated Doherty PA using HCBTs as active devices. Input power is split using hybrid coupler with 90° phase difference. Input delay lines bring signals in the main and peaking branches in-phase at the combining point. Input and output matching networks, IMN and OMN, are the same for the two amplifiers. Bias networks are implemented using quarter-wave microstrip transmission lines terminated by 13-pF capacitors which provide short at 2.4 GHz. Additional capacitors, larger in value, are also used for bypassing the lower frequencies.

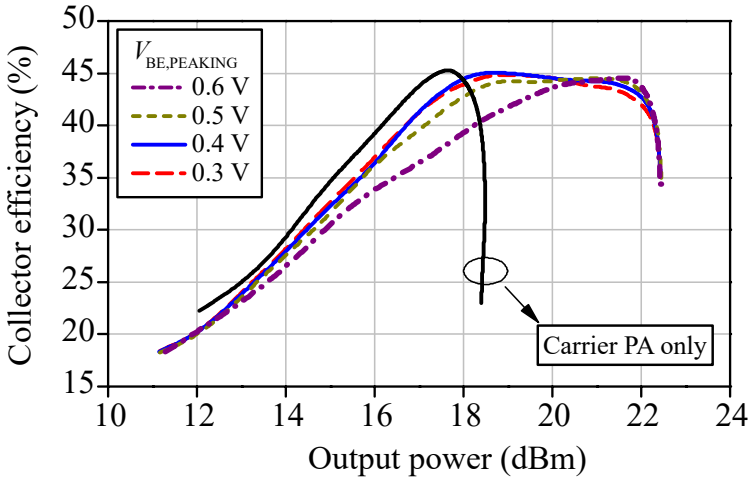


Figure 4.12: Measured collector efficiency as a function of output power of the fabricated Doherty PA. Collector efficiency is measured for different base voltages of the peaking PA, wherein $V_{BE,PEAKING}$ provides the best overall performance, exhibiting a flat efficiency characteristic over 4-dB output power back-off.

to enable performance optimization by varying the bias of the peaking PA during testing and on-board optimization.

4.5 Measurement results

From the previous analysis, the expected output power at the maximum input drive is 22.5 dBm, since both PAs provide 19.5 dBm at their outputs, with collector efficiency of 46%. At 6-dB output power back-off, expected output power is 16.5 dBm with collector efficiency of 42%. Collector efficiency as a function of output power is shown in Fig. 4.12. The amplifier provides maximum efficiency of up to 46%. By varying the base bias of the peaking PA, $V_{BE,PEAKING}$, the efficiency at full output power can be optimized. The optimum is found for $V_{BE,PEAKING} = 0.4$ V, wherein the maximum efficiency range extends from 18 dBm up to 22 dBm. Therefore, the PA is suitable for signals of peak to average power ratio of around 4 dB, whereas a 6 dB back-off was envisioned during the design. The difference arises mainly due to the bias dependent phase characteristic of the peaking PA. Since the design was carried out for Class-C bias of $V_{BE,PEAKING} = 0$ V, the length of the output phase shift line of peaking PA, shown in Fig. 4.7, should be optimized so that the output impedance achieves maximum for $V_{BE,PEAKING} = 0.4$ V, at the 6-dB output power back-off. On the other hand, a flat efficiency characteristic is achieved, with up to 45% collector efficiency over the 4-dB OPBO.

Since the optimum input and output impedances of the HCBT devices are close to 50 Ω, a wideband design is achievable, employing simple microstrip matching networks. The frequency dependence of the collector efficiency and output power at 4-dB OPBO is shown in Fig. 4.13. The collector efficiency is maintained above 41.5% over the bandwidth of 100 MHz. Achieved

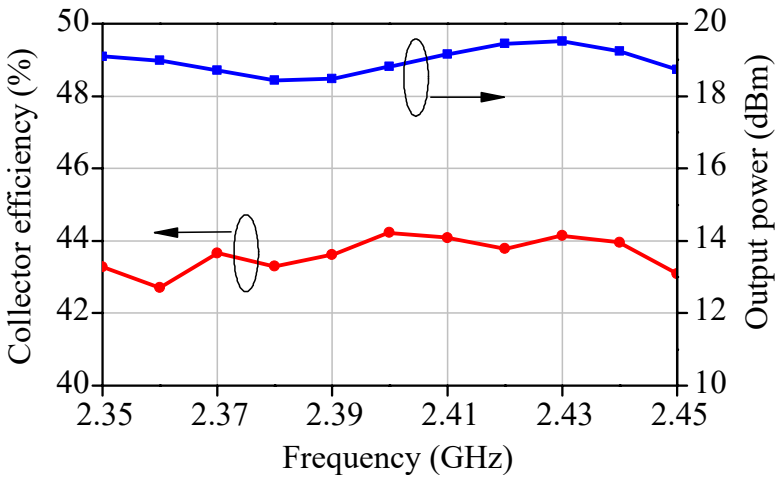


Figure 4.13: Measured collector efficiency and output power at 4-dB output power back-off as a function of frequency of the Doherty PA for $V_{\mathrm{BE,PEAKING}} = 0.4$ V.

output power equals 19 dBm $+/-$ 1.5 dB over the entire bandwidth. The amplifier is tested by applying a 5-MHz-wide, WCDMA modulated signal with a 3.5-dB PAPR. For output power of 16.5 dBm, the collector efficiency of 38.7% is achieved. The performance is comparable with state-of-the-art handset PAs [108].

The Doherty power amplifier exhibits flat efficiency characteristics in the 4-dB output power back-off range. Furthermore, the bandwidth of maximum collector efficiency is close to 100 MHz, which is the direct consequence of the optimal matching impedances in the vicinity of 50 Ω. In effect, this enables the employment of the amplifier for wideband OFDM signals with a peak to average power ratio of around 4 dB, where the efficiency is the most important parameter.

Chapter 5

Balanced power amplifier

The optimal characteristics of a power amplifier, such as efficiency and linearity, are usually maintained in narrow frequency bands, hence the need for a separate amplifier for each wireless standard in a handheld device. The bandwidth can be increased by employing configurations of multiple single-stage power amplifiers, such as balanced PA, which exhibit excellent input and output return loss [14, 15]. A balanced PA consists of two power amplifiers connected in parallel, doubling the output power of a single-stage PA.

5.1 Bandwidth and return loss

The motivation for the balanced PA is to achieve wide bandwidth and high input and output return loss in the passband. The latter is the main difference between the balanced PA and other techniques to achieve wide bandwidth, e.g. matching networks of higher order or gain shaping. The input and output of the balanced power amplifier are buffered by the hybrid couplers, wherein the return loss is determined by the characteristics of the coupler, and not the separate amplifiers in the balanced configuration.

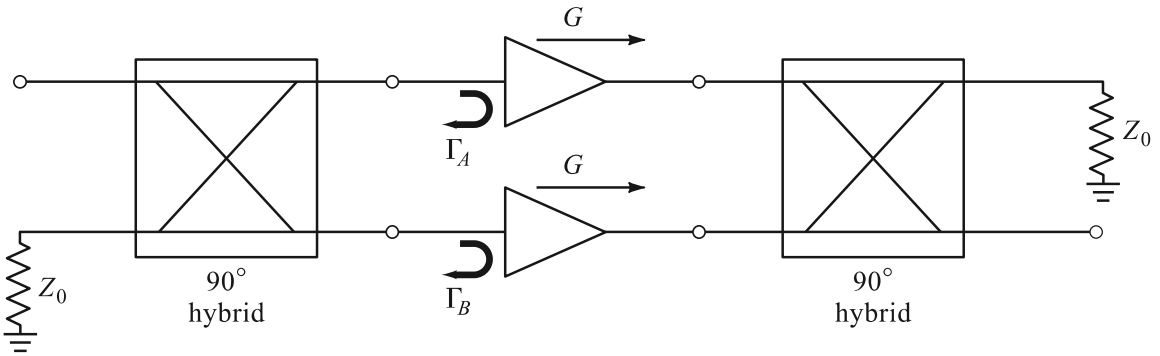


Figure 5.1: Block diagram of a balanced power amplifier. The upper amplifier has gain and input reflection coefficient of G_A and Γ_A, whereas the lower one has gain and input reflection coefficient of G_B and Γ_B.

To split the input signal and combine the output signals, a 3-dB coupler with 90° phase shift between the through and coupled ports is used [14]. As a result, the reflected waves at the input and output of each PA in the balanced configuration are cancelled by the input and output coupler, respectively. Thus, input and output return losses can be high even if PAs present high reflection coefficients to the couplers. Therefore, the bandwidth of the balanced amplifier is mainly determined by the characteristics of the input and output coupler. Additionally, the reliability is increased, since the balanced PA continues to operate with limited performance, caused by a change in load impedance due to the failure of one of the amplifiers. In contrast to a Doherty PA, the outputs of the two amplifiers are connected through coupler, as is the case for the input, therefore, the outputs are isolated from each other and there is no load modulation.

With reference to Fig. 5.1, it can be shown that the gain of a balanced power amplifier is given by [14]

$$S_{21} = \frac{-j}{2}\left(G_{\mathrm{A}} + G_{\mathrm{B}}\right), \tag{5.1}$$

where G_{A} and G_{B} are the voltage gains of the upper and lower PAs shown in Fig. 5.1. Thus, the overall gain of the balanced configuration is the average of the voltage gains of the separate amplifiers. Similarly, the input reflection coefficient is given by

$$S_{11} = \frac{1}{2}\left(\Gamma_{\mathrm{A}} - \Gamma_{\mathrm{B}}\right), \tag{5.2}$$

which is ideal and equal to 0 for $\Gamma_{\mathrm{A}} = \Gamma_{\mathrm{B}}$. In other words, if the two amplifiers are made equal, which means that

$$\Gamma_{\mathrm{A}} = \Gamma_{\mathrm{B}} \tag{5.3}$$

and

$$G_{\mathrm{A}} = G_{\mathrm{B}}, \tag{5.4}$$

then the input reflection coefficient of the balanced configuration S_{11} is 0, whereas the gain is equal to the gain of the individual amplifier. Additionally, if one amplifier fails, the gain drops four times, since there is a decrease because of $G_{\mathrm{A||B}} = 0$ dB and $S_{11} \neq 0$.

5.2 Branchline coupler

For the balanced PA design, a hybrid coupler is used implemented employing transmission lines, usually termed branchline coupler [14]. It is a four-port device with the ideal characteristics

defined by

$$\mathbf{S}_{\mathrm{bc}} = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{5.5}$$

where $\mathbf{S}_{\mathrm{bc}}$ is the S-matrix of a branchline coupler. Thus, the input signal is fed to the port 1, the output signals are taken at the ports 2 and 3, wherein the phase difference between the signals at ports 2 and 3 is 90°. The input power is equally split between the ports 2 and 3 with no power coupled to port 4. Additionally, the coupler is symmetrical, i.e., the input signal can be fed to any port with the corresponding change in the coupled and isolated ports. Namely, the isolated port is always the one at the same side as the input port.

5.2.1 Double-box branchline coupler

In its basic form, a branchline coupler consists of four transmission lines and exhibits high return loss at the design frequency, but it is very narrowband [14]. Therefore, a balanced amplifier utilizing such a coupler would also be narrowband. To increase the bandwidth of the amplifier, a double-box branchline coupler [109] is employed for the signal splitting and combining in the balanced power amplifier. The schematic of the a double-box branchline coupler is shown in Fig. 5.2. The coupler also has four ports, with port 1 being the input port, port 2 the through port, port 3 the coupled port, and port 4 the isolated port, but the double-box has three more transmission lines when compared to the classical branchline coupler. The Z_3 line has the lowest characteristics impedance, whereas the outer two, of characteristic impedance Z_2, have the highest. The design equations for the coupler are given by

$$Z_2 = \left(1+\sqrt{2}\right) Z_1, \tag{5.6}$$

$$Z_3 = Z_1\sqrt{2}, \tag{5.7}$$

where Z_{n} are characteristic impedances of the transmission lines from Fig. 5.2. Therefore, characteristic impedance Z_1 is a design parameter which defines characteristic impedances Z_2 and Z_3 according to (5.6) and (5.7), respectively.

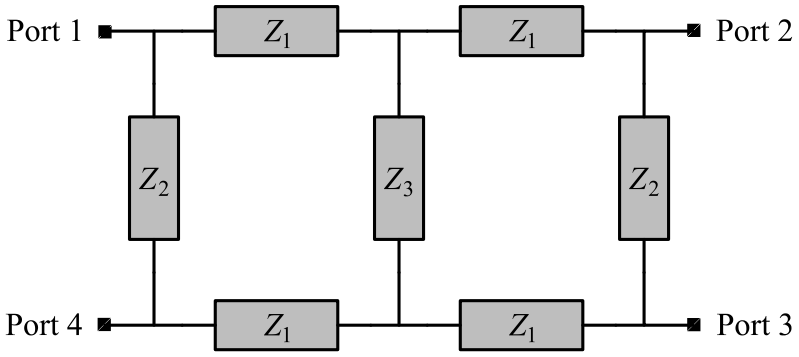


Figure 5.2: Schematic of a double-box branchline hybrid coupler.

5.2.2 Microstrip branchline coupler design

A double-box branchline coupler is designed at the center frequency of 2.4 GHz employing microstrip transmission lines [110]. According to (5.6) and (5.7), selecting the default value of 50 Ω for Z_1, sets the Z_2 to 120.7 Ω and Z_3 to 70.7 Ω. Microstrip transmission lines of such a high characteristic impedance are very narrow, considering the substrate used for the design. Both coupler and amplifier are fabricated on a low-cost 1-mm-thick FR-4 laminate, which has dielectric constant ε_r and loss tangent $\tan\delta$, of 4.3 and 0.02, respectively. When implemented on this laminate, the 120.7 Ω microstrip line has a relatively small width of around 9 mil, which can result in large variations of the characteristic impedances of the two Z_2 lines when fabricated. To increase the width of the high impedance Z_2 lines, a lower value of Z_1 is thus needed.

The optimal width of the Z_1 transmission line and the overall functionality of the coupler are arrived at by simulations employing ideal transmission lines and microstrip line models, which use the parameters of the substrate. The performance of the coupler is then optimized using electromagnetic finite element method (FEM) simulations. The final layout of the coupler is shown in Fig. 5.3a. The optimization give $Z_1 = 38$ Ω, the value which further increases the bandwidth of the double-box branchline coupler and, at the same time, relaxes the width constraint of the high impedance lines. At each port, a 50-Ω line ($w_1 = 76$ mil, $l_1 = 200$ mil) is added to enable the interface with coaxial connectors. The coupler is optimized by tweaking the widths of the Z_2 and Z_3 lines to achieve the highest return loss with equal 3-dB power split between through and coupled ports. The best performance is achieved for $w_3 = 13.9$ mil and $w_4 = 93.3$ mil. The width of the Z_3 line of 13.9 mil is now larger than the minimum line thickness specified by the board manufacturer of 10 mil. Therefore, the characteristic impedance is not highly dependent on the quality of the implementation as would be the case for the width of 9 mil.

Measurements are compared with the electromagnetic simulations in Fig. 5.3b-d. The *S*-parameters of the coupler are measured by using a two-port vector network analyzer (VNA),

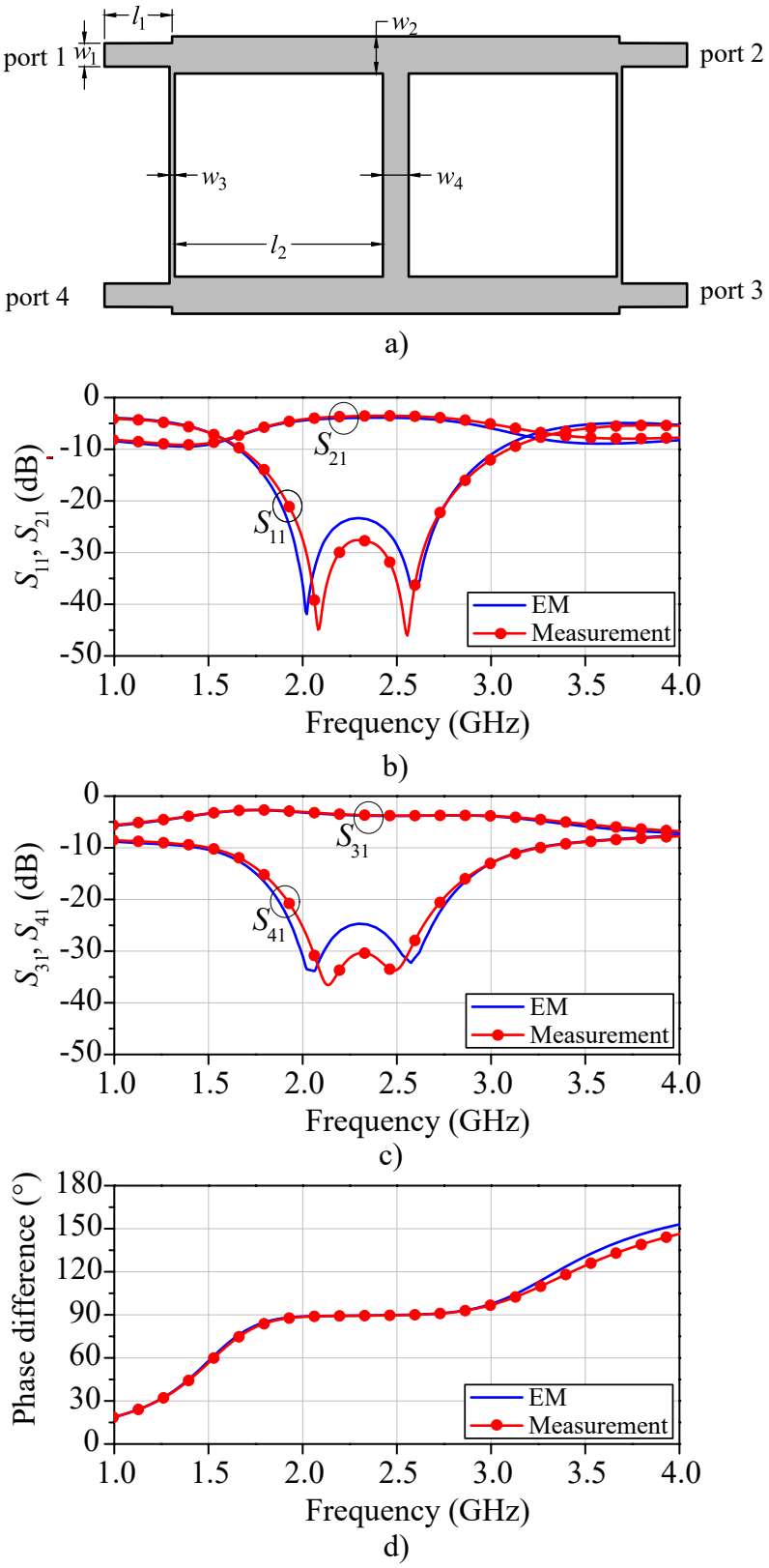


Figure 5.3: (a) Layout of the double-box branchline coupler designed using microstrip transmission lines on the FR4 substrate with $\varepsilon_r = 4.3$ and $\tan\delta = 0.02$. The center frequency is 2.4 GHz. Width and lengths of the lines are: $w_1 = 76$ mil; $w_2 = 117.4$ mil; $w_3 = 13.9$ mil; $w_4 = 93.3$ mil; $l_1 = 200$ mil; and $l_2 = 678.6$ mil. Measured and EM simulated (b) S_{11} and S_{21}, (c) S_{31} and S_{41}, and (d) phase difference between the port 2 and 3, $\angle S_{21} - \angle S_{31}$, over the frequency range from 1 GHz to 4 GHz.

thus, the two ports not being measured are terminated by 50 Ω. At 2.4 GHz, measured S_{11}, S_{21}, S_{31}, and S_{41}, are -28.2 dB, -3.52 dB, -3.73 dB, and -31.7 dB, respectively, whereas the phase difference between the through port 2 and coupled port 3 is 89.55°. Input return loss, $R_{\mathrm{L}} = -20\log(|S_{11}|)$ dB, is higher than 20 dB in the 800-MHz bandwidth from 1.9 GHz to 2.7 GHz. Amplitude imbalance of port 2 and 3 is $+/-0.6$ dB and $+/-0.45$ dB, respectively, whereas the phase imbalance is $+/-3.4°$. Overall, the coupler exhibits high input return loss around 2.4 GHz and small amplitude and phase imbalance over the bandwidth of 800 MHz.

5.3 Optimal matching impedances

In order to achieve maximum output power and maximum available gain from the HCBT devices employed in the design, the transistors in both amplifiers of the balanced configuration are matched for maximum output power and maximum gain at the output and input, respectively. To that end, large-signal input and output impedances are found using the calibrated load-pull setup employing automated mechanical impedance tuners. The HCBTs used for the design of the balanced power amplifier are of the emitter area $A_{\mathrm{E}} = 31.2\ \mu\mathrm{m}^2$. The devices have open-base breakdown voltage $\mathrm{BV_{CEO}}$ of 3.2 V.

Firstly, the bias is defined for both amplifiers based on their respective output DC characteristics and maximum voltage and current ratings. The DC measurements and measured load-pull data for the HCBTs used in the current design are shown in Chapter 2. The results also present the comparison of the performance of the HCBT in three different classes of PA operation, namely, Class-A, Class-AB, and Class-B. The best performance is achieved in Class-AB with $I_{\mathrm{C}} = 20$ mA and $V_{\mathrm{CE}} = 2.87$ V, wherein output power, collector efficiency, and gain in 1-dB compression point, are 18.6 dBm, 46%, and 10 dB, respectively [82]. Thus, both PAs of the balanced configuration are biased by the DC collector-emitter voltage of 2.87 V. Since the device is reliably operated at even higher collector current of 50 mA, the HCBTs in the balanced PA are biased at $I_{\mathrm{C}} = 50$ mA to achieve maximum output power available from the device. Once the bias is defined, load-pull and source-pull are performed to find the optimal input and output impedances at the fundamental frequency of 2.4 GHz, which are

$$Z_{\mathrm{S}} = 39.9 + j7.7\ \Omega, \tag{5.8}$$

$$Z_{\mathrm{L}} = 32.4 - j8.2\ \Omega, \tag{5.9}$$

where Z_{S} and Z_{L} are the optimal input and output matching impedances, respectively. The reflection coefficients associated with the impedances from (5.8) and (5.9) are 0.14 and 0.24,

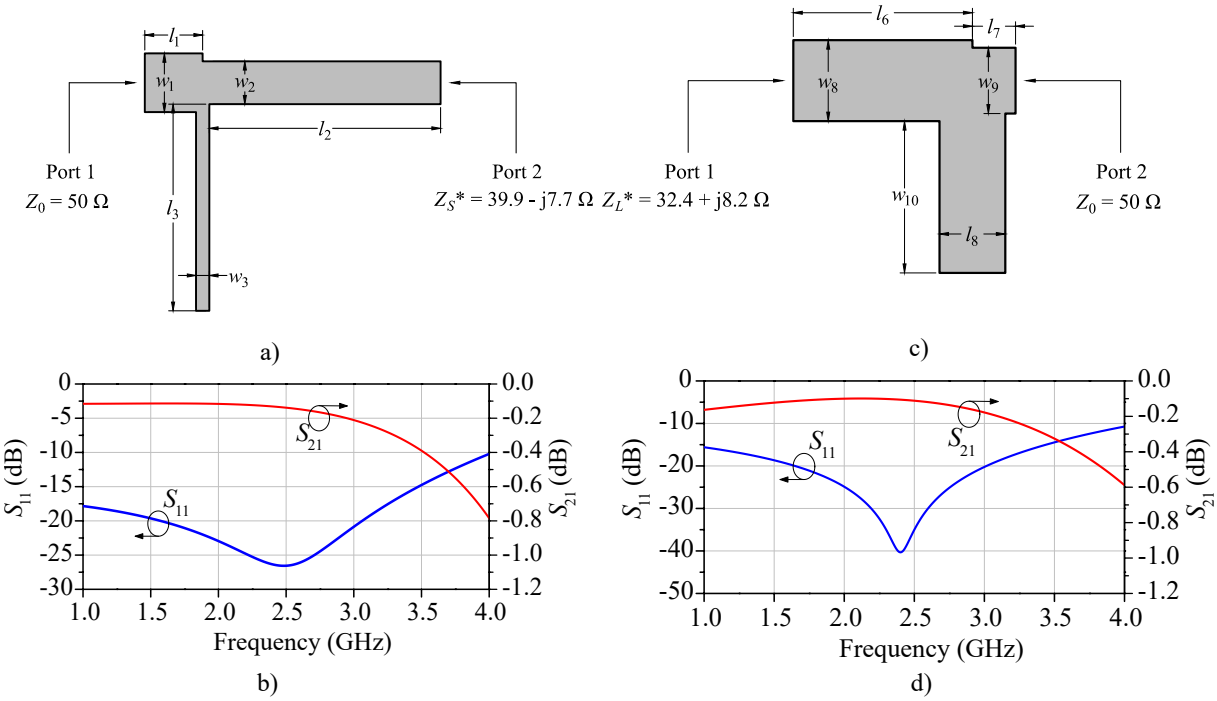


Figure 5.4: (a) Input matching network layout. Widths and lengths of the lines are: $w_1 = 76$ mil; $l_1 = 75$ mil; $w_2 = 55.4$ mil; $l_2 = 299$ mil; $w_3 = 17.16$ mil; and $l_3 = 267$ mil, and (b) simulated S_{11} and S_{21} of the input matching network. (c) Output matching network layout. Widths and lengths of the lines are: $l_6 = 208$ mil; $l_7 = 50$ mil; $l_8 = 76.3$ mil; $w_9 = 76$ mil; and $w_10 = 176$ mil, and (d) simulated S_{11} and S_{21} of the output matching network.

respectively. Therefore, the impedances are close to the center of a Smith chart, i.e. system impedance of 50 Ω. This enables a wideband match employing simple reactive two-element matching networks.

5.4 Input and output matching networks

Input matching network (IMN) and output matching network (OMN) are designed employing microstrip transmission lines utilizing open-circuited shunt stubs and series stubs. Both networks are optimized first using ideal transmission lines and the performance is then fine-tuned in the electromagnetic simulator. The networks are the same for both PAs in the balanced configuration.

The layout of the input matching network is shown in Fig. 5.4a. The network comprises a 100-Ω open-circuited shunt stub (w_3, l_3) followed by a 60-Ω series stub (w_2, l_2). The signal is fed from port 2 or 3 of the input hybrid coupler to port 1 of the IMN over a small trace of 50-Ω line (w_1, l_1) which is used to place the input decoupling capacitor on the board. The EM simulation results for the IMN are shown in Fig. 5.4b for port 2 impedance defined as a complex-conjugate of Z_S. Since the optimum input impedance of the used HCBT is very close to 50 Ω, a wideband match is achieved with return loss higher than 20 dB in the frequency

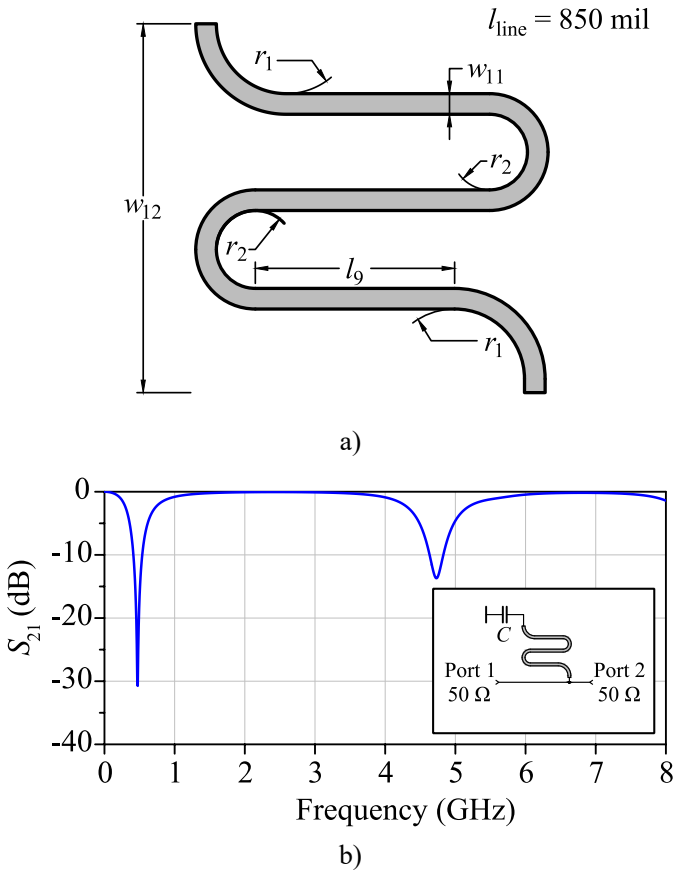


Figure 5.5: (a) Bias network layout. Widths, lengths, and radii of the lines are: w_{11} = 13 mil; l_9 = 146 mil; w_{12} = 230 mil; r_1 = 68 mil; and r_2 = 49 mil, and (b) simulated S_{21}. The inset shows the simulation configuration.

range from 1.6 GHz to 3 GHz. The insertion loss is 0.1 dB at 2.4 GHz and increases to 0.2 dB at 3 GHz.

The layout of the OMN is shown in Fig. 5.4c. The network comprises a 44-Ω series stub (w_8, l_6) followed by a 60-Ω open-circuited shunt stub (w_{10}, l_8). The EM simulation results for the OMN are shown in Fig. 5.4d for port 1 impedance defined as a complex-conjugate of Z_L. Return loss is higher than 20 dB in the frequency range from 1.65 GHz to 3 GHz. In the frequency range from 1.6 GHz to 3 GHz insertion loss is lower than 0.2 dB.

5.5 Bias network

The bias network should present high impedance to the input and output of the transistor over the bandwidth of the amplifier, while incurring minimal loss at DC. Both the base and collector bias are implemented employing a short-circuited quarter-wavelength ($\lambda/4$) transmission line. Ideal $\lambda/4$ transmission line provides infinite impedance at the fundamental frequency and short circuit at even harmonics [14]. Therefore, the bias microstrip line is designed at the center frequency of 2.4 GHz. Firstly, the characteristic impedance of the line is selected to be as high

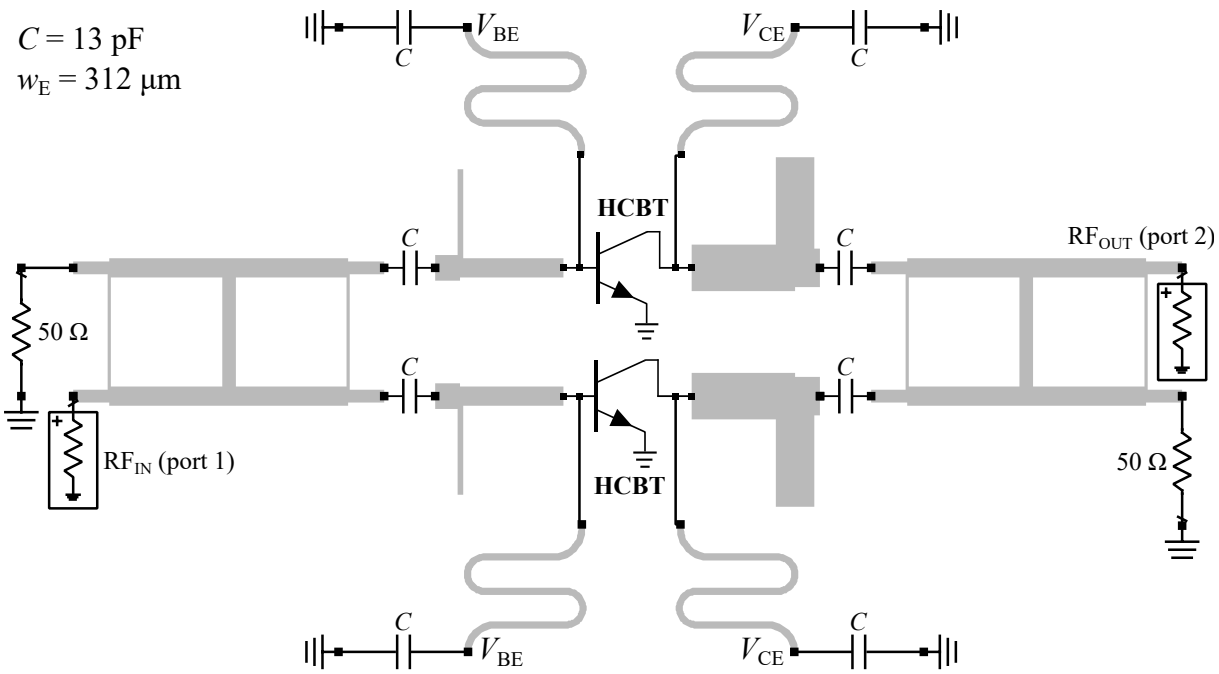


Figure 5.6: Schematic of the balanced power amplifier for the EM co-simulation with the small-signal model of the HCBT and discrete capacitors. The capacitor dimension (0402) is chosen such that its series resonance occurs at the fundamental frequency of 2.4 GHz.

as possible, since the bandwidth of the $\lambda/4$ microstrip line is larger for higher characteristic impedance at the fundamental frequency. The impedance chosen is 110 Ω, setting the width of the line at 13 mil. The length of such $\lambda/4$ microstrip line turns out to be 720 mil for the used substrate. To achieve more compact layout, the line is meandered, and the final layout is optimized using EM simulations, as shown in Fig. 5.5a. The line is 850-mil long, but the length of the layout (w_{12}) is reduced to 230 mil. The results of the EM simulation are shown in Fig. 5.5b, wherein the bias line is simulated in shunt configuration (shown in the inset). The capacitor $C = 10$ pF is utilized near the self-resonant frequency to provide low impedance at 2.4 GHz. From 1.6 GHz to 3 GHz, S_{21} is higher than -0.17 dB and equals -0.05 dB at 2.4 GHz. The minimum at 470 MHz is caused by the resonance of the equivalent inductance of the bias line of 11 nH, and the 10-pF capacitor.

5.6 Small-signal simulations

The balanced amplifier is simulated by incorporating the networks in the simulation environment together with the discrete capacitors needed for the supply bypass and DC blocking. The schematic of the amplifier is shown in Fig. 5.6. The HCBT model is a small-signal model extracted from *S*-parameter measurements. The bias is applied through the meandered quarter-wave line at both base and collector pins. The capacitor is chosen such that it exhibits a series resonant frequency at the fundamental frequency of 2.4 GHz, thus providing a low impedance

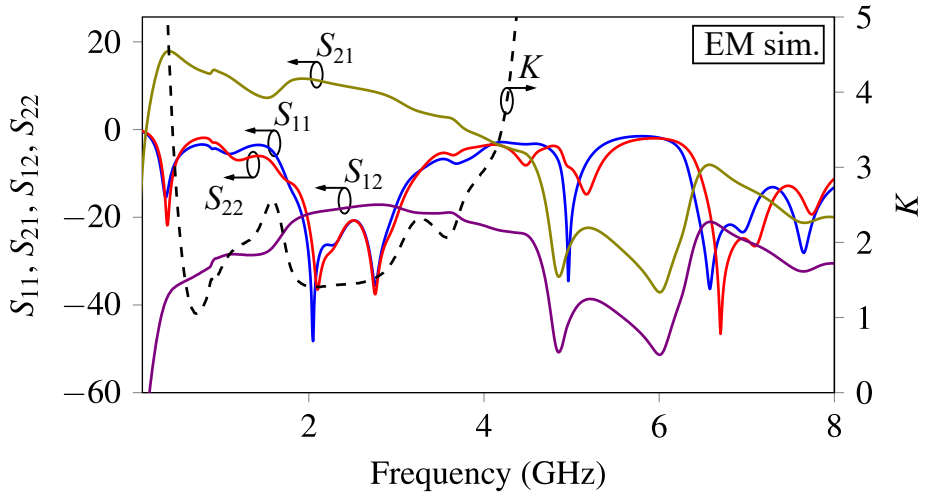


Figure 5.7: Simulated small-signal performance of the balanced HCBT PA. The distributed elements are EM-simulated, whereas the small-signal models of the discrete capacitors are taken from the manufacturer's measured data. The bias point of the HCBTs is $(I_{CQ}, V_{CEQ}) = (50\text{ mA}, 2.87\text{ V})$

at f_0 of around 2 Ω. Since the couplers at the input and output are symmetrical components, the PA can be driven at either of the ports on the input, wherein the unused port is terminated by 50 Ω. If the upper port on the left is used as an input, the output is taken at lower port on the right [see Fig. 5.6].

The input reflection coefficient S_{11}, output reflection coefficient S_{22}, forward transmission coefficient S_{21}, and reverse transmission coefficient S_{12}, are simulated by employing EM simulations for the distributed components along with the S-parameter simulations for the discrete capacitors [see Fig. 5.7]. The Rollet's stability factor K is greater than one for all frequencies, whereas it is the lowest and equal to 1.06 at 700 MHz. Both input and output reflection coefficients S_{11} and S_{22}, respectively, are lower than 20 dB from just below 2 GHz up to 3 GHz. The amplifier exhibits small-signal gain of around 10 dB over the bandwidth of around 1 GHz, with small ripple of $+/-0.5$ dB. Additionally, the reverse transmission coefficient is lower than -20 dB over the frequency span from DC to 8 GHz.

5.7 Schematic and fabricated amplifier

The schematic and final printed circuit board of the balanced PA designed using HCBT are shown in Fig. 5.8. The amplifier uses two previously designed double-box branchline couplers for power splitting and combining. Input signal is applied at port 4 of the input coupler and the output signal is taken at the port 2 of the output coupler. Unused port 1 of the input coupler and port 3 of the output coupler are terminated by coaxial 50 Ω, as shown in Fig. 5.8b. Both emitter pins are grounded by employing multiple plated through-hole vias to lower the inductance in the emitter so as not to incur additional degeneration. The capacitor used to provide RF short for the proper operation of $\lambda/4$ short-circuited stub does not provide bypass for low

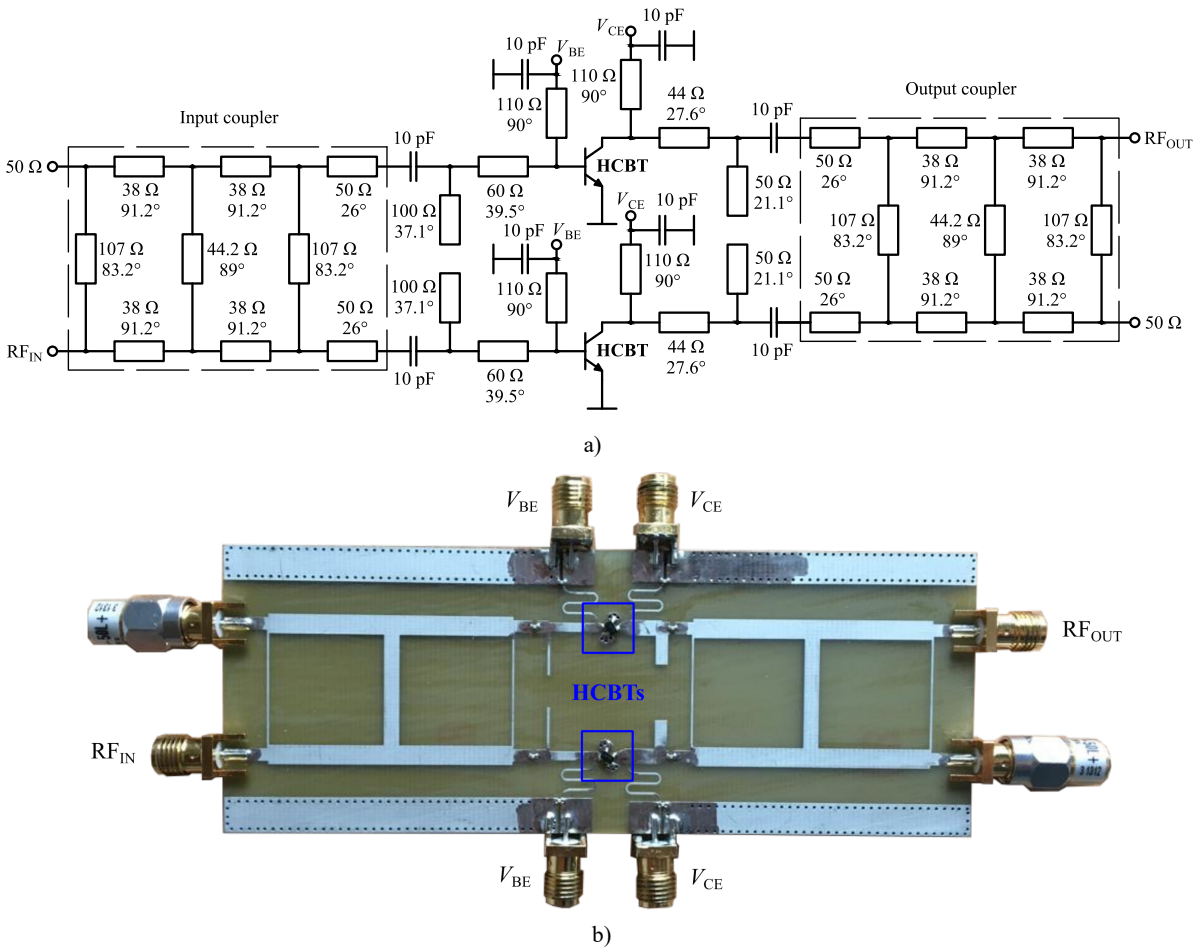


Figure 5.8: Balanced PA (a) schematic and (b) final fabricated PCB. The coaxial SMA connectors are soldered at all four RF ports and four bias ports. Unused RF ports are terminated by 50 Ω.

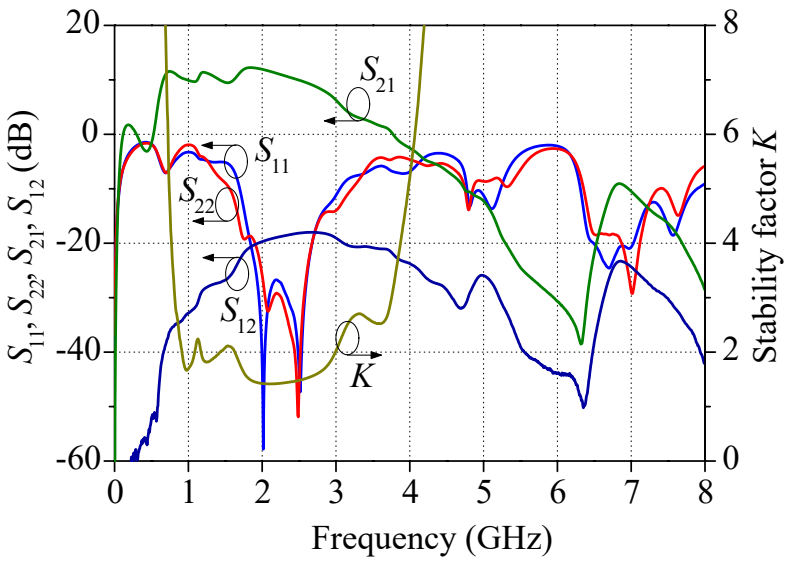


Figure 5.9: Measured *S*-parameters of the balanced PA in the frequency range from 300 kHz to 8 GHz.

frequency components, which can cause instabilities since the transistors have high gain at low frequencies. To ensure that the low frequency components do not cause instabilities, both base and collector bias is applied through wideband coaxial bias tees, which exhibit passband in the range from 200 kHz to 12 GHz. In this way, the bias tee provides a 50 Ω termination for the low-frequency components thus enhancing the stability of the PA. The operation in the passband, i.e. around 2.4 GHz, is not disturbed by adding the bias tees since the $\lambda/4$ line presents an open circuit to those frequencies, as shown in Fig. 5.5b.

5.8 Measurement results

5.8.1 Small-signal performance

Measured *S*-parameters of the balanced PA are shown in Fig. 5.9. At 2.4 GHz, the PA exhibits small-signal gain S_{21} of 10.5 dB with high input and output return loss of 30.6 dB and 37 dB, respectively. Reverse isolation is higher than 18.7 dB up to 8 GHz. The bandwidth of the PA is mainly limited by the bandwidth of the couplers, thus, the PA exhibits 800 MHz bandwidth since the input and output return losses are higher than 20 dB in the frequency range from 1.9 GHz to 2.7 GHz. In the band, the small-signal gain is higher than 9 dB. Also shown in the figure is the stability factor K which is higher than 1 in the entire frequency range from DC to 8 GHz.

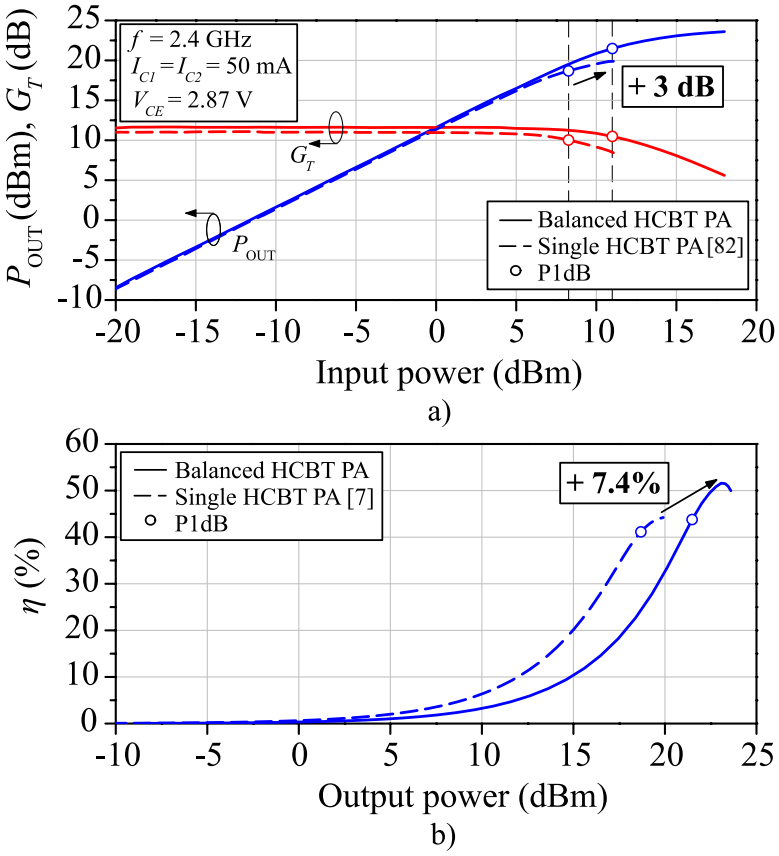


Figure 5.10: Measured a) output power P_{OUT} in P1dB, transducer gain G_{T}, and b) collector efficiency η for $I_{\mathrm{C1}} = I_{\mathrm{C2}} = 50$ mA and $V_{\mathrm{CE}} = 2.87$ V at 2.4 GHz. Measurements are compared to the performance a single device.

5.8.2 Large-signal performance

The large-signal performance of the PA at 2.4 GHz is shown in Fig. 5.10. In 1-dB compression point (P1dB), the output power P_{OUT} and transducer gain G_{T} are 21.5 dBm and 10.6 dB, respectively, which is an increase in output power of 2.8 dB compared to a single amplifier [82]. Collector efficiency is 44% in P1dB and reaches maximum of 52% at the output power of 23.1 dBm, which is an increase of 7.4% compared to a single amplifier. Since the output power of the balanced PA is twice the output power of the single HCBT, balanced PA has efficiency peak at around 3-dB higher output power.

Frequency dependence of large-signal parameters is shown in Fig. 5.11. In the frequency range from 1.8 GHz to 2.5 GHz, output power and gain are $21.4 +/- 0.18$ dBm and $10.4 +/- 0.15$ dB, respectively, with minimum collector efficiency of 36% at 2.1 GHz which increases to 45% at 2.3 GHz. Since the PA is designed at the center frequency of 2.4 GHz, the best performance is achieved around 2.4 GHz whereas the characteristics deteriorate outside the passband due to bandwidth limitation of the input and output couplers.

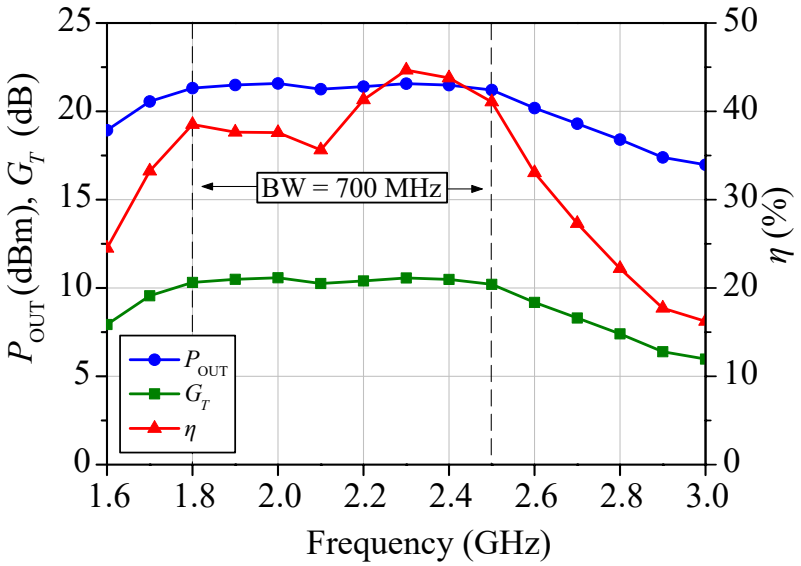


Figure 5.11: Measured output power P_{OUT}, transducer gain G_{T}, and collector efficiency η, for $I_{\mathrm{C}} = 50$ mA and $V_{\mathrm{CE}} = 2.87$ V in the frequency range from 1.6 GHz to 3 GHz.

Graceful degradation

In case one of the PAs in a balanced configuration fails, the amplifier retains acceptable performance. More precisely, the gain of the balanced PA becomes 6 dB lower in case one PA fails [15]. In order to verify this behaviour, the performance of the HCBT balanced PA with one stage turned off is simulated and then the same condition is measured. The failed condition is achieved by turning off the bias of one amplifier and biasing the other so that only one is active at the time. The measured small-signal and large-signal performance are shown in Fig. 5.12. As expected, S_{21} decreased for around 5.5 dB in the frequency range from 1.8 GHz to 2.5 GHz, as shown in Fig. 5.12a. Input return loss decreased to around 10 dB since the turned-off PA presents high impedance to the input coupler. Output power and gain also decreased by 5.5 dB over the entire input power range [see Fig. 5.12b]. Collector efficiency curve resembles the characteristics of a single-transistor PA shown in Fig. 5.10b, but since the half of the input power is now reflected back to the couplers and dissipated in the 50-Ω load, the efficiency is much lower. Nevertheless, with one stage turned off, HCBT balanced PA maintains functionality with 6 dB lower gain and output power, but with higher efficiency at lower output powers.

The small-signal performance in graceful degradation is simulated and the results are shown in Fig. 5.13. The small-signal gain drops to around 4.5 dB in the band, whereas both input and output return losses decreases to around 6 dB and 10 dB, respectively, at 2.4 GHz. Due to this decrease, the reverse transmission is even lower in this case, which increases the stability of the amplifier, which can be seen from the plot of K factor. Thus, the balanced configuration provides additional reliability margin which is not present in most of the other advanced PA architectures.

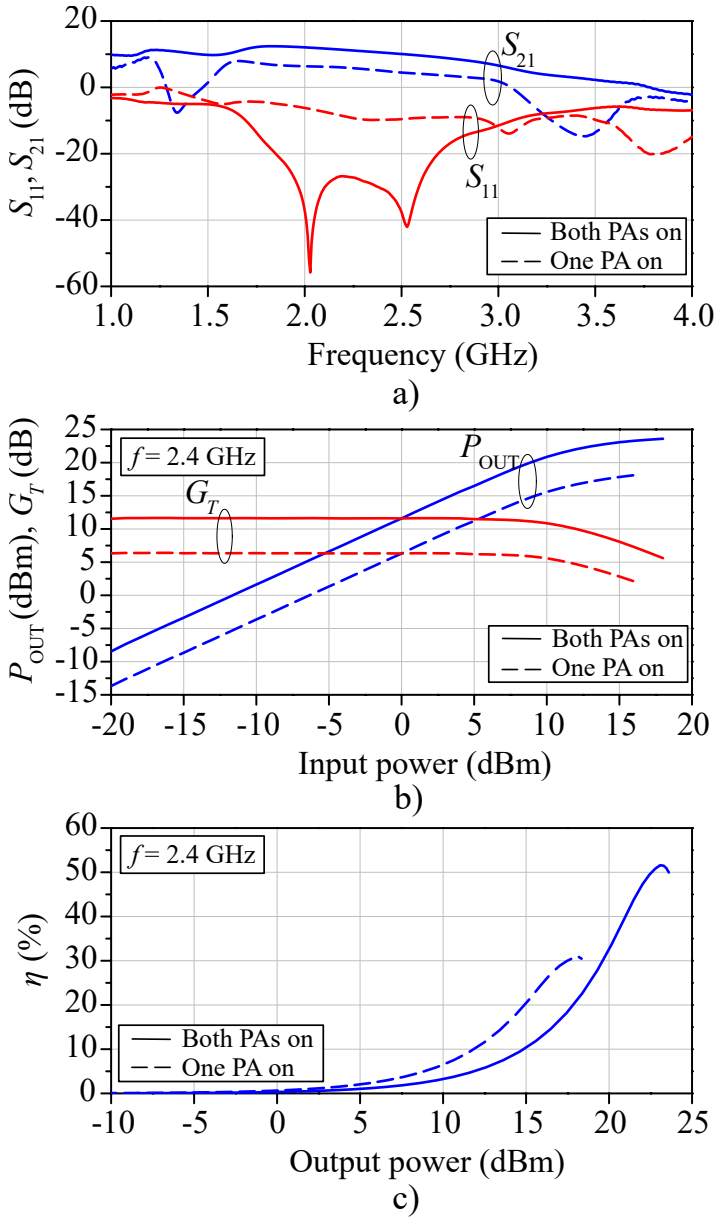


Figure 5.12: Measured performance of the balanced PA with one stage turned off to emulate the graceful degradation. a) S_{11} and S_{21}, b) output power P_{OUT}, and transducer gain G_{T}, and c) collector efficiency η, for $I_{\mathrm{C1}} = I_{\mathrm{C2}} = 50$ mA and $V_{\mathrm{CE}} = 2.87$ V.

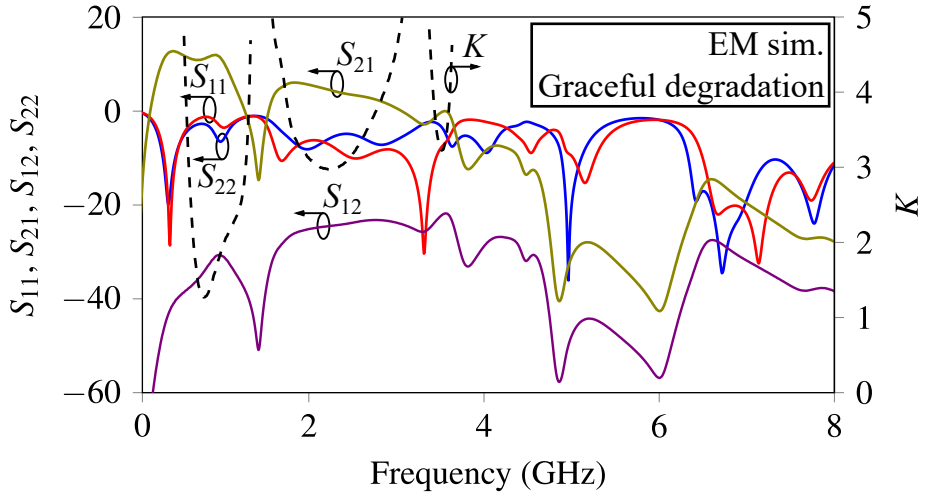


Figure 5.13: Simulated small-signal performance of the balanced PA with one stage turned off to emulate the graceful degradation. The bias point of the HCBTs is $(I_{CQ}, V_{CEQ}) = (50\text{ mA}, 2.87\text{ V})$.

5.9 Comparison with state-of-the-art

The performance of the balanced PA is compared in Tab.5.1 to the performance of the amplifiers implemented in advanced transistor technologies. Even though HCBT PA operates with a relatively lower output power, it achieves minimum collector efficiency of 35.6% with input and output return loss higher than 20 dB, while achieving similar bandwidth.

Table 5.1: Performance of power amplifiers implemented in advanced semiconductor technologies with respect to HCBT balanced power amplifier.

Ref.	[111]	[112]	HCBT balanced PA
Bandwidth (GHz)	1-8 - 2.8	1.8 - 2.4	1.8 - 2.5
P1dB (dBm)	28	27.2	21.4
η, PAE (%)	7.5 (PAE)	28 (η)	>35.6 (η)
Input and output RL (dB)	10	<15	>20
Technology	GaAs HBT	CMOS SOS	HCBT

The balanced PA is designed at the frequency of 2.4 GHz using HCBT. The design is based on measured load-pull data of the HCBTs employed, whereas the matching and bias networks are designed in microstrip technology on an FR4 substrate. The HCBT balanced PA provides $21.4 +/- 0.18$ dBm of output power and $10.4 +/- 0.15$ dB over the bandwidth of 700 MHz, from 1.8 GHz to 2.5 GHz. The bandwidth of the PA is determined by wideband input and output branchline couplers which ensure return losses higher than 20 dB in the passband.

Chapter 6

Conclusion

The modern wireless communications are a rapidly growing segment of the communications industry mainly due to the extreme demands of the end-users, which require a fast and reliable data transfer at any place and at any time. More importantly, the endless application scenarios in which wireless communications are employed, e.g. massive Internet of Things and low-latency remote surgery, surpass the performance of the legacy wireless communication standards. The upcoming standards aim to provide seamless communication at ever-increasing throughputs and spectral efficiencies. This spectral efficiency is readily a result of an increased wireless channel bandwidth and complex signal modulations, both of which push the circuitry in modern handheld devices and base stations to their limits.

More spectral efficiency is usually achieved at the cost of a front-end performance, i.e., the linearity and efficiency of the transmit path of a modern wireless front-end deteriorates significantly if excited by modern modulated wideband signals. In most cases, a radiofrequency power amplifier is a bottleneck for the entire wireless communication channel due to its inherent low linearity in large-signal operation. Furthermore, the time-domain nature of a modern modulated signal, whose average power varies with the signal's envelope, degrade the efficiency of a power amplifier, thus decreasing the battery lifetime in handheld or the cooling costs in base stations. At the circuit level, the decreasing efficiency and linearity of the power amplifier are coped with by adopting advanced transistor technologies and/or high-efficiency circuit architectures. The transistor employed for the design of a power amplifier, determines the maximum possible performance of the circuit to a large extent. Among the vast varieties of different advanced transistor technologies employed for a power amplifier design, a horizontal current bipolar transistor (HCBT) provides a high-performance and low-cost, the two parameters of great importance for the modern radiofrequency hardware.

As a first step in the power amplifier design process employing the HCBTs, the performance of the HCBT is investigated by performing large-signal characterization employing a scalar load-pull measurement setup. The performance of the HCBT is analyzed by performing the

load-pull measurements at 0.9 GHz, 1.8 GHz, and 2.4 GHz. The measurement setup is developed and the methodology for the measurement of output power, gain, and collector efficiency, is described. The measurements are performed for the three linear classes of power amplifier operation, namely, Class-A, Class-AB, and Class-B, wherein optimal source and load impedances for the maximum output power are found for all three classes. For the HCBT with the uniform *n*-collector, the output power, collector efficiency, and transducer gain, of 17.54 dBm, 31.5%, and 10.8 dB, is achieved, respectively, for the Class-A operation at 2.4 GHz. Lowering the bias collector current into Class-B regime, the HCBT achieves output power and collector efficiency of 17.7 dBm and 56.5%, respectively. The optimum is found to be in Class-AB operation, wherein the HCBT achieves output power, collector efficiency, and transducer gain, of 18.6 dBm, 46%, and 9.98 dB, respectively. Furthermore, the HCBT shows the potential for even higher output power, with 22.6 dBm output power and 11.6 dB gain in Class-A regime. Next, three HCBT devices of different collector design are anaylzed; uniform *n*-collector, CMOS *n*-well collector, and low-doped *n*-collector. The low-doped HCBT provides the best overall performance, with its optimal source and load impedances close to 50 Ω and output power, gain, and collector efficiency, of 21.8 dBm, 10.8 dB, and 45.3%, respectively. On the other hand, due to the lower saturation voltage of CMOS *n*-well HCBT, it has the highest efficiency in the power back-off operation. Thus, the two devices provide either the wideband or high-efficiency solutions for the power amplifier design.

The upgrade of the scalar load-pull setup is developed in order to access the time-domain waveforms at the collector and in this way further optimize the load line in Class-A operation. The methodology is described for the measurement of the linear operating area in large-signal operation. The linear operating area is defined as a boundary which defines the maximum collector current swing for the linear response in large-signal regime. The boundary comprises the saturation region and the onset of Kirk effect at high collector currents, the two forming a continuous boundary which determines the maximum available output power for a given transistor. The setup and methodology are next employed to investigate the impact of the nonlinearity in large-signal operation on DC bias point. The measurements are performed for the two limiting cases of base biasing, namely, constant base-emitter voltage (voltage source) and constant base current (current source). Additionally, the DC bias point behaviour is measured for two different mechanisms of load line hard-limitation; hard-limitation in cut-off region and in saturation region. Furthermore, the case wherein the load line crosses the breakdown voltage is also investigated, since this is a common occurrence in large-signal operation. With the hard-limitation in the cut-off, the HCBT exhibits linear input power range, whereas it is opposite for the hard-limitation in the saturation region. Furthermore, a peak in DC collector current is measured in the vicinity of 1-dB compression point when the load line crosses the open-base breakdown voltage. The results provide useful information for the determination of optimal bias and load

impedance conditions for the HCBT in Class-A operation.

After the device characterization, a power amplifier is designed using packaged HCBTs. Firstly, the maximum efficiency is aimed for, while providing the maximum output power for a given HCBT. Therefore, a Doherty power amplifier is designed and fabricated at the fundamental frequency of 2.4 GHz, using two HCBTs of equal characteristics. Firstly, the principle of active modulation is described and the empirical methodology to find the optimum load impedances at both the maximum output power and 6-dB output power back-off points is given. The bias and matching networks are designed in microstrip transmission line technology on an FR4 substrate, which are simulated and optimized employing electromagnetic simulations. The Doherty PA exhibits 45% collector efficiency over the 4-dB output power back-off range, in which it achieves maximum output power of 22 dBm. Furthermore, a bandwidth of 100 MHz is achieved with the collector efficiency of 41.5% and output power of 19 dBm $+/-$ 1.5 dB in the 4-dB back-off point. For a modulated excitation of a WCDMA type, the Doherty achieves average collector efficiency of 38.7% and output power of 16.5 dBm, which is comparable with the power amplifiers implemented in advanced semiconductor technologies.

For the second designed power amplifier, a wide bandwidth is a design goal while extracting the maximum output power out of a chosen HCBT. The chosen architecture for the wideband design is a balanced power amplifier. Again, a balanced amplifier is designed at 2.4 GHz using two identical HCBTs. The bandwidth and input and output return loss are determined in the balanced architecture by the input and output double-box branchline couplers, which are optimized by performing extensive numerical electromagnetic simulations. The balanced power amplifier provides 21.4 dBm $+/-$ 0.18 dB output power, and 10.4 $+/-$ 0.15 dB gain, over the bandwidth of 700 MHz, from 1.8 GHz to 2.5 GHz. Due to the high return losses of the input and output branchline couplers, the return losses of the balanced power amplifier are higher than 20 dB over the entire bandwidth.

In summary, the HCBT technology is characterized in large-signal regime by employing both the scalar and vector load-pull measurements. The parameters crucial for designing high-performance radiofrequency power amplifiers are identified by performing extensive measurements of the collector voltage and current time-domain waveforms, such as a boundary of linear operating area and the impact of the above-breakdown operation on the DC bias point. Both provide necessary information for the optimal Class-A design; a power amplifier which is a mainstay of the radiofrequency hardware, especially for the higher frequencies popular in the modern wireless communications. The suitability of the HCBT is demonstrated by designing both the high-efficiency and wideband power amplifiers, wherein the wideband HCBT power amplifier exhibits comparable or better characteristics with respect to the amplifiers implemented in the advanced and costlier semiconductor technologies. Future work encompasses further large-signal analysis and high-efficiency linearized HCBT power amplifier design.

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Biography

Željko Osrečki graduated from Faculty of Electrical Engineering, Computer Science and Information Technology Osijek in 2014 and from Faculty of Electrical Engineering and Computing in Zagreb in 2016. Over a period from July 2016 to October 2016 he was working on a project "Demonstration of low noise amplifier in horizontal current bipolar transistor technology" as a project engineer. As of October 2016, he is with the Department of Electronics, Microelectronics, Computer and Intelligent Systems as a Research and Teaching Assistant on the project "High-performance Semiconductor Devices for Wireless Circuit and Optical Detection Applications" led by Professor Tomislav Suligoj. His research focus is design and optimization of radiofrequency power amplifiers in advanced horizontal current bipolar technology - HCBT. He is winner of Dean's Award for the team scientific work "Design of quenching circuits for single-photon avalanche diodes".

List of publications

Journal papers

1. Osrečki, Ž., Žilak, J., Koričić, M., Suligoj, T. "Measurement of RF Linear Operating Area of Bipolar Transistors", IEEE Microwave and Wireless Component Letters, Vol. 30, Issue 11, October 2020, pp. 1057-1060.
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1. Osrečki, Ž., Žilak, J., Koričić, M., Suligoj, T. "Impact of Large-signal Operation on DC Operating Point of Horizontal Current Bipolar Transistor", 2020 IEEE BiCMOS and

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9. Osrečki, Ž., Knežević, T., Nanver L. K., Suligoj, T. "Indirect optical crosstalk reduction by highly- doped backside layer in PureB single-photon avalanche diode arrays", 2017 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD), Copenhagen, July 2017, pp. 69-70.
10. Berdalović, I., Osrečki, Ž., Šegmanović, F., Grubišić, D., Knežević, T., Suligoj. T. "Design of Passive-Quenching Active-Reset Circuit with Adjustable Hold-Off Time for Single-Photon Avalanche Diodes", 2016 39th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), Opatija,

Croatia, May 2016, pp. 34-39.

Životopis

Željko Osrečki diplomirao je 2014. godine na Fakultetu elektrotehnike, računarstva i informacijskih tehnologija u Osijeku a potom 2016. godine na Fakultetu elektrotehnike i računarstva u Zagrebu. Od srpnja do listopada 2016. godine zaposlen je kao stručni suradnik na projektu „Demonstracija niskošumnog pojačala upotrebom diskretnih bipolarnih tranzistora s horizontalnim tokom struje“ na Fakultetu elektrotehnike i računarstva u Zagrebu. U listopadu 2016. upisuje doktorski studij na Fakultetu elektrotehnike i računarstva u Zagrebu gdje je zaposlen kao stručni suradnik na projektu „Poluvodički elementi visokih performansi za primjene u sklopovima za bežične komunikacije i optičke detektore“. U sklopu istraživanja bavi se projektiranjem i optimizacijom visokofrekvencijskih pojačala snage u naprednoj bipolarnoj tehnologiji s horizontalnim tokom struje – HCBT. Dobitnik je Rektorove nagrade za timski znanstveni rad pod nazivom „Projektiranje sklopova za potiskivanje proboja fotodioda za detekciju jednog fotona“.