Power management integrated circuit featuring high-efficiency analog techniques

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Sveučilište u Zagrebu
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INTEGRIRANI SKLOP ZA UPRAVLJANJE NAPAJANJEM ZASNOVAN NA ANALOGNIM POSTUPCIMA VISOKE UČINKOVITOSTI

DOKTORSKI RAD

Mentor: prof. dr. sc. Dražen Jurišić

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This doctoral thesis has been done at the University of Zagreb, Faculty of Electrical Engineering and Computing, Department of Electronic Systems and Information Processing.

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Supervisor: Professor Dražen Jurišić, Ph.D.

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About the supervisor

Dražen Jurišić received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Zagreb, Croatia, in 1990, 1995, and 2002, respectively. From 1997 to 1999, he was with the Institute of Signal and Information Processing, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland. Since 2008, he has been visiting the Faculty of Engineering at Bar-Ilan University, Israel, and doing research in the field of analog circuits and filters. He is currently a full professor at the Faculty of Electrical Engineering and Computing (FER), University of Zagreb. He lectures in the field of electrical circuits, signals and systems, and analog and mixed-signal processing circuitry. His research interests include analog and digital signal processing and filter designs, integrated circuit designs, and the study and analysis of fractional-order systems. He has been an MC Member of the COST Action CA15225 ‘‘Fractional-Order Systems: Analysis, Synthesis and Their Importance for Future Design.’’ He is a member of the Croatian Society for Communications, Computing, Electronics, Measurement and Control and the IEEE-CAS Society. He was awarded the Silver Plaque Josip Loncar for a distinguished Ph.D. thesis and an IEEE Best Paper Finalist Award for a conference paper.

O mentoru

Dražen Jurišić diplomirao je 1990., magistrirao 1995., te doktorirao 2002. godine na Sveučilištu u Zagrebu, Fakultet elektrotehnike i računarstva. Od 1997. do 1999. radio je na Institutu za obradu signala i informacija, Švicarskog saveznog instituta za tehnologiju (ETH), Zürich, Švicarska. Od 2008. godine boravi na Tehničkom fakultetu Sveučilišta Bar-Ilan u Izraelu i bavi se istraživanjem u području analognih sklopova i filtara. Trenutno je redoviti profesor na Fakultetu elektrotehnike i računarstva (FER) Sveučilišta u Zagrebu. Predaje iz područja električnih krugova, signala i sustava, te analognih i mješovitih sklopova za obradu signala. Njegovi istraživački interesi uključuju analognu i digitalnu obradu signala, dizajn filtara, dizajn integriranih sklopova te proučavanje i analizu sustava frakcijskog reda. Bio je član MC-a COST Action CA15225 "Fractional-Order Systems: Analysis, Synthesis and Their Importance for Future Design". Član je Hrvatskog društva za komunikacije, računarstvo, elektroniku, mjerenje i upravljanje i IEEE-CAS društva. Dobitnik je Srebrne plakete Josip Lončar za istaknutu doktorsku disertaciju, te nagrade IEEE Best Paper Finalist Award za konferencijski rad.

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Abstract

The rapid advancement of Internet-of-Things (IoT) devices has pushed the boundaries of System-on-Chip (SoC) solutions, leading to a higher demand for stable on-chip power supplies. The primary function of an integrated power management circuit is to generate required voltage levels on-chip from an external energy source while ensuring high energy efficiency, speedy response, and stability. Additionally, the energy harvesting function may be included as part of the power management circuit, enabling the utilization of energy from the environment to improve overall energy efficiency. The scientific contribution to the field of fully integrated power management was conducted in a way of designing and producing four distinguished integrated circuits: a step-down DC-DC converter in TSMC 65nm, a boost DC-DC converter in TSMC 180nm, a low-power clock generator in TSMC 180nm, and a digitally controlled fractional-order capacitor in AMS 350nm. Measured and simulated results indicate that novel circuits and techniques developed during research for doctoral studies enable the state-of-the-art performance of DC-DC converters in terms of energy efficiency, power density, and speed. The fact that DC-DC converters play a crucial role in power management makes the presented circuits inspiring solutions for low-power applications of IoT devices.

Keywords: DC-DC converters, clock generators, energy harvesting, power management, analog techniques, efficiency, fractional order, regulation.

Prošireni sažetak

Integrirani sklop za upravljanje napajanjem zasnovan na analognim postupcima visoke učinkovitosti

Brzi napredak Internet-of-Things (IoT) uređaja doveo je do povećane potražnje za stabilnim izvorima napajanja izvedenim na čipu. Integrirani IoT uređaj obično zahtijeva više naponskih razina koje se generiraju iz jednog vanjskog izvora energije. Napon napajanja digitalne domene kreće se od 0.5 V do 1.2 V, dok analogni sklopovi zahtjevaju nešto viši napon za rad (1.2 V do 5 V). Vanjski izvor energije često je nestabilan, te može ovisti o temperaturi, šumu, potrošnji energije i drugim čimbenicima. Kod sustava koji koriste baterijsko napajanje, razina napona baterije može varirati ovisno o njenoj napunjenosti dok sklopovlje unutar čipa obično zahtijeva stabilan napon napajanja unutar određenih granica. Primarna funkcija potpuno integrirane jedinice za upravljanje napajanjem je osiguranje potrebnih napona napajanja za sustav na čipu uz što bolju energetsku učinkovitost, brzinu i stabilnost. Energetski učinkovito upravljanje napajanjem od iznimne je važnosti jer izravno utječe na energetsku učinkovitost cijelog sustava, čime se znatno produljuje vijek trajanja baterije (ili potrošnju alternativnog izvora energije). Jedinica za upravljanje napajanjem za najsuvremenije IoT uređaje obično se sastoji od nekoliko međusobno povezanih regulatora napona koji skupnim radom osiguravaju potrebne napone uzevši u obzir zahtjeve sustava.

Primarna funkcija regulatora napona, kao ključne komponente u upravljanju napajanjem, je pretvaranje jedne razine napona u drugu. Ovaj proces je ključan za održavanje stabilnog i reguliranog napajanja sustava. Regulator napona možemo opisati kroz sustav koji kao ulaznu veličinu prima ulazni napon i referentni napon, a na izlazu daje izlazni napon. Razina ulaznog napona koju regulator dobiva obično je nestabilna i nepredvidiva. Nasuprot tome, razina izlaznog napona mora biti regulirana i stabilna unutar određene tolerancije. Ovisno o vrsti regulatora, sustav može ili ne mora zahtjevati ulazni signal takta. Referentni napon smatra se konstantnom razinom napona na koji, u teoriji, ne utječu drugi čimbenici. U praksi referentni napon obično ima vrlo malu ovisnost o temperaturi, razini napona napajanja, šumu, opterećenju i ostalim faktorima, a koristi se kao referentna točka za regulaciju izlaznog napona. Ovisno o konfiguraciji regulatora,

izlazni napon može biti reguliran na razinu referentnog napona ili na razinu referentnog napona pomnoženog s cjelobrojnim faktorom. Jedan od glavnih parametara za svaki regulator napona je energetska učinkovitost, a definira se kao omjer izlazne i ulazne snage. Kod razmatranja integriranih regulatora, gustoća snage postaje važan parametar budući da površina silicija određuje cijenu izrade čipa. Definicija gustoće snage jednaka je omjeru izlazne snage i aktivne površine regulatora na čipu. Budući da regulatori napona mogu raditi s nizom različitih ulaznih i izlaznih napona, uveden je parametar nazvan omjer pretvorbe napona, a označava omjer između izlaznog i ulaznog napona. Valovitost izlaznog napona koristi se za opisivanje varijacija izlaznog napona za vrijeme statičkih uvijeta rada (obično se izražava kao vrijednost izmjenične komponente izlaznog napona od vrha do vrha), dok se varijacije izlaznog napona u dinamičkim uvjetima mogu opisati kroz propad ili nadvišenje napona. Glavni okidač za propad ili nadvišenje je brza prijelazna promjena izlazne struje. Proporcije napona valovitosti i propada odnosno nadvišenja uglavnom su određene brzinom regulatora i kapacitetom izlaznog kondenzatora. Dvije glavne kategorije regulatora napona su linearni regulatori i prekidački DC-DC konverteri. Osnovna razlika je u tome što linearni regulatori ne mijenjaju konfiguraciju u ovisnosti o vremenu (moguće ih je opisati jednim nadomjesnom strujnim krugom), dok prekidački regulatori rade u dvije faze koje se izmjenjuju u vremenu i svaka od faza ima zaseban nadomjesni strujni krug. Osnovno ograničenje kod linearnih regulatora je to što je teoretski maksimalna energetska učinkovitost jednaka omjeru pretvorbe napona. Bez obzira na ovaj faktor ograničenja, linearni regulatori naširoko se koriste kad god je to moguće zbog jednostavnosti, pouzdanosti i superiornih performansi u svim parametrima osim učinkovitosti za niski omjer pretvorbe napona. Drugo ograničenje linearnih regulatora je nemogućnost proizvodnje izlaznog napona većeg od ulaznog. Zbog svoje nelinearne prirode rada, rješenje za oba ograničenja pružaju prekidački DC-DC konverteri (pretvarači). Paralelno s razvojem DC-DC konvertera, uveden je dodatni pokazatelj vrijednosti nazvan faktor poboljšanja učinkovitosti kako bi se posebno opisali DC-DC pretvarači. Razlog tome leži u činjenici da klasična učinkovitost ponekad može dovesti u zabludu jer se implementiraju različiti omjeri pretvorbe napona. Složenost postizanja visoke učinkovitosti obrnuto je proporcionalna s omjerom pretvorbe napona (za niži omjer pretvorbe napona izvedba je složenija s više sklopki i više reaktivnih elemenata). Nadalje, DC-DC pretvarači s visokim omjerom pretvorbe napona (blizu 1) mogu se jednostavno zamijeniti linearnim regulatorima, čime se smanjuje njihova vrijednost u praktičnim primjenama. Faktor poboljšanja učinkovitosti važan je parametar kada se

uspoređuju silazni (buck) DC-DC pretvarači, jer uzima u obzir i učinkovitost i omjer pretvorbe napona. U prektičnom smislu ovaj parametar opisuje koliko je razmatrani DC-DC pretvarač bolji u odnosu na idealan linearni regulator u pogledu energetske učinkovitosti, za isti omjer pretvorbe napona. Ovisno o vrsti reaktivnog elementa korištenog za pohranu energije, razlikujemo dvije skupine DC-DC pretvarača: kapacitivne i induktivne. Glavna razlika je u tome što kapacitivni pretvarači pohranjuju energiju u obliku napona na kondenzatoru, dok induktivni pretvarači pohranjuju energiju u obliku struje kroz zavojnicu. Kod potpuno integriranih sustava, kapacitivni DC-DC pretvarači superiorni su u gotovo svim aspektima u odnosu na induktivne i stoga nailaze na mnogo širu upotrebu. Razlog tome je teškoća u proizvodnji visokokvalitetnih zavojnica na siliciju. Glavni nedostatak kapacitivnih DC-DC pretvarača je fiksan omjer pretvorbe napona koji je definiran mrežnom konfiguracijom prekidajućih kondenzatora.

Proces kojim se električna energija dobiva iz vanjskih izvora (svijetlost, mehaničke vibracije, toplina, zračenje, itd.) i koristi kao izvor napajanja za električne uređaje naziva se prikupljanje energije. Prikupljena energija može se koristiti kao jedini izvor napajanja sustava ili se može koristiti kao djelomični izvor energije za produljenje vijeka trajanja baterije. Zbog trenda samodostatnih uređaja male snage, prikupljanje energije često se implementira kao dio sustava upravljanja napajanjem. Potpuno integrirani IoT uređaji posebno su zanimljivi za prikupljanje energije budući da je sustave niske potrošnje lakše proizvesti na čipu, što omogućuje da prikupljena energija postane glavni izvor napajanja. Budući da ambijentalni izvori energije obično generiraju električne signale u obliku neprikladnom za napajanje (preniskog napona i nestabilni), središnji zadatak procesa prikupljanja energije vrti se oko generiranja razina izlaznog napona pogodnih za daljnju upotrebu. Rješenje za ovaj problem obično je dodatni DC-DC pretvarač s omjerom pretvorbe napona većim od jedan (boost DC-DC pretvarač). U slučaju da je prikupljeni signal izmjeničnog valnog oblika, kao što je radio val, vibracija piezoelektričnog senzora i slično, potrebno ga je prvo ispraviti, a zatim pojačati na potrebnu naponsku razinu. Za razliku od konvencionalnog DC-DC pretvarača, gdje se snaga regulira na temelju struje opterećenja, DC-DC prikupljač treba regulirati svoju snagu na temelju ulaznog naboja. Na taj se način energija sakuplja uz maksimalnu učinkovitost. Izlazni napon u ovom slučaju nije toliko kritičan jer se obično spaja na veliki kondenzator ili bateriju, što ga čini stabilnim. Sekundarna regulacijska petlja ponekad se može implementirati za povremeno pražnjenje izlaznog čvora u bateriju. Sustav može biti samodostatan ako prosječna prikupljena energija premašuje potrošnju energije kruga. Međutim,

gotovo je uvijek potreban neki oblik pohrane energije jer je prikupljeni signal nepredvidiv. Čak i ako je prosječna potrošnja energije manja od prosječne prikupljene energije za dulji vremenski interval, u nekim trenucima može biti suprotno, što bi uzrokovalo kvar sustava bez pohrane energije.

Generator takta je električni krug korišten za proizvodnju signala takta. Signal takta obično je pravokutnog valnog obilika, poznate i jasno definirane frekvencije, te se koristi za sinkronizaciju ostalih krugova u sustavu. Za kvalificiranje i usporedbu generatora takta potrebno je uzeti u obzir nekoliko važnih parametara. Uz osnovne parametre kao što su raspon napona napajanja i raspon izlazne frekvencije, potrebno je definirati dodatne parametre kao što su potrošnja energije, radni ciklus i temperaturni koeficijent. Budući da se generatori takta koriste za vrlo širok raspon aplikacija, važnost određenog parametra ovisi o primjeni. Jednostavna potrošnja energije izražena u vatima ponekad nije dovoljno dobar parametar za usporedbu budući da je veća vjerojatnost da će generatori takta s višom frekvencijom imati veću potrošnju energije. Iz tog razloga, dodatni parametar koji se zove energetska učinkovitost definiran je kao omjer potrošnje energije i frekvencije. Energetska učinkovitost jedan je od kritičnih parametara za generatore takta koji se koriste u upravljanju napajanjem budući da je glavna svrha upravljanja napajanjem učinkovito korištenje energije. IoT uređaji male snage obično rade u stanju mirovanja većinu vremena. Faktor niske aktivnosti znači da se mnogi podsustavi, uključujući generatore takta, moraju često aktivirati i deaktivirati. U takvom scenariju vrijeme pokretanja postaje važan parametar.

Studija prethodnog stanja tehnike koja se odnosi na integrirano upravljanje napajanjem pokazuje da su područja male snage posebno izazovna za postizanje dobrih performansi. Razlog tome je ograničena količina raspoložive snage koju je potrebno rasporediti između podsklopova zaduženih za obavljanje različitih zadataka. Daljnja analiza pokazuje da prethodno objavljani DC-DC pretvarači male snage imaju problema s niskom učinkovitošću, niskom gustoćom snage i sporim prijelaznim odzivom. Također, često zahtijevaju veliki izlazni kondenzator što ograničava njihovu praktičnu primjenu.

Glavni fokus ovog doktorskog rada je poboljšanje upravljanja napajanjem u područjima energetske učinkovitosti i brzine uvođenjem inovativnih integriranih sklopova i tehnika. Za potrebe istraživanja proizvedena su četiri potpuno integrirana sustava, a rezultati su objavljeni u obliku jednog konferencijskog rada i tri rada u časopisima. Drugo poglavlje opisuje silazni (buck) DC-

DC pretvarač proizveden u tehnologiji TSMC 65nm i objavljen kao konferencijski rad s proširenom verzijom u časopisu. Uzlazni (boost) DC-DC pretvarač proizveden u tehnologiji TSMC 180nm kao dio platforme za senzor slike, objavljanoj u časopisu, predstavljen je u trećem poglavlju. Generator takta male snage, kao dio iste platforme za senzor slike, ilustriran je u četvrtom poglavlju. Dodatni doprinos području potpuno integriranog upravljanja napajanjem implementiran je u obliku digitalno kontroliranog kondenzatora necjelobrojnog reda, dizajniranog u tehnologiji AMS 350nm, objavljenog u časopisu, te opisanog u petom poglavlju.

Osnovni znanstveni doprinos, kako u pogledu energetske učinkovitosti tako i u pogledu brzine, opisan je u drugom poglavlju. Silazni DC-DC pretvarač temeljen na inverteru pokazuje poboljšanje stanja tehnike svojim faktorom poboljšanja efikasnosti od 66%, gustoćom snage od 2.56 mW/mm^2 i brzim prijelaznim odzivom koji ne pokazuje propade niti nadvišenja . Brzina predstavljenog DC-DC pretvarača omogućuje mu rad s minimalnim izlaznim kondenzatorom od 50pF, što dodatno štedi površinu silicija. Glavna nova značajka koja je omogućila vrhunske rezultate bila je komparator zasnovan na inverteru. Loše strane inverterskog komparatora su prevladane dodatnom regulacijskom petljom za napon napajanja invertera. Precizne analogne tehnike korištene su za postizanje dodatnih značajki kao što su mogućnost korištenja srednjih izlaznih napona i smanjena potrošnja uslijed prekidanja. Učinkovitost, brzina i gustoća snage predloženog DC-DC pretvarača čine ga korisnim rješenjem za sveprisutne integrirane sustave za upravljanje napajanjem u IoT uređajima.

Dodatni znanstveni doprinosi prikazani su u trećem, četvrtom i petom poglavlju. Uzlazni DC-DC pretvarač kao dio platforme za senzor slike opisan je u trećem poglavlju. Glavna svrha DC-DC pretvarača u ovoj aplikaciji je povećanje razine napona u procesa prikupljanja energije, čime se poboljšava energetska učinkovitost cijelog sustava. Energija je sakupljena iz naboja prikupljenog od fotodioda. Budući da fotodiode počinju puštati struju blizu razine napona praga (~500 mV), naponski čvor koji prikuplja naboj potrebno je držati ispod te razine (~450 mV). Implementirani DC-DC pretvarač koristi se za povećanje napona diode na razinu prikladnu za punjenje baterije (~1.5 V) s vršnom učinkovitošću od 60%. Potrebno je naglasiti da se iste fotodiode koje služe za prikupljanje energije također koriste za očitanje slike, a detekcija događaja provodi se tijekom prikupljanja energije. Ova nova značajka omogućuje dulje cikluse prikupljanja energije što dovodi do boljih značajki samoodrživih senzora slike.

Generator takta male snage s implementiranom kompenzacijom temperature i radnog ciklusa opisan je u četvrtom poglavlju. Primjena sklopa demonstrirana je u platformi za senzor slike, također spomenutoj u trećem poglavlju. Postignuto je dodatno poboljšanje energetske učinkovitosti sustava korištenjem generatora takta male snage dizajniranog posebno za ovu svrhu. Strujno kontrolirani prstenasti oscilator koristi se za proizvodnju početnog signala, koji se zatim pomiče po razini, te mu se kompenzira radni ciklus. Glavni nedostatak ovakvog dizajna je velika temperaturna ovisnost strujno upravljanog prstenastog oscilatora. Ovaj problem prevladan je uvođenjem izvora struje koji ima suprotnu temperaturnu ovisnost od oscilatora, te je na taj način izvedena kompenzacija temperaturnog koeficienta. Generator takta pokazuje vrhunske značajke u pogledu površine od 0.019mm2, energetske učinkovitosti od 0.6 μW/MHz (0.3 μW/Mhz prije kompenzacije radnog ciklusa), te vremena pokretanja od 5 μs.

Peto poglavlja opisuje digitalno upravljani kondenzator frakcionalnog reda koji radi u frekvencijskom rasponu relevantnom za DC-DC pretvarače s prekidajućim kondenzatorima. Ovakava realizacija utječe na sustave upravljanja napajanjem iz razloga što frakcionalni kondenzator može biti korišten kao reaktivni element unutar jezgre DC-DC pretvarača ili regulacijski element unutar regulacijske petlje u svrhu poboljšanja energetske učinkovitosti. Dizajnirani frakcionalni kondenzator može postići tri različita fazna pomaka: -30°, -45° i -60°. Na taj način djeluje kao frakcija standardnog kondenzatora (1/3, 1/2 i 2/3).

Integrirani sklopovi opisani u ovom diplomskom radu unaprijedili su područje potpuno integriranog upravljanja napajanjem u nekoliko aspekata, što ih čini inspirativnim rješenjima za aplikacije niske potrošnje IoT uređaja.

Ključni riječi: DC-DC pretvarači, generator signala takta, prikupljanje energije, upravljanje napajanjem, analogne tehnike, učinkovitost, frakcionalni red, regulacija.

Contents

1. INTRODUCTION TO AN INTEGRATED POWER MANAGEMENT SYSTEMS

Power Management

The rapid advancement of Internet-of-Things (IoT) devices has pushed the boundaries of System-on-Chip (SoC) solutions, leading to a higher demand for stable on-chip power supplies. An integrated IoT device typically requires multiple voltage levels to be generated from a single external energy source. The digital domain supply voltages range from 0.5 to 1.2V, while analog circuits need a slightly higher voltage to operate (1.2V to 5V). However, the external energy source is often unstable, with temperature, noise, power consumption, and other factors influencing voltage variations. For instance, the voltage level of a battery can vary depending on its charge. Yet, the circuits inside the chip usually require a stable voltage within a certain limit. Moreover, the use of energy harvesting within the system is becoming more prevalent due to the demand for self-sustaining, low-power devices. The primary function of a fully integrated power management unit, as depicted in Fig. 1.1, is to address all these requirements while ensuring high energy efficiency, speed, and stability.

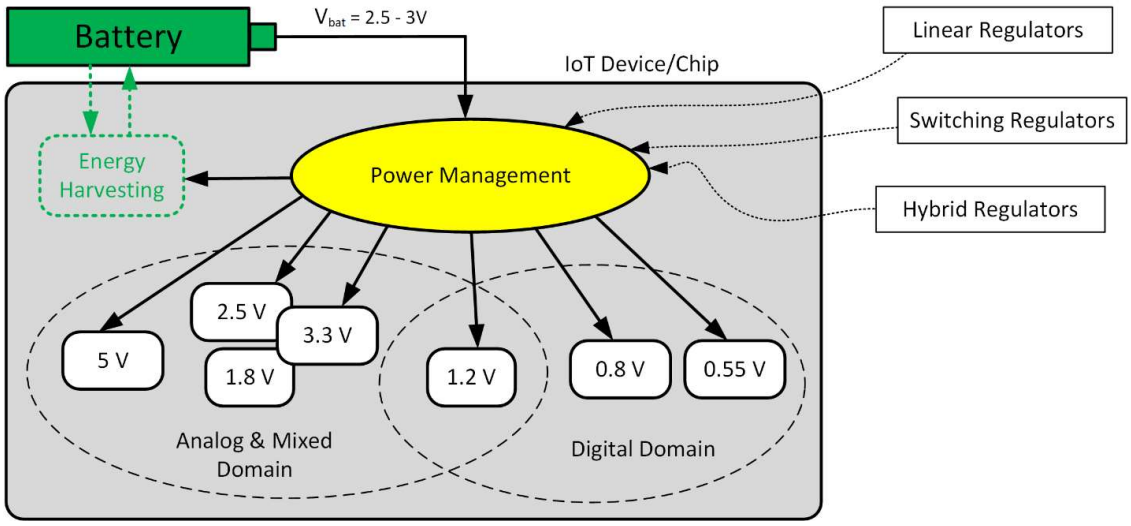


Fig. 1.1. Power Management for IoT Devices.

Energy-efficient power management is of utmost importance as it directly influences the energy efficiency of the entire system, thereby significantly extending the life of the battery (or alternative energy source). A power management unit for cutting-edge IoT devices typically comprises several interconnected voltage regulators that work in tandem to produce voltage supplies based on the system's requirements, highlighting the benefits of energy-efficient power management.

Voltage Regulators

The primary function of a voltage regulator, a key component in power management, is to convert electrical energy from the input voltage level (Vin) to the output voltage level (Vout), as demonstrated in Fig. 1.2. This process is crucial in maintaining a stable and regulated power supply for the system.

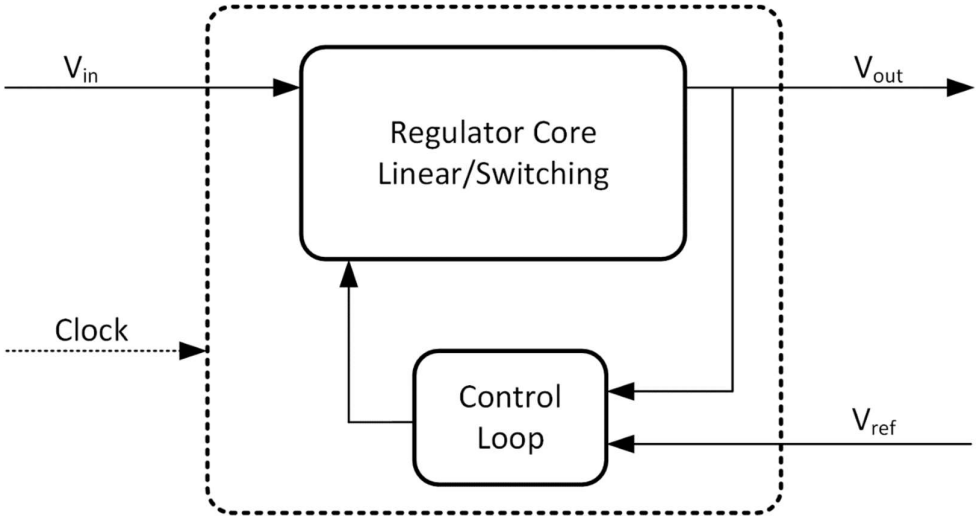


Fig. 1.2. Voltage regulator.

The input voltage level is typically expected to be unstable and unpredictable. In contrast, the output voltage level needs to be regulated and stable within a certain tolerance. Depending on the type of regulator, the system may or may not need an input clock signal. Voltage reference (V_{ref}) is considered a constant voltage level that, in theory, is not affected by other factors. In practice, V_{ref} usually has some very small dependence on the temperature, supply voltage level, noise, load, etc. It is used as a reference point for the regulation of the output voltage.

Depending on the regulator configuration, V_{out} can aim to be equal to V_{ref} or equal to V_{ref} multiplied by some constant factor.

One of the main parameters for every voltage regulator is power efficiency (η), and it is defined as

$$\eta = \frac{P_{out}}{P_{in}} \tag{1.1}$$

where the output power is P_{out} and the input power is P_{in}. When integrated regulators are considered, Power-Density (PD) becomes an important parameter since the silicon area determines the price of the chip. It is defined as

$$PD = \frac{P_{out}}{A} \tag{1.2}$$

where A stands for the active area of the regulator on silicon. Since voltage regulators can operate with a variety of different input and output voltages, a parameter called Voltage-Conversion-Ratio (VCR) is introduced as

$$VCR = \frac{V_{out}}{V_{in}} \tag{1.3}.$$

Output voltage ripple (V_{ripple}) is used to describe peak-to-peak variations of the output voltage during the static conditions, while output voltage variations in the dynamic conditions could be observed as voltage droop and overshoot. The main trigger for droops or overshoots is a fast transient output current (I_{out}) change. Proportions of both V_{ripple} and droops/overshoots are mainly determined by the regulator speed and capacitance of the decoupling capacitor (C_{out}). To illustrate the described parameters, a previously published transient response of the fully integrated DC-DC converter is shown in Fig. 1.3 [1]. Significant droop and overshoot events in V_{out} can be observed during the transient load changes (the load resistance is varied from 100 kΩ towards 9.1 kΩ and back to 100 kΩ). Also, in static conditions, when the load resistance

is constant, an output voltage ripple is visible. The clock signal waveform shows that the output power regulation is conducted by the clock frequency change.

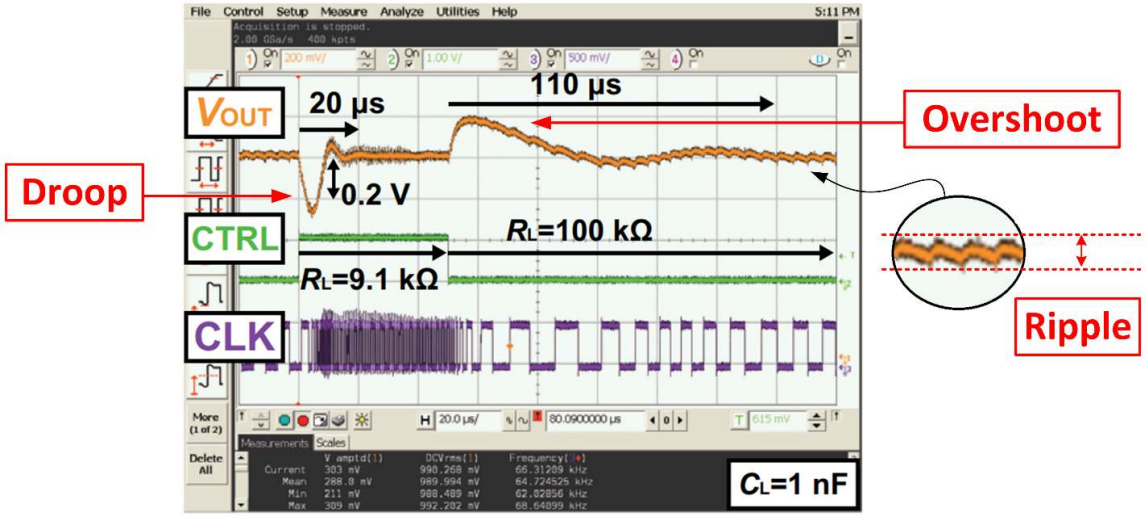


Fig.1.3. Ripple, droop, and overshoot.

Two main categories of voltage regulators are linear and switching DC-DC converters. Figure 1.4 shows an example of a Low-Drop-Out (LDO) linear regulator where the simple regulation loop is implemented with an operation amplifier.

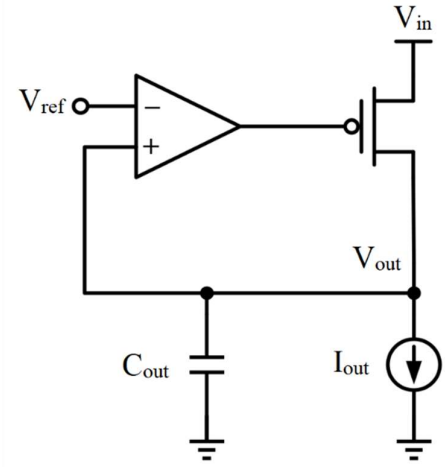


Fig. 1.4. Low-Drop-Out (LDO) linear regulator.

The resistance of the PMOS transistor is regulated so that V_{out} always tends to follow V_{ref}. It can be observed that the power loss will always be proportional to the difference between V_{in} and V_{out}. This fact results in the main limitation of the efficiency regarding the linear voltage regulators:

$$\eta_{max} = VCR \tag{1.4}$$

Regardless of this limitation factor, linear regulators are widely used whenever possible due to simplicity, reliability, and superior performance in all areas except efficiency for low VCR. Another limitation of the linear voltage regulators is the inability to produce V_{out} higher than V_{in}. The solution for both limitations is provided by switching DC-DC converters. The block diagram of the generic DC-DC converter is presented in Fig. 1.5. The main reason for its nonlinear behavior originates from the DC-DC core that changes configuration over time (contains switches and reactive elements). The DC-DC converters require a clock signal and usually operate in two phases. During the first phase (charge phase), the charge is transported from the energy source (V_{in}) and stored inside a reactive element (capacitor or inductor). In the second phase, the charge is delivered to the load (V_{out}). The control loop of the DC-DC converter usually regulates output power by the clock frequency or duty cycle.

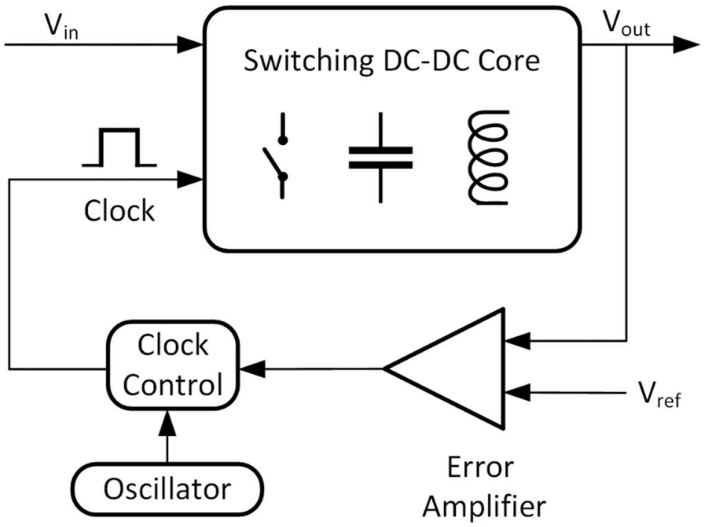


Fig. 1.5. Nonlinear (switching) regulator.

Following the development of the DC-DC converters, an additional Figure-Of-Merit (FOM) called Efficiency-Enhancement-Factor (EEF) is introduced to describe step-down DC-DC converters specifically. The reason for this lies in the fact that classical efficiency sometimes could be misleading because various VCRs are being implemented. Difficulty in achieving high efficiency is inversely proportional with converters VCR due to the complexity of the core (more switches and more reactive elements). Additionally, DC-DC converters with high VCR (close to 1) can be easily replaced with linear regulators, thus reducing their value in practical applications.

The EEF is an important parameter when comparing step-down (buck) DC-DC converters, as it considers both the efficiency and the VCR [2]. EEF is defined as

$$EEF = 1 - \frac{\eta_{lin}}{\eta_{sw}} \tag{1.5}$$

where η_{lin} is the efficiency of an ideal LDO, and η_{sw} is the efficiency of the DC-DC converter under consideration. For instance, a DC-DC converter with a VCR of 0.8 and an efficiency of 80% may not be useful, as it is similar to an LDO, resulting in an EEF of 0. Conversely, a DC-DC converter with an efficiency of 50% but a VCR of 0.2 would have an EEF of 60%, indicating superior performance over an LDO. The VCR used for EEF calculation is the actual achieved ratio between V_{out} and V_{in}, which is slightly lower than the topology VCR determined by the number of flying capacitors. The reason for that lies in the fact that "real" VCR takes into account additional IR drop that always exists at the output voltage.

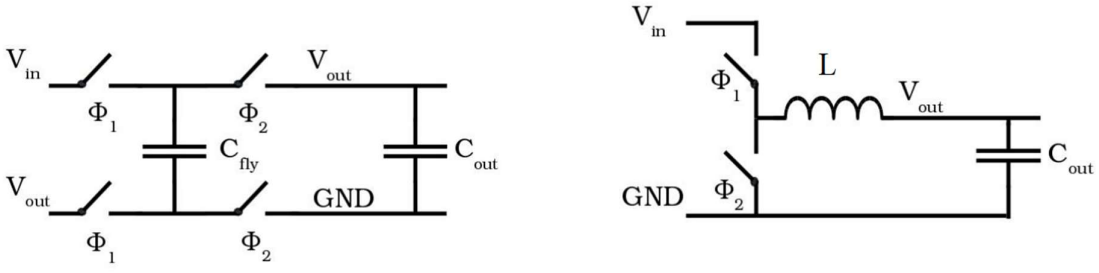


Fig. 1.6. Simple concept of the capacitive and inductive DC-DC converter [2].

Depending on the type of reactive element, two groups of DC-DC converters can be distinguished: capacitive and inductive (Fig. 1.6). The main difference is that capacitive converters store energy in the form of voltage on the capacitor (Cfly), while inductive converters store energy in the form of current through the inductor (L). Table 1.1 shows a general comparison between the two types of integrated DC-DC converters [3].

Table 1.1. Comparison between Inductive and capacitive DC-DC converter type

	Inductive type	Capacitive type
Energy Transfer	Low Q-factor	High Q-factor
Inpact of Scaling	No influence on Q-factor	Improving Q-factor
EMI	EF radiated	EF between plates
Modeling	Finite element	Spice
η_{theory}	100%	<100%
$\eta_{practical}$	Low	High
Flexibility	Broad I/O range	Small I/O range

Unlike in the case of non-integrated converters, it can be observed that capacitive DC-DC converters are superior in many areas and thus have much more widespread usage. The reason for that is the difficulty in producing high-quality inductors in silicon. The quality of the reactive elements is quantified in the Quality factor (Q-factor) in the following equations:

$$Q_L = \frac{2\pi f L}{R} \tag{1.6}$$

$$Q_C = \frac{2\pi f C}{R} \tag{1.7}$$

where R stands for equivalent serial resistance of the considered reactive element while f represents the frequency of interest.

The main disadvantage of capacitive DC-DC converters is that their VCR depends on the Switch-Capacitor (SC) network configuration. Therefore, many different SC networks are used

to achieve desired VCRs. Fig. 1.7 shows an example of a stacked SC network with charge and discharge phases including equivalent electrical circuits.

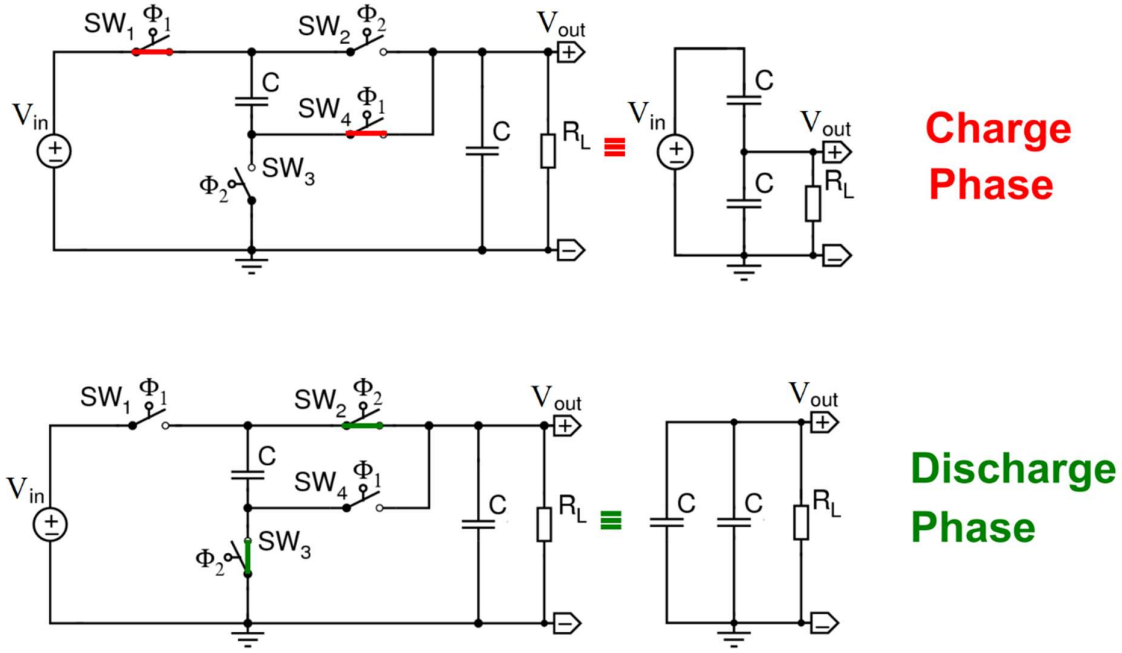


Fig. 1.7. Operating phases of the DC-DC converters [3].

Even though the configuration VCR is a fixed number, ½ in this case, the output voltage can be regulated to some extent by changing the output resistance (R_{out}) of the DC-DC converter, as shown in Fig. 1.8. The real ratio of the V_{out} and V_{in} is always going to be lower than topology VCR due to the voltage drop on the equivalent R_{out}. The main factor that determines R_{out} is switching frequency (clock frequency). With a higher switching frequency, the DC-DC converter is able to deliver more charge to the V_{out}, and thus, the load sees a lower R_{out}. The regulation loop aims to adjust the clock frequency depending on the load current.

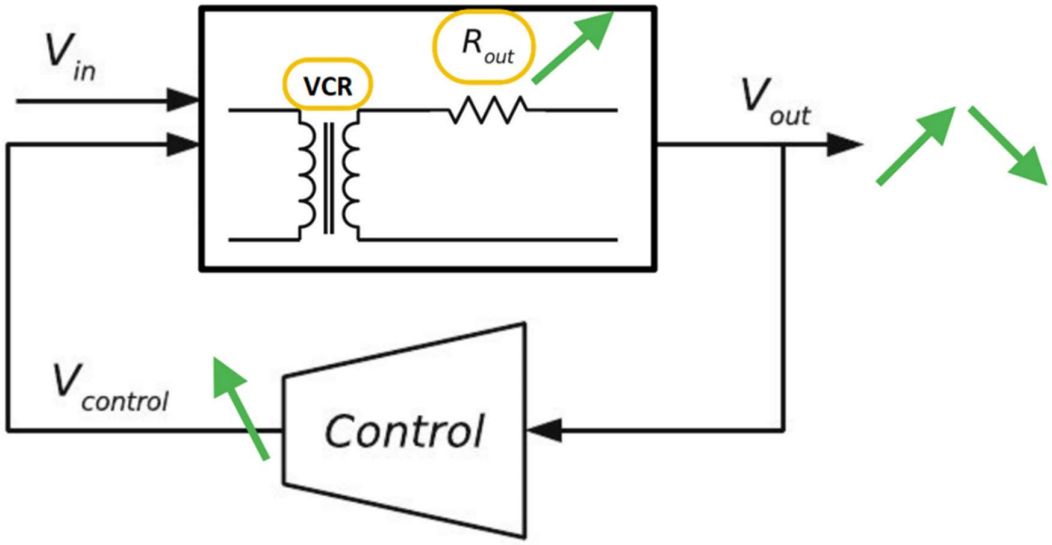


Fig. 1.8. Output resistance control [3].

Figures 1.9 – 1.12 [3] show different SC networks that are used to accomplish various VCRs with equivalent circuits for both phases. Parallel-series SC network can be used in cases when VCR is greater than one, i.e., V_{out} is greater than V_{in} (Fig. 1.9). Ladder SC network, shown in Fig. 1.11, features all flying capacitors having the same voltage between the plates. This can be useful since the V_{in} is divided, so each capacitor needs to sustain only a fragment of it. Ladder-star represents a variation where all bottom plates of the C_{fly} are connected, thus reducing the effect of the parasitics (Fig. 1.12). The ladder-star SC network is particularly important in the case of integrated DC-DC converters since the parasitic capacitance of the C_{fly} could be as large as 10% of the nominal capacitance value.

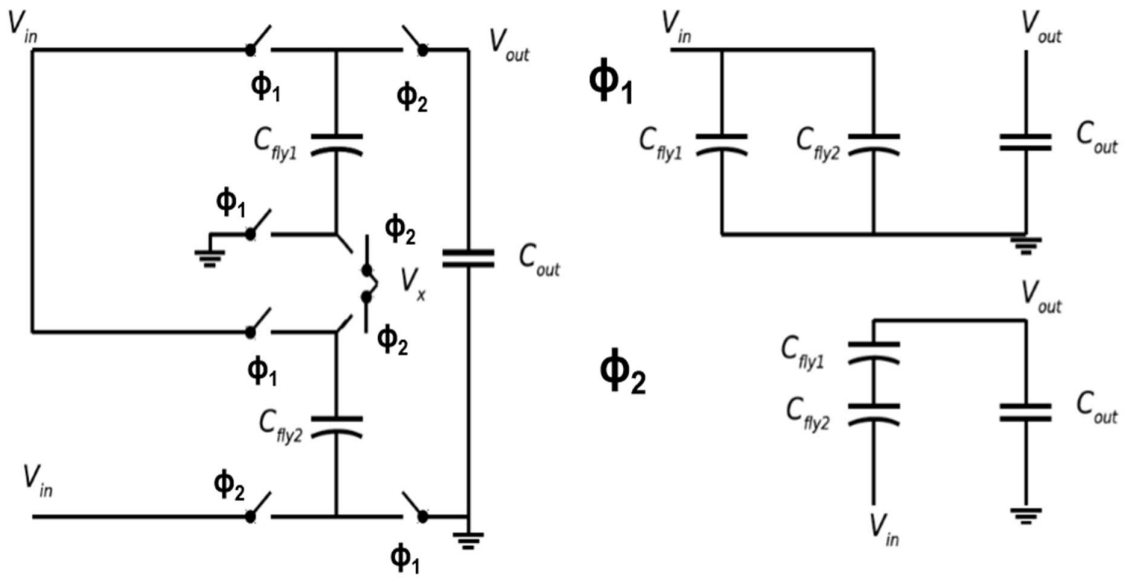


Fig. 1.9. Parallel-series SC network.

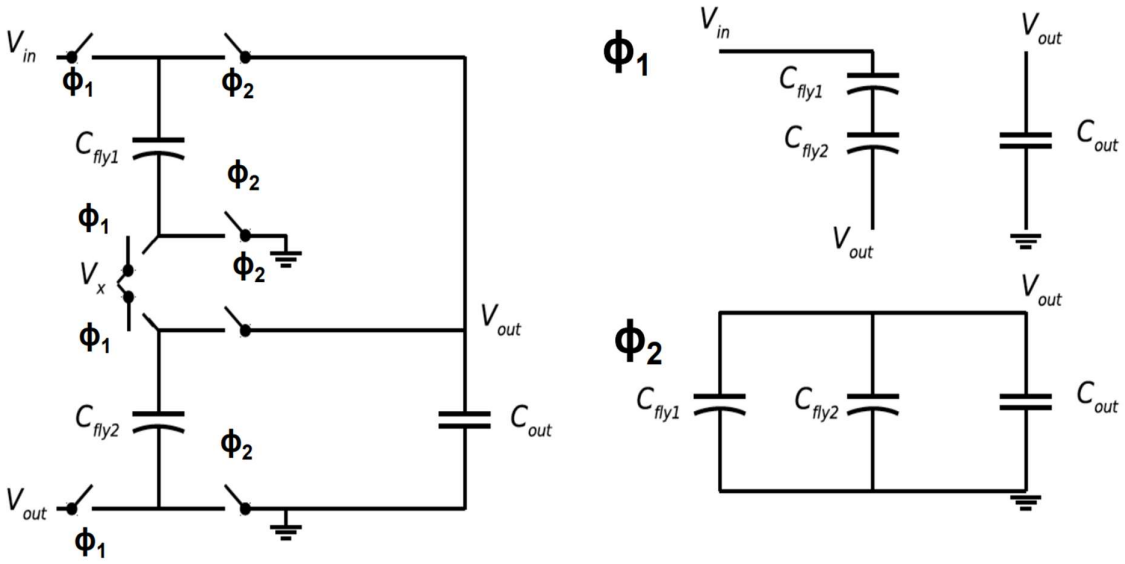


Fig. 1.10. Series-parallel SC network.

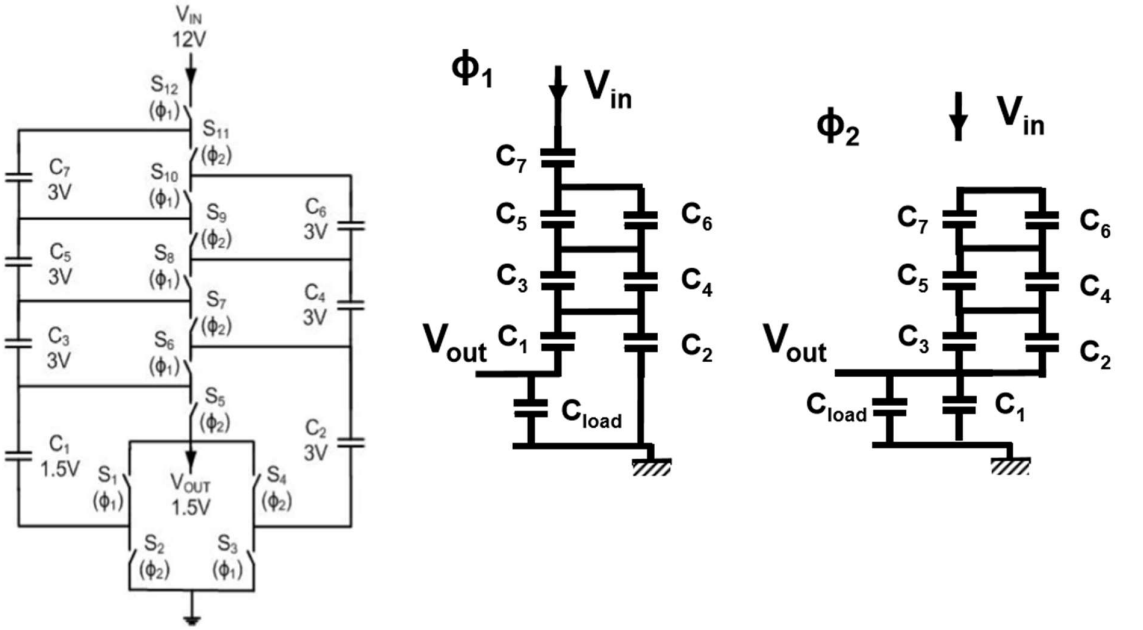


Fig. 1.11. Ladder SC network.

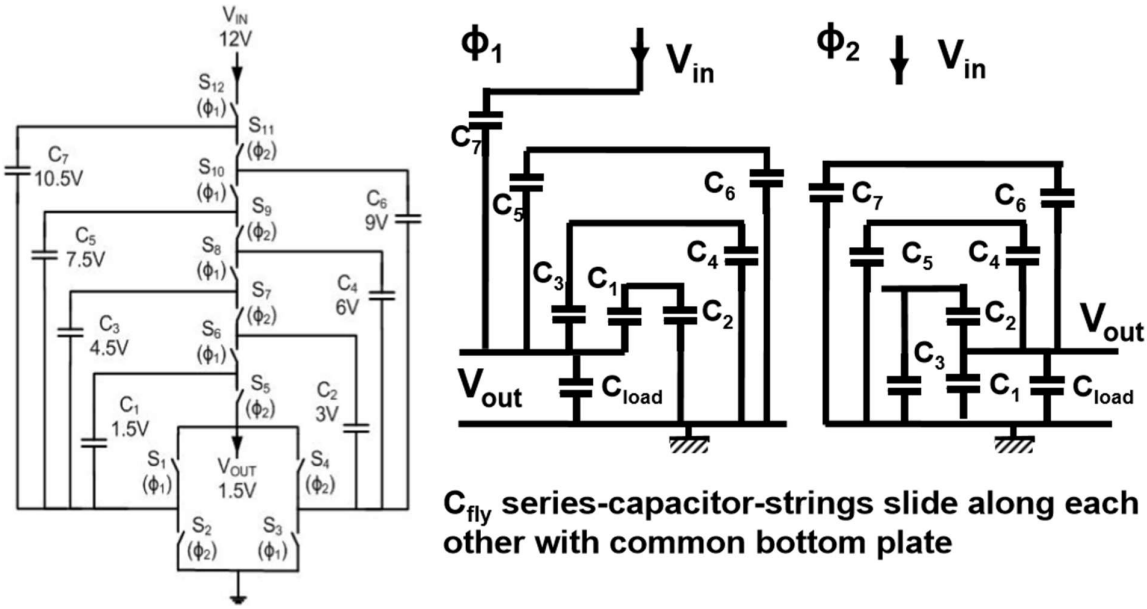


Fig. 1.12. Ladder-star SC network.

Energy Harvesting

The process by which electrical energy is derived from external sources (light, mechanical vibrations, heat, radiation, etc.) and used as a power supply for electrical circuits is called Energy Harvesting (EH). Harvested energy can be used as the sole power source of the system, or it can be utilized as a partial power source to prolong battery life [4]. Due to the trend of low-power, self-sufficient devices, energy harvesting is frequently implemented as a part of the power management system. Fully integrated IoT devices are especially interesting for energy harvesting since the low-power systems are easier to manufacture on-die, enabling harvested energy to become the main power source. Since the ambiental energy sources typically generate electric signals in a form unsuitable for a power supply (too low and unstable), the central task of the energy harvesting process revolves around the generation of output voltage levels suitable for further usage. The solution for this problem is usually another DC-DC converter with a VCR greater than one (boost DC-DC converter), as shown in Fig 1.13.

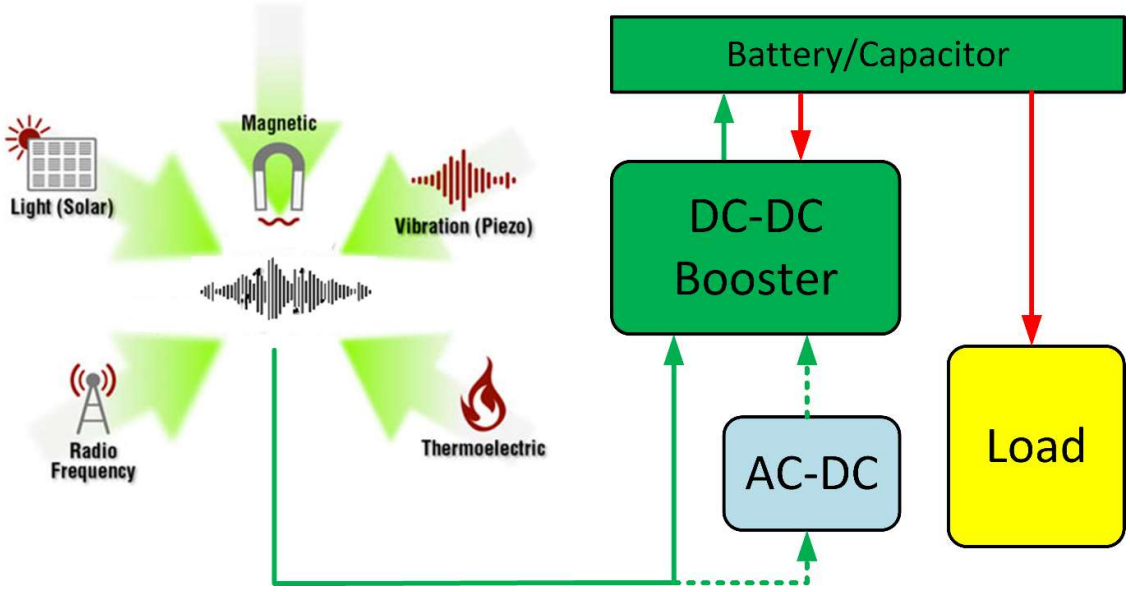


Fig 1.13. Energy Harvesting concept.

In case the harvested signal is AC, such as a radio wave, vibration from a piezoelectric sensor, etc., it must be first rectified and then boosted to the required voltage. Unlike the conventional DC-DC converter, where the power is regulated based on the load current, the DC-DC harvester needs to regulate its power based on the input charge [4]. This way, energy is harvested at maximum efficiency. The output voltage, in this case, is not so critical since it usually connects

to the large capacitor or battery, which makes it stable. The secondary regulation loop could sometimes be implemented to discharge the output node to the battery periodically.

The system can be self-sufficient if the average harvested energy exceeds the circuit's power consumption. However, some form of energy storage is almost always necessary because the harvested signal is unpredictable. Even if the average power consumption is lower than the average harvested power, it could be the opposite at some given moments, which would create system malfunction without energy storage.

Low-Power Clock Generation

A clock generator is an electric circuit that produces a clock signal used to synchronize the other circuits in the system. A clock generator is sometimes also called an oscillator, even though the term 'oscillator' has a wider definition, and some oscillators are unsuitable for producing clock signals (for instance, sine wave oscillator). Several important parameters must be considered to qualify and compare clock generators. In addition to basic parameters like supply voltage range and output frequency range, additional parameters such as power consumption, duty cycle, temperature coefficient, etc., need to be defined. In the field of integrated systems, area becomes an important parameter. Since the clock is used for a large variety of applications, the importance of the specific parameter depends on the application.

Simple power consumption (PC) expressed in Watts might sometimes be misleading since higher-frequency clocks are more likely to have higher power consumption. For that reason, an additional parameter called power efficiency is defined as the ratio of PC and frequency. The unit practical for integrated clock generators is μW/MHz. The same parameter is sometimes referred to as energy efficiency, and the unit used is pJ/cycle (both units are the same in value, μW/MHz = pJ/cycle). Power efficiency is one of the critical parameters for clock generators used in power management since the main purpose of power management is efficient energy usage.

Low-power IoT devices usually operate in standby mode for most of the time. A low activity factor means many sub-systems, including clock generators, must be activated and deactivated frequently. In such a scenario, startup time becomes an important parameter.

A square wave oscillator's duty cycle marks the pulse width (PW) to period (T) ratio. It is usually defined as a percentage or just a number between 0 and 1. A graphical explanation of the duty cycle is provided in Fig. 1.14.

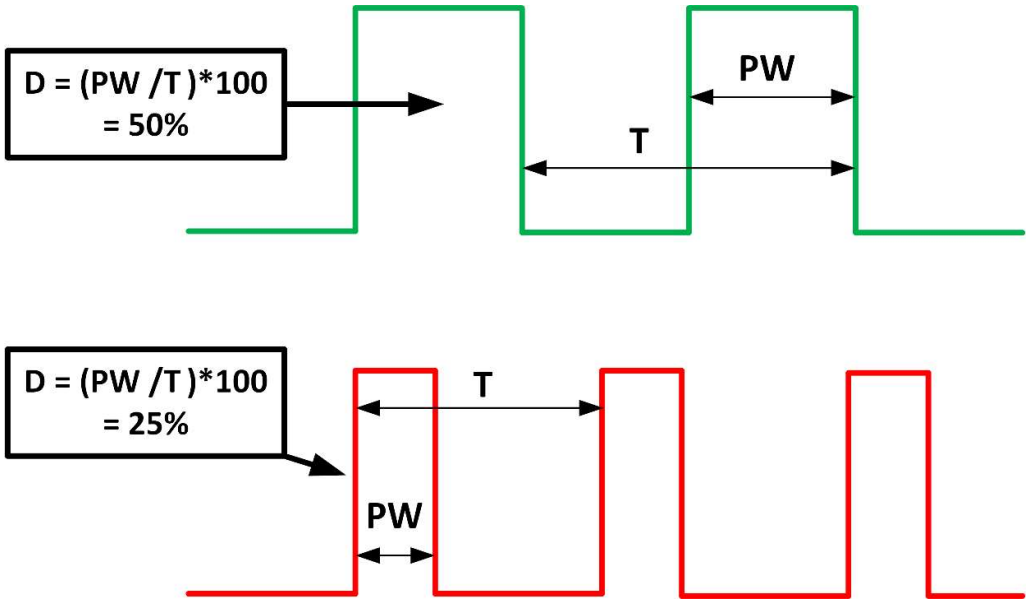


Fig. 1.14. Duty cycle illustration.

Period Jitter is the parameter that describes variations in the clock's period caused by thermal noise and other disturbing factors. It is usually expressed as a peak-to-peak (P2P) variation, RMS, or standard deviation over a large number of samples (10000 typically). Since Period Jitter is a type of noise, RMS can be estimated from peak-to-peak variations as $Jitter_{RMS}=Jitter_{P2P}/8$. It is sometimes useful to present Jitter as a percentage of the clock period so that a comparison between clock generators at different frequencies can be conducted. Figure 1.15 illustrates how peak-to-peak period jitter is measured.

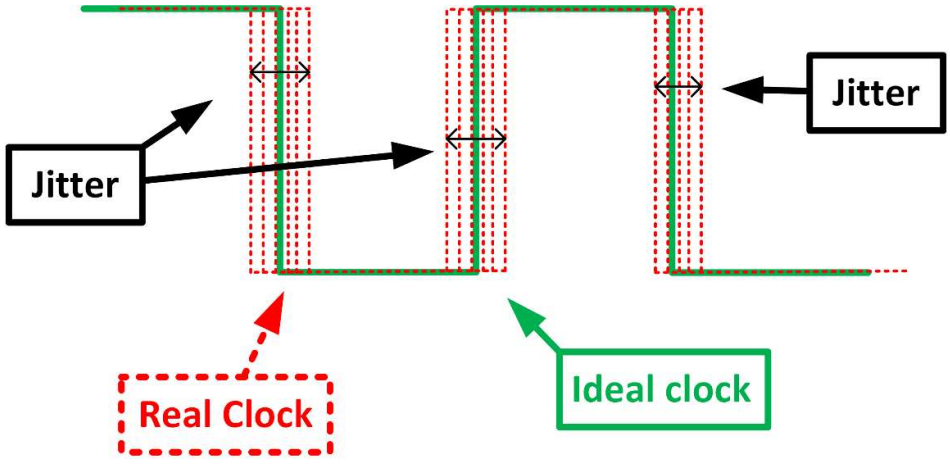


Fig. 1.15. Peak-to-peak period Jitter.

As mentioned before, many parts of the power management system require a clock signal. In some cases, an external clock signal can be used. When dealing with fully integrated battery-

supplied IoT devices, a clock for power management needs to be generated on-die. Since power efficiency is one of the main quality indicators for any power management system, clock generators must function according to that fact. The tradeoff between power consumption and other parameters must be conducted in practice. When designing the clock generator for a power management system, the power consumption is minimized while keeping other parameters (area, duty cycle, jitter, temperature stability, etc.) within the system requirements [4].

Fractional-order elements in power management

In recent decades, fractional-order (FO) systems have emerged in interdisciplinary research as systems of the 21st century capable of representing continuous-time linear systems more efficiently than integer-order (IO) systems [5] [6]. Out of a large variety of applications such as control theory, material theory, diffusion theory, robotics, signal processing, viscoelasticity, etc., FO elements also find their usage in the field of power management. Switching-capacitor DC-DC converter, as an unavoidable part of state-of-the-art power management, has a significant limit of fixed VCR for a given SC Network topology (Table 1.1). Standard switching capacitors are very suitable when input voltage needs to be divided or multiplied by the integer number (VCR= 1, 2, 3, 1/2, 1/3, etc). However, when optimal VCR becomes a fraction that includes non-integer numbers, SC network topology becomes more complicated with an increasing number of switches and capacitors.

The research focused on conventional IO SC DC-DC converters attempted to solve the problem of fixed VCR by introducing the so-called gearbox of SC Networks, as depicted in Fig 1.16 [3]. This approach means that the number of different SC network cores must be implemented in the design, and it still does not provide a smooth transition between different VCRs. A possible solution to this problem might be to introduce a digitally controlled fractional-order capacitor instead of a standard, integer-order capacitor [7] [8]. That way, the transition between neighboring VCRs can be smoother without significant drops in Efficiency.

Even though FO elements provide an elegant and promising solution to this problem, further research needs to be conducted to investigate their value, especially for fully integrated DC-DC converters. Several main aspects of already existing FO systems need to be improved to make them suitable for DC-DC converters: power consumption, speed, and frequency range. Power consumption is especially critical since the FO capacitor is usually implemented with active components that consume current.

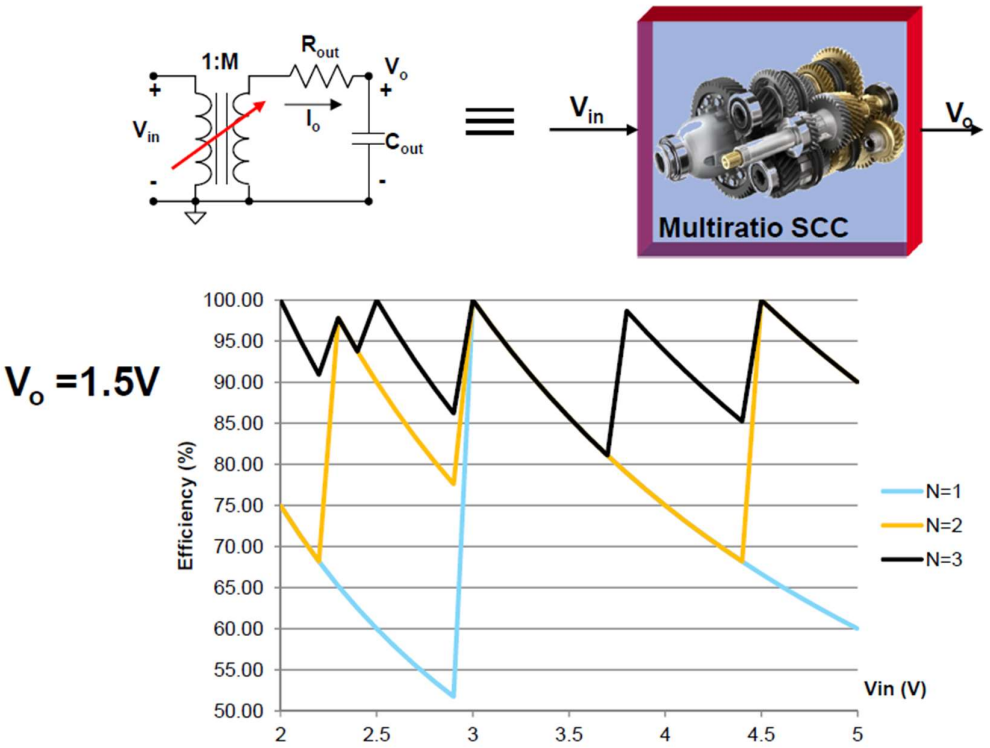


Fig. 1.16. Switching capacitor gearbox.

Prior Art and Motivation

The prior art study concerning integrated power management shows that low-power areas are particularly challenging for achieving high energy efficiency, speed, and power density. The reason for that is a limited amount of available power that needs to be distributed amongst the subcircuits responsible for performing various tasks. A graphical presentation of the prior-art integrated DC-DC converters shows a very limited amount of research papers for sub-mW power. (Fig. 1.13, and Fig 1.14) [9].

Further analysis shows that the presented low-power DC-DC converters have problems with low efficiency, low power density, and slow transient response. They also often require a large decoupling capacitor at the output.

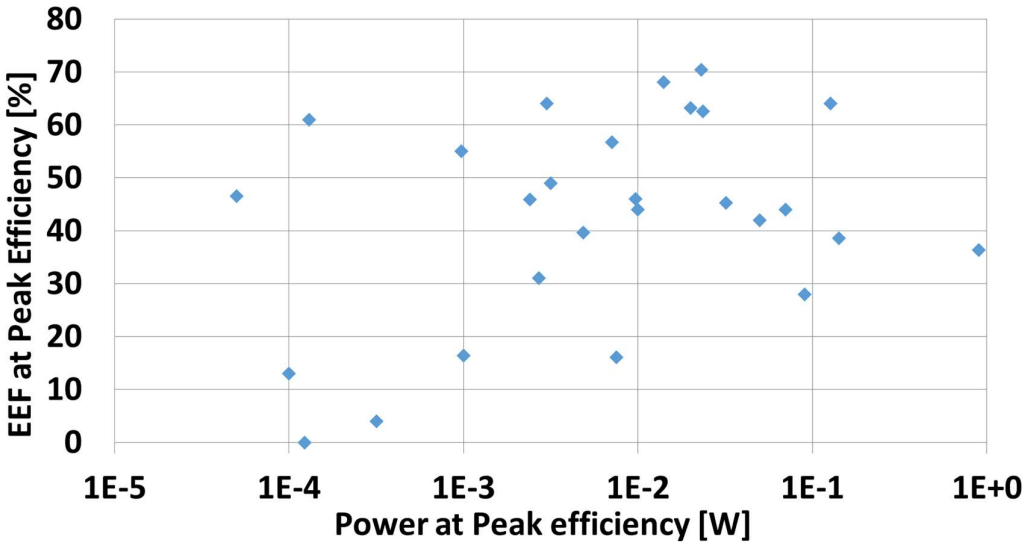


Fig. 1.13. Prior-art integrated switched-capacitor DC-DC converters - EEF.

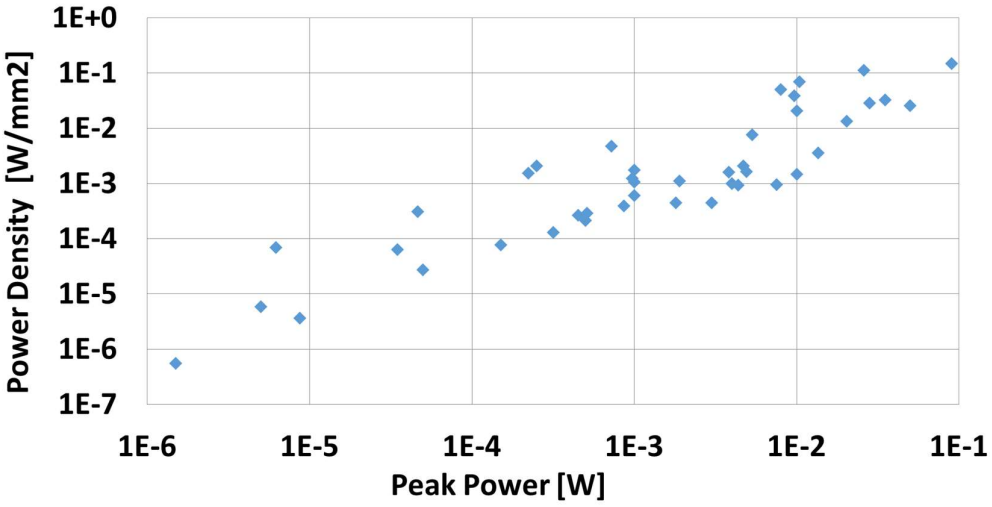


Fig. 1.14. Prior-art integrated switched-capacitor DC-DC converters – Power Density.

The main focus of this PhD thesis is to improve power management in areas of energy efficiency and speed by introducing novel integrated circuits and techniques. For research purposes, four distinct fully integrated systems were designed, and the results were published in the form of 1 conference paper and 3 journal papers, with 2 additional publications expected in the future:

(1) D. Zagouri*, A. Rimer*, **E. Emanović***, Y. Ninio*, Y. Slezak, D. Jurišić, A. Fish, and J. Shor, "A Photovoltaic Energy Harvester/Image Sensor Platform With Event Detection Capability in 180 nm," in IEEE Solid-State Circuits Letters, vol. 7, pp. 62-65, 2024. *Authors with equal contribution [4].

(2) **E. Emanović**, J. Shor and D. Jurišić, "An Inverter-Based, Ultra-Low Power, Fully Integrated, Switched-Capacitor DC-DC Buck Converter," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 359-362 [10].

(3) **E. Emanović**, D. Jurišić, J. Shor, "An Inverter-Based, Ultra-Low Power, Fully Integrated, Switched-Capacitor DC-DC Buck Converter," in IEEE Access [11].

(4) E. Emanović, M. Vonić, D. Jurišić, C. Psychalinos, "Digitally Controlled Fractional-Order Elements Using OTA-C Structures," Electronics. 2024; 13(11):2066 [12].

(5) **Expected additional publication:** "Boost DC-DC converter as part of the Image sensing platform" as an extension of the system paper [4].

(6) **Expected additional publication:** "Temperature compensated low-power clock generator as part of the Image sensing platform" as an extension of the system paper [4].

Chapter 2 describes a step-down (buck) DC-DC converter fabricated in TSMC 65nm and published as a conference paper [10] with an extended journal version [11]. A boost DC-DC converter fabricated in TSMC 180nm as part of the image-sensing platform published as a journal paper [4] is presented in Chapter 3. A low-power clock generator (as part of the same image-sensing platform [4]) is illustrated in Chapter 4. An additional contribution to the area of fully integrated power management was implemented in the form of a digitally controlled fractional-order capacitor, designed in AMS 350nm, published as a journal paper [12], and described in Chapter 5.

2. SWITCHED-CAPACITOR DC-DC BUCK CONVERTER

Introduction

Internet-of-Things (IoT) devices at the edge are required to operate at ultra-low average power levels of 10's of μW and lower [13]. To conserve power, IoT chips operate at a very low activity factor in most of the computing circuits. However, always-on circuits, such as wakeup circuits, reference voltages, real-time clocks, and digital circuits controlling them, can be a dominant energy consumer in the system despite the fact they are low-power. The main voltage regulators of the IC active circuits may have very poor efficiency at such light loads. Although a Low-Drop-Out linear regulator (LDO) could sometimes be utilized for such low powers, the main limitation lies in the fact that the LDO's efficiency is limited by the ratio of output and input voltages. Therefore, an efficient on-die DC-to-DC converter is essential to regulate the power of the battery voltage for these low-power domains. In always-on applications, digital domains operate at or near the threshold voltage (V_{th}), typically 0.5-0.6V, while analog circuits require higher voltages (1.2-1.8V). Research works on on-die switched capacitor DC-DC converters in the 10-100μW domain are limited [1], [13], [14], [15], [16], [17]. In the low-voltage domain, the speed of the DC-DC converter is crucial because any voltage droop caused by current surges can affect digital speed paths.

This chapter describes a switched capacitor DC-DC converter for low power always-on domains, and it is an extension of the work reported in [10]. An inverter-based amplifier was used for loop regulation due to its low-power, high-speed nature, which limited droops and overshoots during load transients. Additionally, the fast regulation loop enables the circuit to operate even with an output capacitance as low as 50 pF. The DC-DC converter operates at battery voltage levels, V_{bat} of 2.5-3 V. The main output voltage (V_{out}=0.55V nominally) is generated for the digital circuitry, as well as intermediate voltage levels (VDD_1=1.8V and VDD_2=1.2V), which can be utilized for analog circuits. Combining several analog techniques (counter-phase cores, floating well circuit, and multi-level clocking) with a novel way of output voltage detection (inverter-based comparator) the proposed topology was able to achieve contribution in terms of EEF and Power Density. Additionally, a very fast transient response was accomplished.

Architecture and Circuit Design

Control Loop and Clock Generation

Figure 2.1 illustrates a simplified block diagram of the DC-DC converter. V_{out} is monitored by

an inverter-based comparator, which generates a rising edge when it detects that $V_{out} < V_{ref}$. Simulated waveforms of V_{out} and comparator output (V_1) are shown in Fig. 2.2(a) and Fig. 2.2(b) respectively, where output current (I_{out}) is set to 50µA. This rising edge changes the output state of the T-flip-flop (V_2), as shown in Fig 2.2(c), and the clock signal is level-shifted and fed into the dual-core Switched-Capacitor (SC) network (Vtp represents the trip point of the inverter used as a comparator). The SC network operates using clocks at three different voltage levels (L1, L2, and L3) for switching purposes. When the rising or falling edge of the clock triggers the SC network, a new package of charge is delivered to V_{out}, which elevates it above V_{ref}, thus resetting the V_1. A Watchdog circuit is included as a failsafe feature, which could also serve as a startup mechanism and is in standby mode during regular DC-DC operation, consuming only 135 nW. If a malfunction is detected, such as overcurrent, the watchdog kicks in and restarts the whole system. Since the DC-DC converter requires internally generated intermediate voltage levels (1.2 and 1.8 V), the reset signal generates the required voltages as needed.

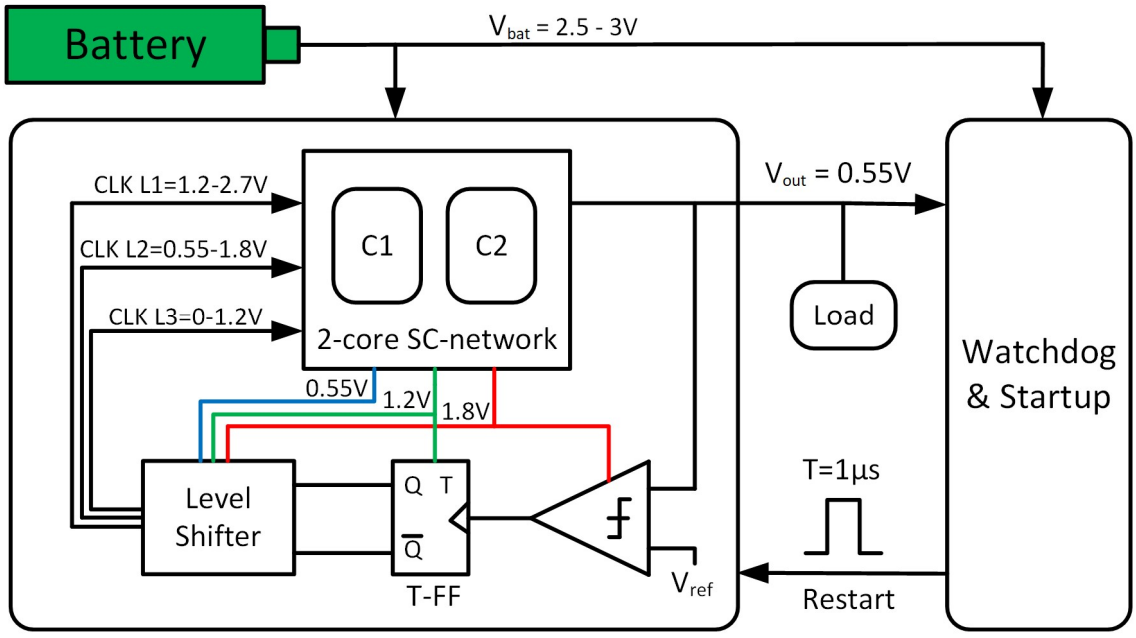


Fig. 2.1. Block diagram.

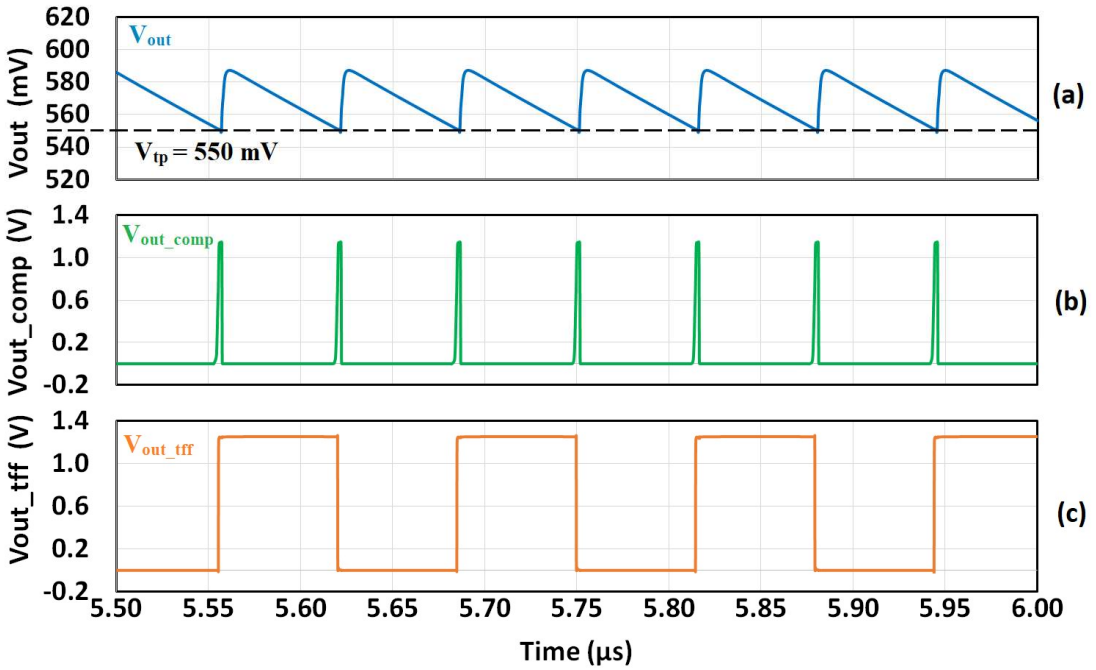


Fig. 2.2. Simulated waveforms of the clock generation mechanism at nominal conditions and I_{out}= 50uA. (a) V_{out}, (b) V_1, (c) V_2.

Switched-Capacitor Network

The architecture utilized to achieve the necessary Voltage-Conversion-Ratio (VCR) is a dual-core Ladder-Star [3] (also known as Dickson or Dickson Star [18]), as illustrated in Fig. 2.3. Each core's flying capacitors (C_{fly}) comprise three 5pF Metal-Insulator-Metal capacitors (MIMCAP). The two cores operate at opposite clock phases, which enables lower ripple and provides access to intermediate voltage levels. Internal voltages of the one core (V_{x0}, V_{x1}, and V_{x2}) are shown in Fig. 2.4. Since the second core's internal voltages are the same in every aspect except the opposite phase, a floating well circuit (Fig. 2.5) can be used for intermediate voltage generation in accordance with the following equations: $VDD_1 = \max(V_{x1},V_{y1})$, $VDD_2 = \max(V_{x2},V_{y2})$. The voltage supplies, VDD_1 (~1.8V) and VDD_2 (~1.2V), are produced by providing the opposite-phase internal voltages (V_{x1}, V_{x2}, V_{y1}, and V_{y2}) to the intermediate voltage generation circuit. A waveform of VDD_1, generated from V_{x1} and V_{y1}, is presented in Fig. 2.6 as an example. VDD_2 is generated in a similar manner. The intermediate voltages, along with the main output voltage (V_{out}), are employed for generating three distinct clock-voltage levels that are applied to the corresponding NMOS and PMOS switches (see Fig. 2.7).

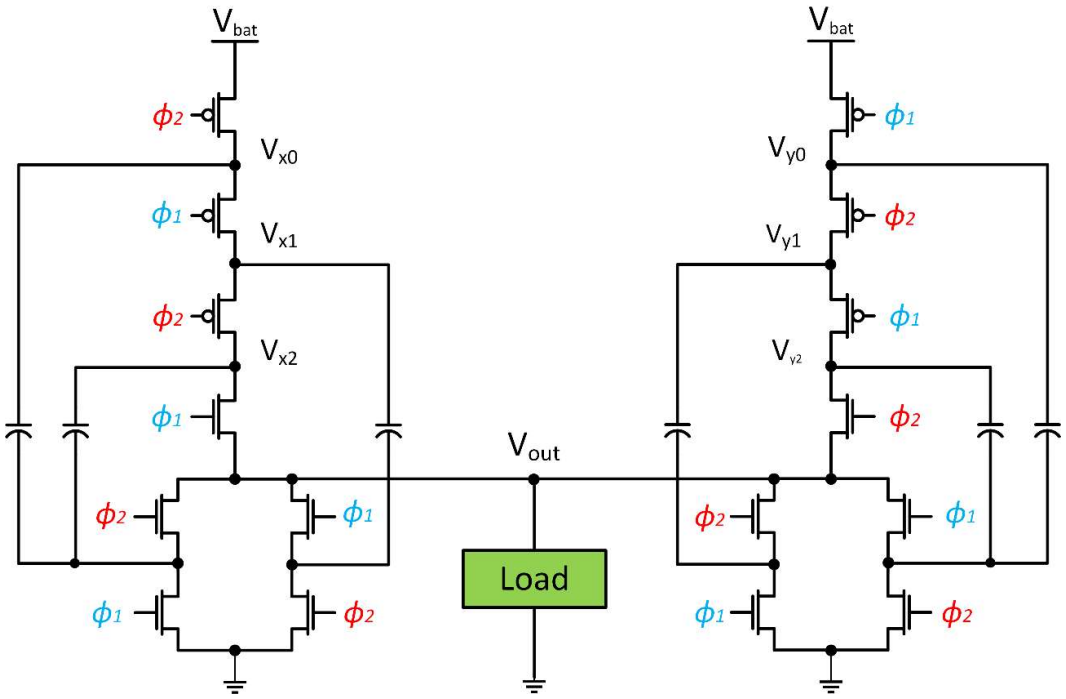


Fig. 2.3. Two core Ladder-Star architecture.

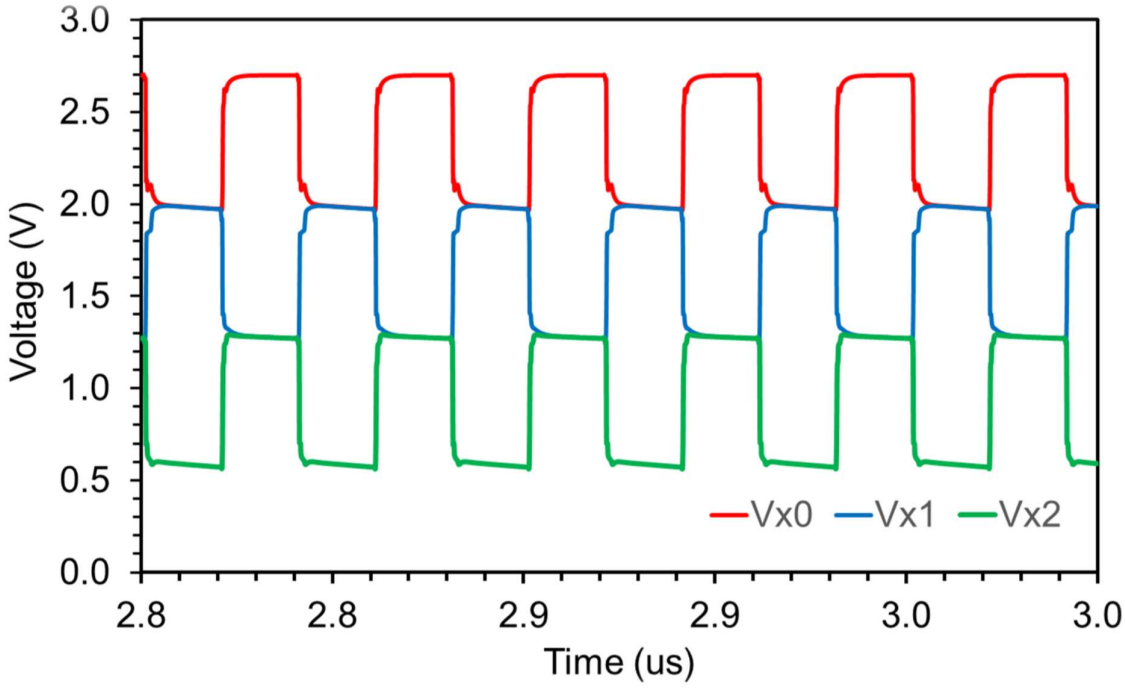


Fig. 2.4. Simulated waveforms of one bank at a 130uA load.

The signal V_2 is first level shifted up to the battery voltage level (V_{bat} = 2.7V). After that, in order to reduce the charging losses, the clock signal is driven into three buffers which charge

the stages L3, L2, and L1 from 0 to 1.2V, 0.6V to 1.8V, and 1.2V to 2.7V respectively. Thus, each stage in the DC-DC can be driven to exactly the voltage required for the conversion. A detailed illustration of both DC-DC cores including the intermediate voltage generation and clock levels used for each stage is shown in Fig. 2.8. Note that each switch is toggled between its required minimum and maximum voltage levels.

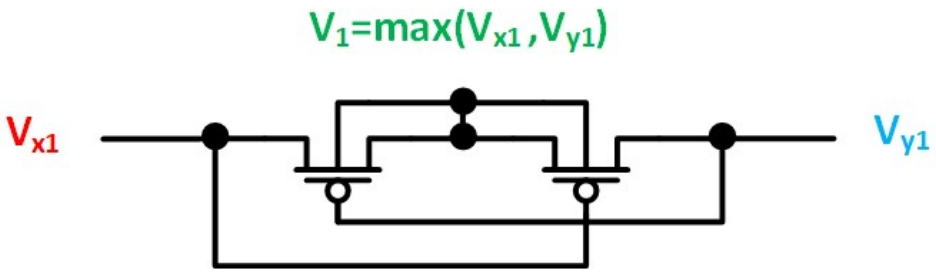


Fig. 2.5. Intermediate voltage generator.

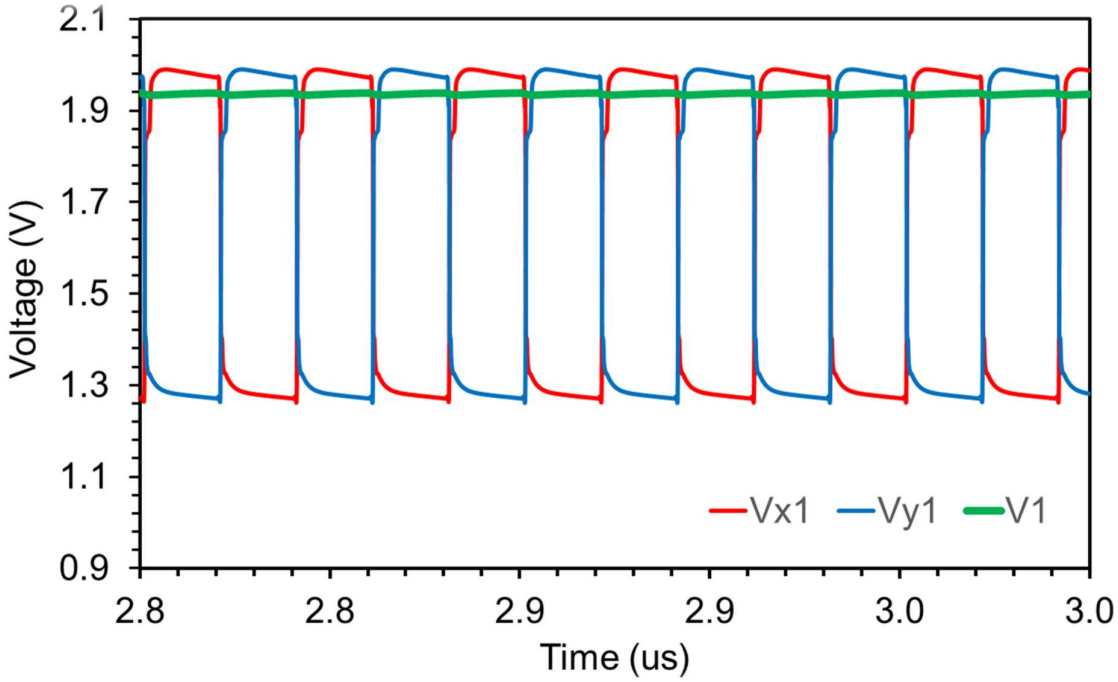


Fig. 2.6. Simulated waveforms of the intermediate voltage generator.

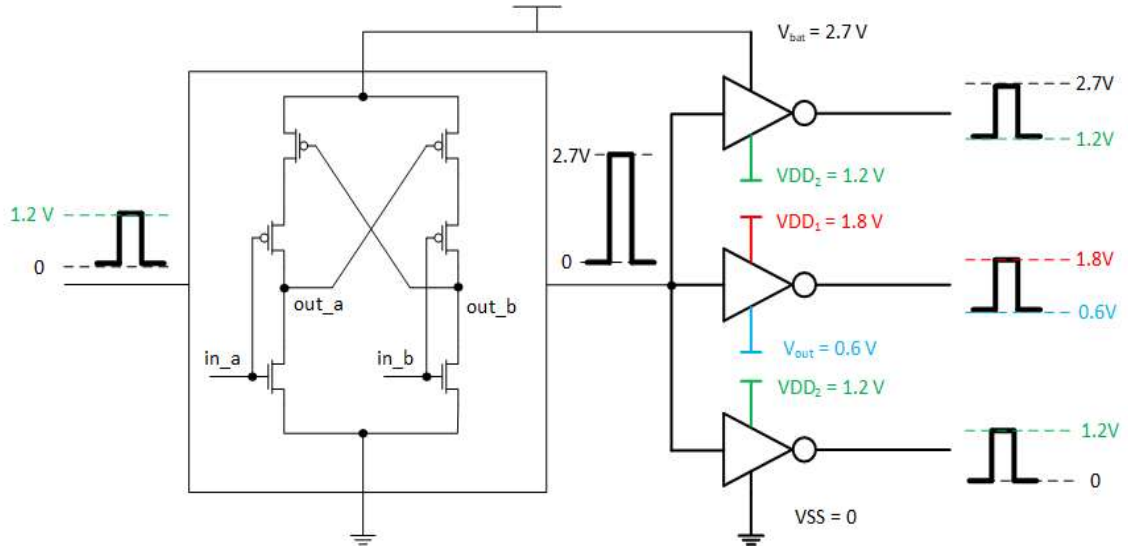


Fig. 2.7. Level shifting concept.

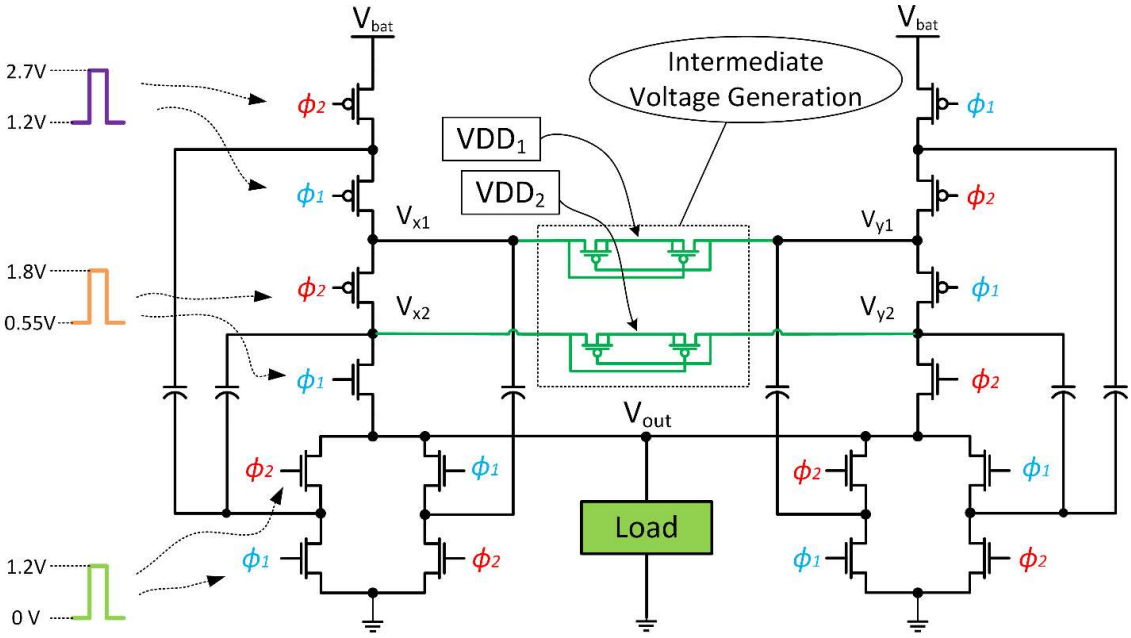


Fig. 2.8. Two core Ladder-Star with intermediate voltages and clock voltage levels.

Inverter-based Comparator

Inverter-based amplifiers are commonly used for their high-speed and low-power properties. However, they are subject to issues such as process-dependence and supply-voltage-dependent trip points. Despite these challenges, an inverter-based amplifier can be implemented as an efficient comparator if its disadvantages can be overcome. To address this, the supply voltage

(V_{dd_inv}) of the inverter is regulated such that its trip point is always at a fixed voltage level, as depicted in Fig. 2.9a. The voltage reference (V_{ref}) is supplied to the input of the Unity Gain Buffer (UGB), whose output is utilized as the supply voltage for the inverter. Therefore, the trip point of the inverter (V_{tp}) is approximately $V_{ref}/2$, based on the ratio of the NMOS and PMOS. The control loop causes V_{out} to track V_{tp}, and fine-tuning of V_{ref} enables digital control of the output voltage. This feature can be accomplished with trimmable subthreshold reference voltage circuits that consume nW or sub-nW level power, such as the 2T based reference in [19], which can operate directly off V_{bat}. It can be observed that the inverter, when used as an analog circuit, has a bandwidth of 363 MHz (Fig. 2.9b) which enables a very fast response to the transient load changes. The V_{tp} point is nearly temperature independent, as seen in simulations (Fig. 2.10). Since the UGB does not require very high-speed operation, it can function with very low bias currents (~1.4 μA).

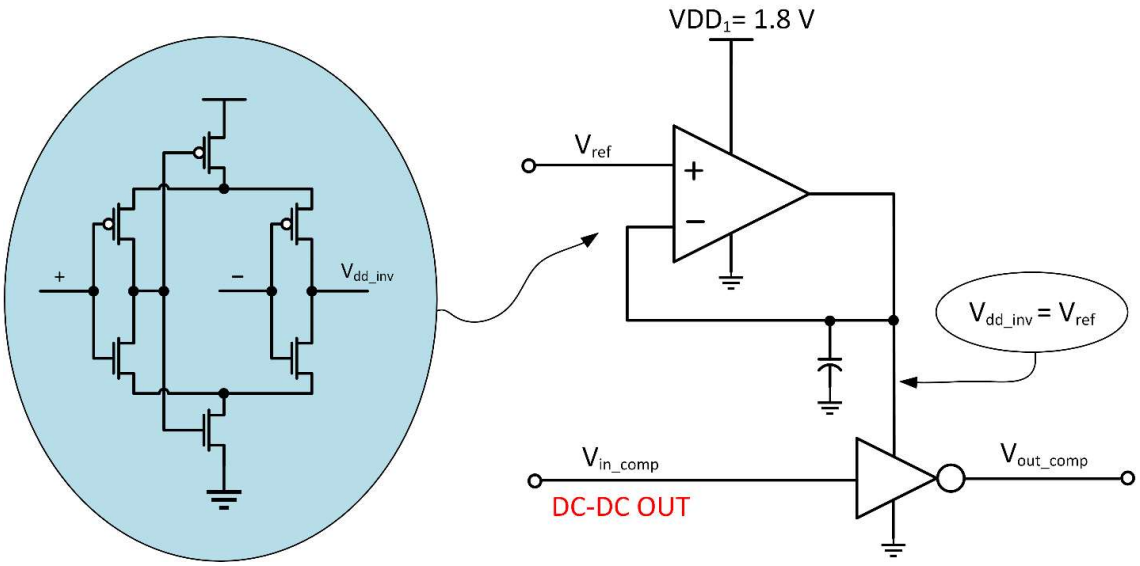


Fig. 2.9a. Comparator with UGB.

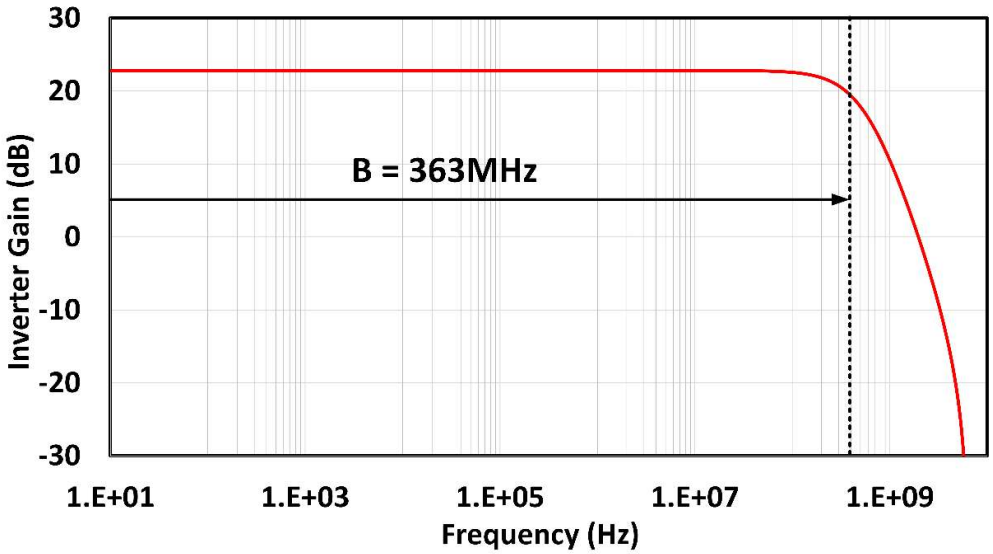


Fig. 2.9b. Inverter Bandwidth.

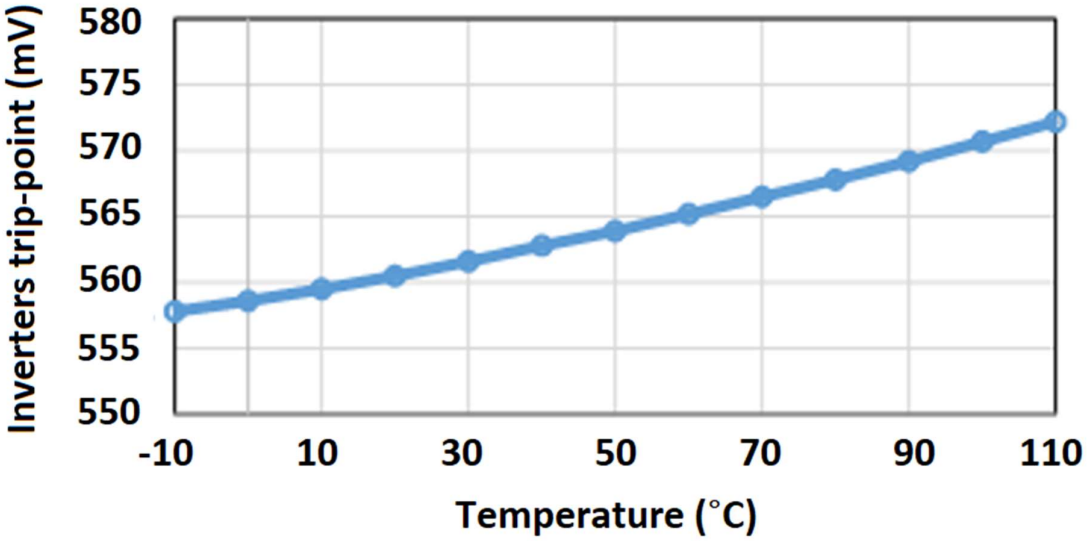


Fig. 2.10. Inverter trip-point vs Temperature.

Watchdog Mechanism

A Watchdog mechanism was designed to reset the DC-DC converter in case of malfunction caused by overvoltage and excessive current, but it could be utilized also as a trigger for the startup mechanism. A startup circuit using a resistor divider between V_{bat} and VSS, as depicted in Fig. 2.11, is used to initialize VDD_1, VDD_2, and V_{out}, and it could be enabled by the external startup pulse or by the watchdog pulse. The simplicity of the circuit provides a great level of reliability and robustness since the functions of reset and startup are crucial parts of the circuit's

normal operation as well as the fail-safe mechanism. In order to secure the required voltage levels (VDD_1, VDD_2, and V_{out}), the startup circuit needs to be enabled for roughly 1µs. Thus, the required length of the reset pulse is generated with the Watchdog circuit as illustrated in Fig. 2.12. Inverter I_1 has a lower trip point than V_{tp} (Fig. 2.9) and is thus used to detect a situation where V_{out} is too low. The supply of I_1 is generated by weak PMOS devices P_1-P_4 which operate off Vbat. Digital inputs $Trim_1$ and $Trim_2$, determine the voltage level at which a malfunction may be detected. If the DC-DC converter operates normally, V_{out} will be above this trip point, and the watchdog will consume minimal power. However, if V_{out} drops too low, a rising edge at node n_1 is generated, which is level-shifted to the battery voltage level at node n_2 and fed to the Edge-Triggered-Pulse-Generator (ETPG) that generates a restart pulse (T=1µs). The restart pulse sets the voltage levels at the DC-DC core back to the normal range, resulting in falling edges at nodes n_1 and n_2. If the malfunction is due to a temporary glitch or current spike, the DC-DC converter will continue to operate normally. The Edge-Triggered-Pulse-Generator is shown in Fig. 2.13.

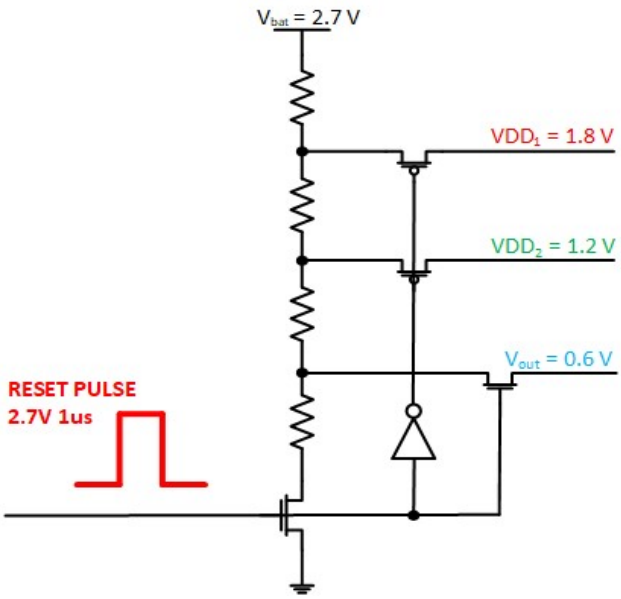


Fig. 2.11. Startup circuit.

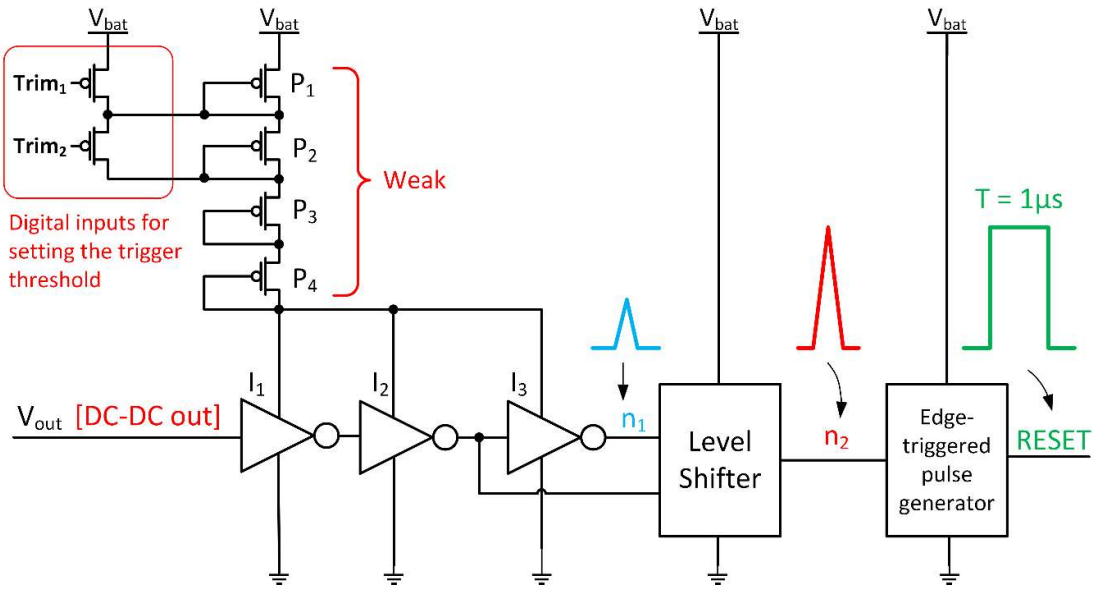


Fig. 2.12. Watchdog circuit.

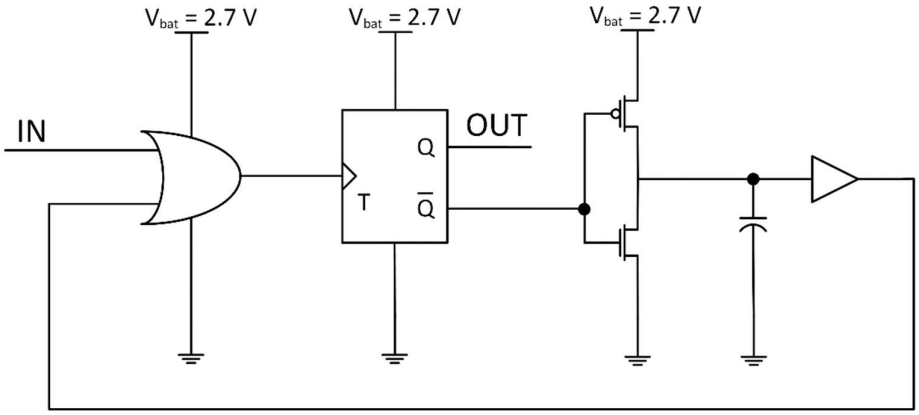


Figure 2.13. Edge-triggered pulse generator.

Internal load setup

In order to measure the parameters of the DC-DC converter in an environment that is as close as possible to realistic operating circumstances, an internal load circuit (Fig. 2.14) was implemented on silicon next to the DC-DC converter. This setup enabled measurement of circuit operation with load capacitance as low as 50pF (including the oscilloscope probe). It also has a tunable resistor load across the required current range and enables a fast internal current transient. This internal current step could be much quicker than an external step, which would be strongly affected by any parasitic package inductances and capacitors.

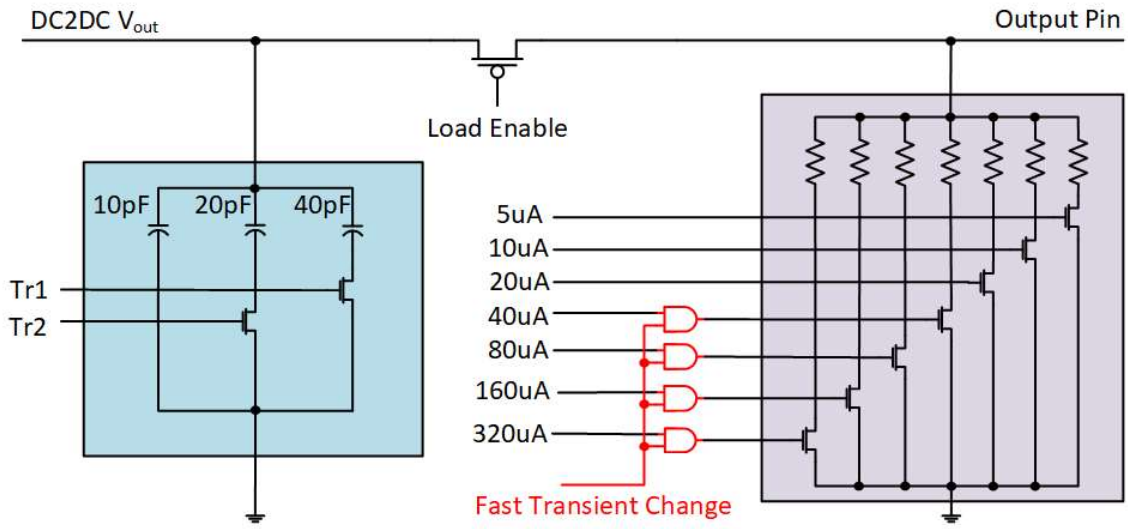


Figure 2.14. Internal load setup.

Simulated Results

Due to the complexity of the whole system and the limited capabilities of silicon measurements in different corners, the simulation results represent an important aspect for performance analysis. The results of the transient analysis, that simultaneously depict the Vout, Iout, as well as other relevant waveforms, are presented in Fig. 2.15a, Fig. 2.15b, and Fig 2.16. A fast response without voltage droops or overshoots can be observed in cases of fast transient load change (Fig. 15a and Fig. 15b). Figure 15b presents waveforms of signals relevant to the speedy transient response (Vout, Iout, Comparator output, and T-flipflop output) right around the moment of transient load change. It can be observed that the response from the comparator takes only 7.1ns from the load change (due to the inverter's high bandwidth). The pulse from the comparator results in an almost immediate change in the clock frequency which enables output voltage to spike up 9ns after load change, thus, preventing voltage droop or malfunction. A dashed red line presents a slope of Vout in case of delayed response from the comparator.

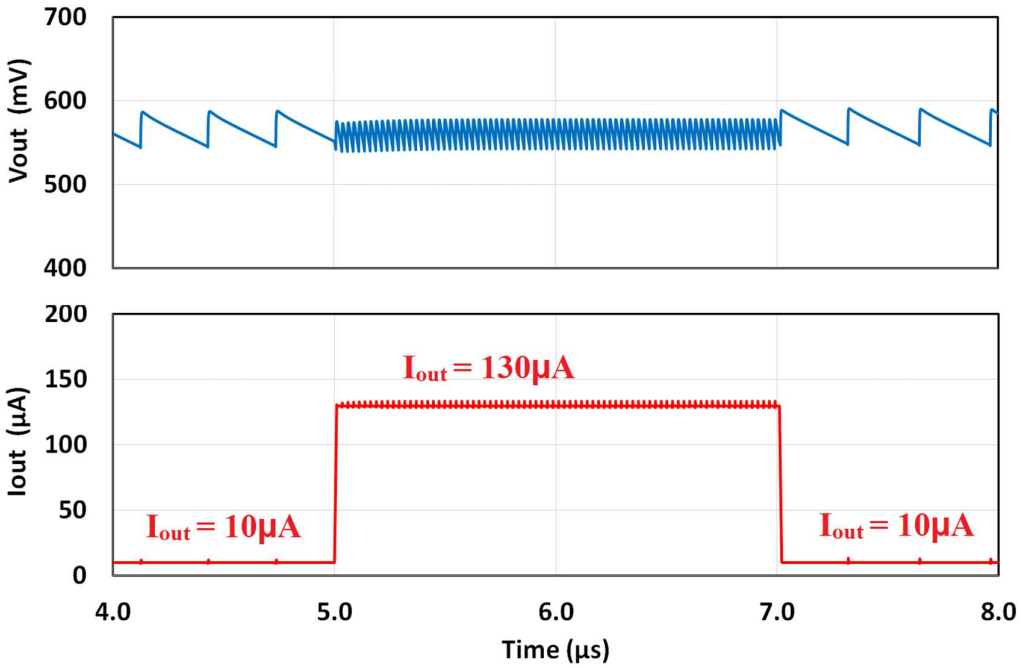


Fig. 2.15a. Simulated transient load.

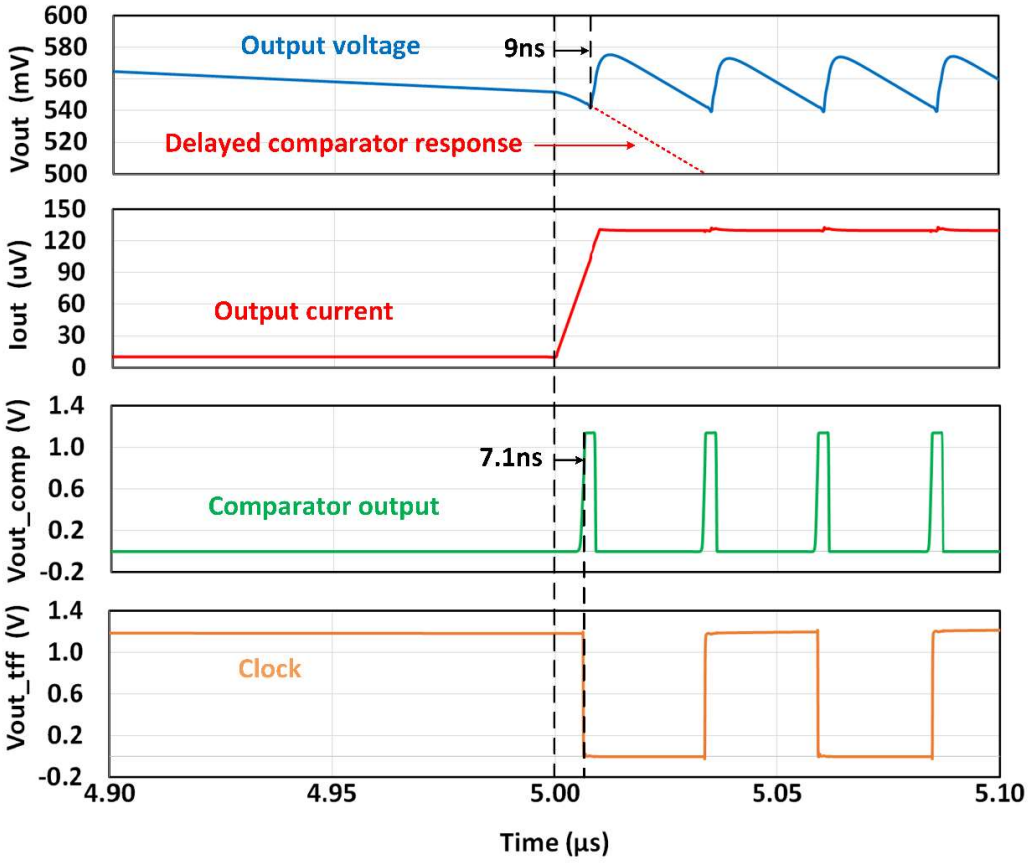


Fig. 2.15b. Relevant waves in the moment of transient load change.

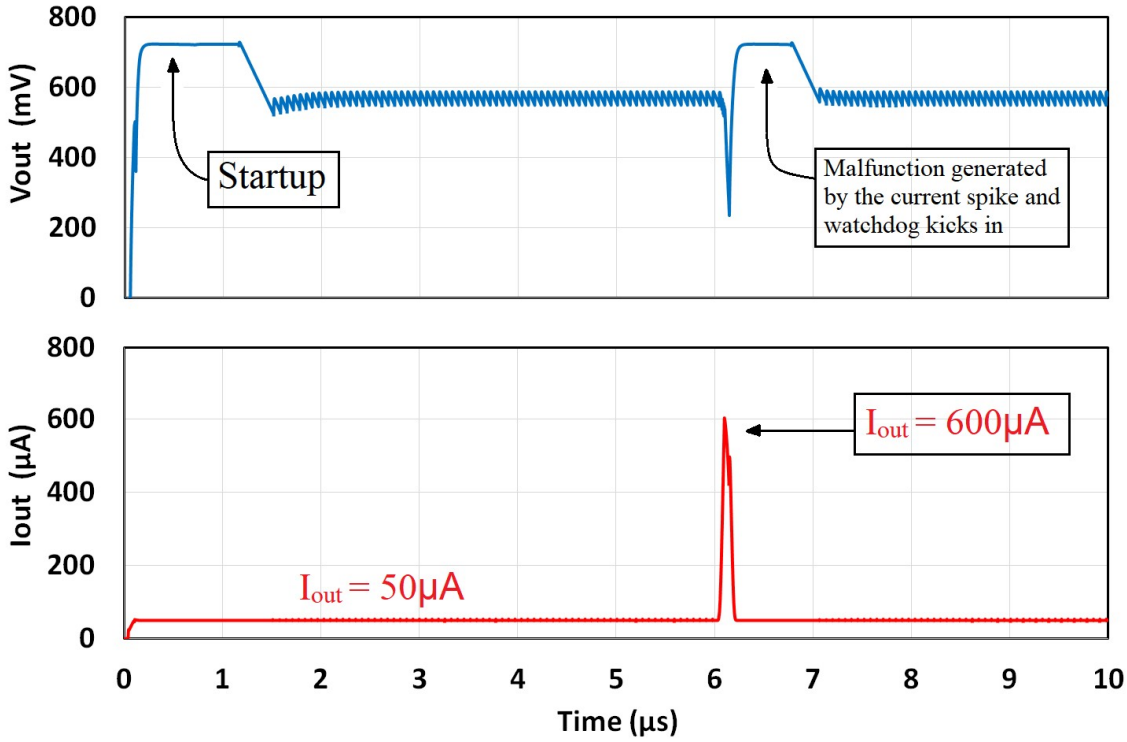


Fig. 2.16. Simulated startup and Watchdog kick-in.

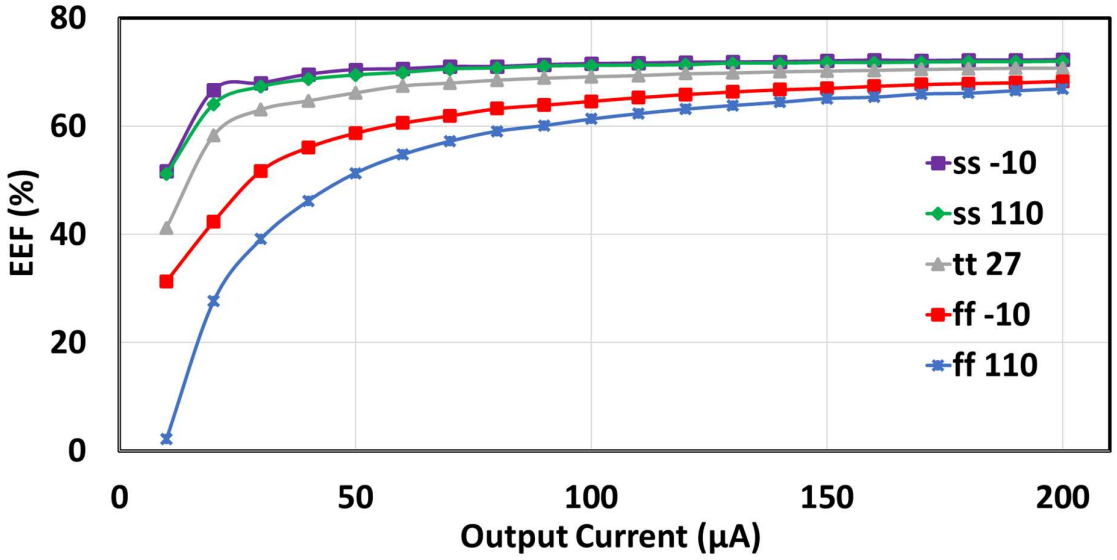


Fig. 2.17. Measured EEF vs I_{out} at V_{in} = 2.7V, nominal and extreme (ss -10 ss 110, ff -10, ff 110)

Figure 2.17 shows simulated extreme cases of the EEF dependence on the I_{out} (process corners combined with extreme temperatures). As expected, a certain drop of efficiency goes with the

fast corner due to the leaky MOSFET switches. It can be observed that even for the worst-case scenario (ff, T=110 °C), the DC-DC converter can be efficiently utilized over the entire operating range as indicated by the positive EEF.

Figures 2.18-2.20 show Monte Carlo variations (process and mismatch) on Efficiency, EEF, and V_{out} for nominal circumstances and I_{out}=160µA. Both Efficiency and EEF have very low dispersion with standard deviations equaling 1.03% and 0.49% respectively. Even though V_{out} shows a slightly larger standard deviation of 16.94 mV, it does not represent the problem since it can be canceled by the trimmable V_{ref}.

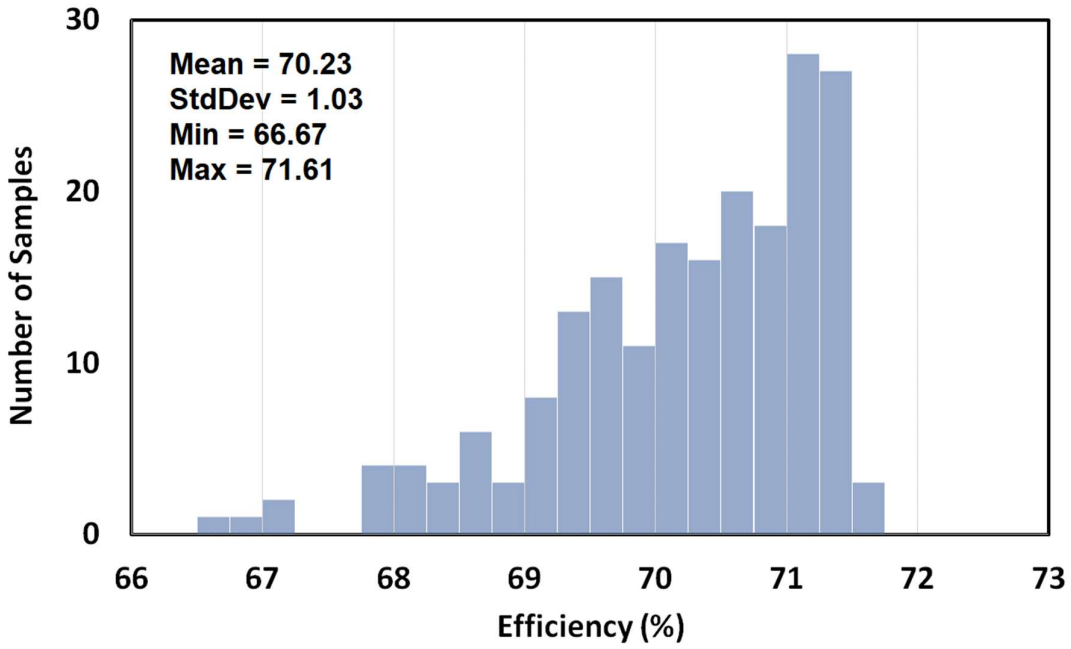


Figure 2.18. Monte Carlo Efficiency at I_{out} = 160µA, 200 samples.

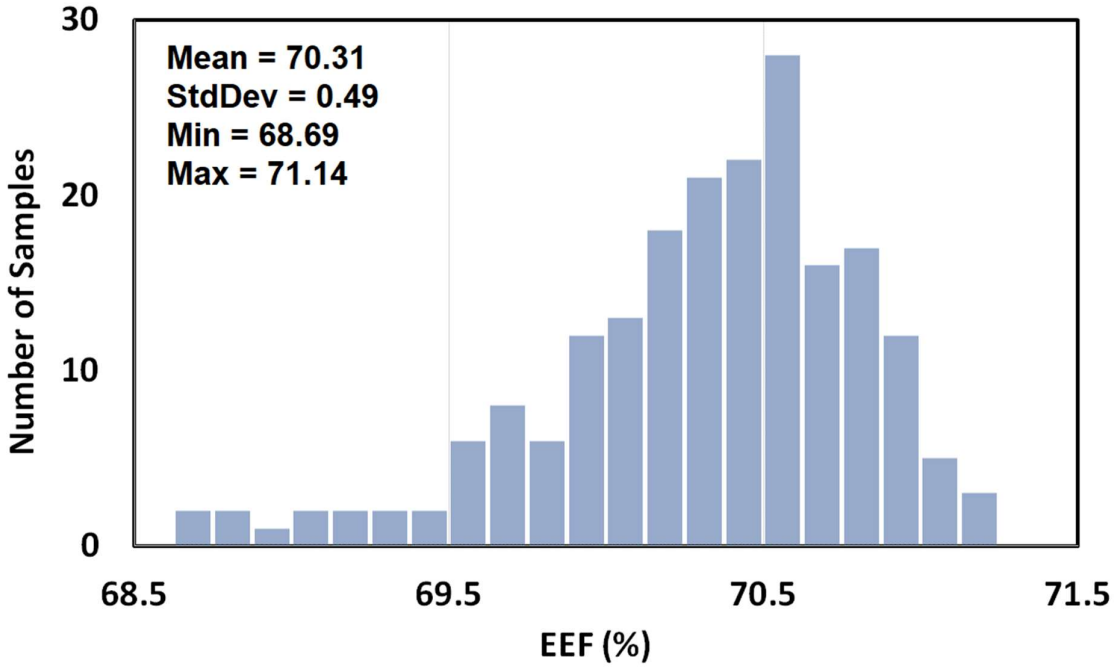


Fig. 2.19. Monte Carlo EEF at I_{out} = 160µA, 200 samples.

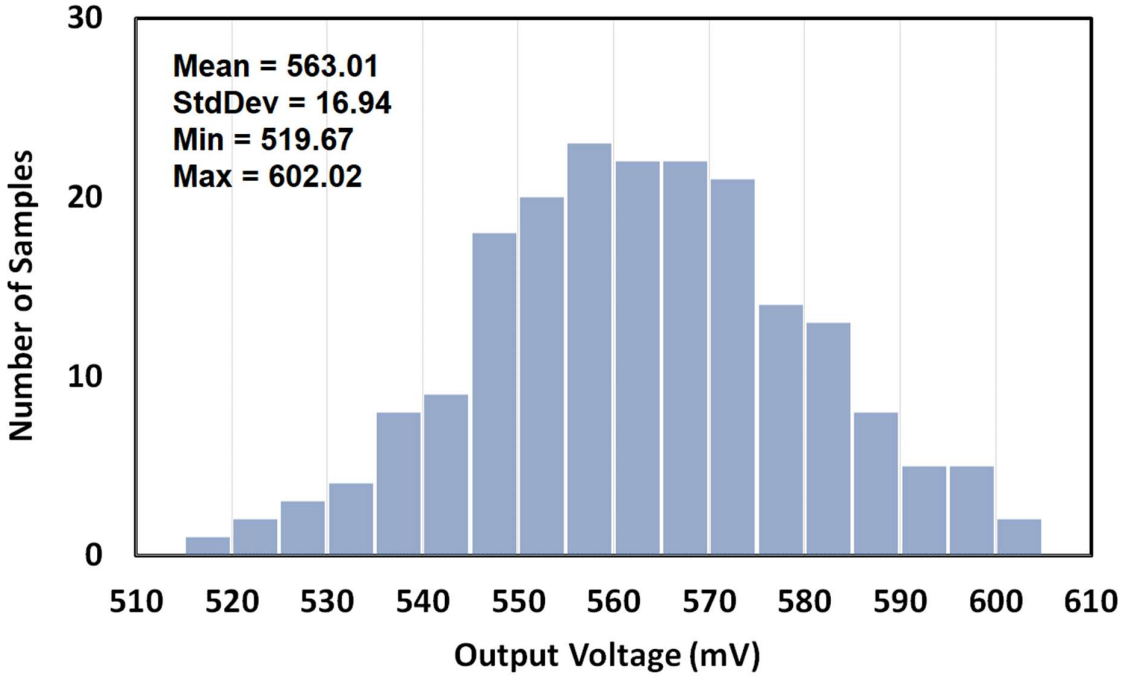


Fig. 2.20. Monte Carlo V_{out} at I_{out} = 160µA, 200 samples.

The energy consumption by the individual sub-circuits is analyzed for two different scenarios, minimum power (Fig. 2.21(a)) and maximum power (Fig. 2.21(b)). The results show that the dominant energy consumer for both scenarios is the switched capacitor network, which is

another indicator of the relatively consistent efficiency over the entire operating range. The main difference between minimum and maximum power in energy consumption contribution can be observed in Comparator and Level Shifter. This happens since the Comparator has power consumers that are not dependent on the clock frequency. For low-current converters, the overhead circuits contribute a larger percentage of the total power budget, as compared to high-power converters. This is why the efficiency and EEF are reduced at very low output currents (see Fig 17).

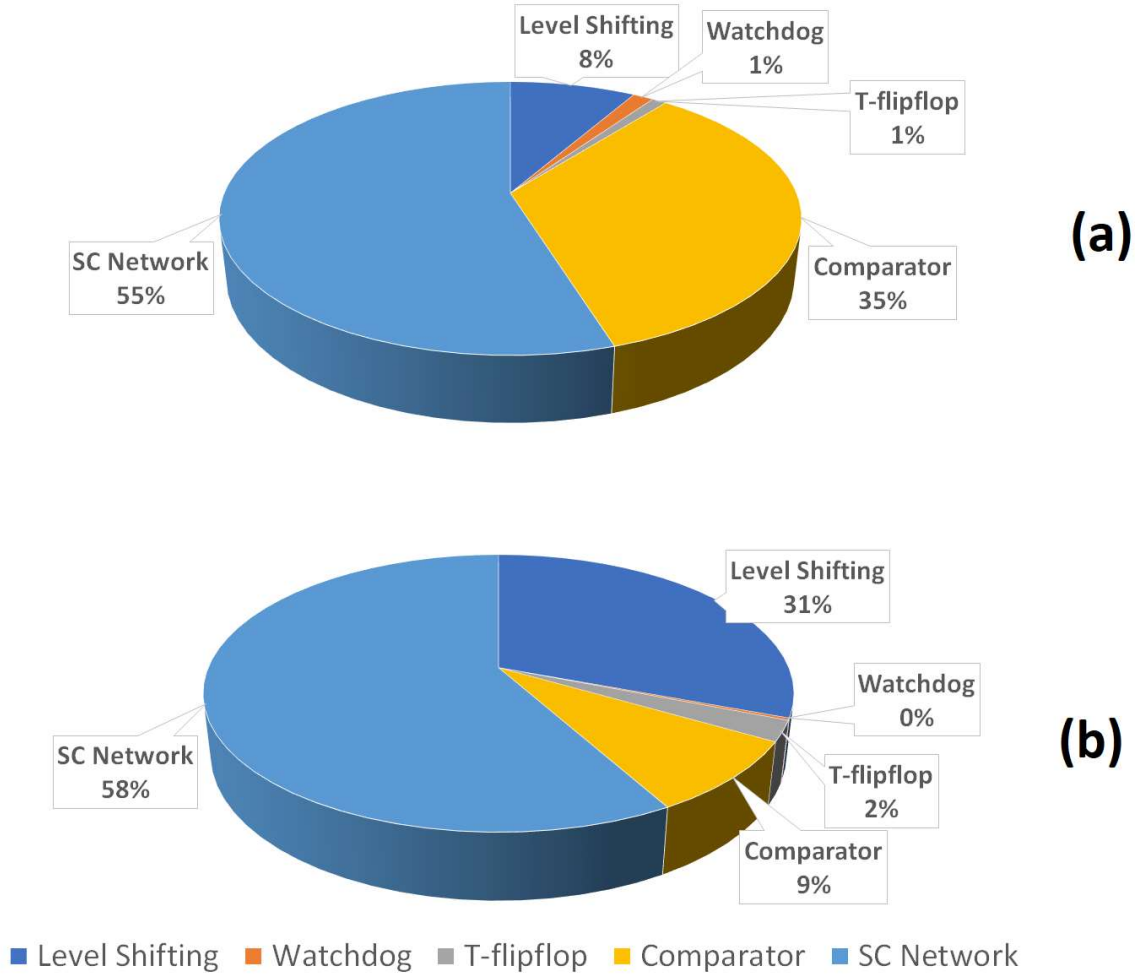


Fig. 2.21. Simulated sub-circuit energy consumption at P_{min} (a) and P_{max} (b).

Measured Results

The DC-DC converter was fabricated using TSMC's 65nm technology node. In Fig. 2.22, the measured efficiency as a function of output current (I_{out}) is presented for a nominal output

voltage of V_{out}=0.55V. The efficiency exhibits a peak value of 62% at the maximum I_{out} and remains close to the peak value over most of the operating range.

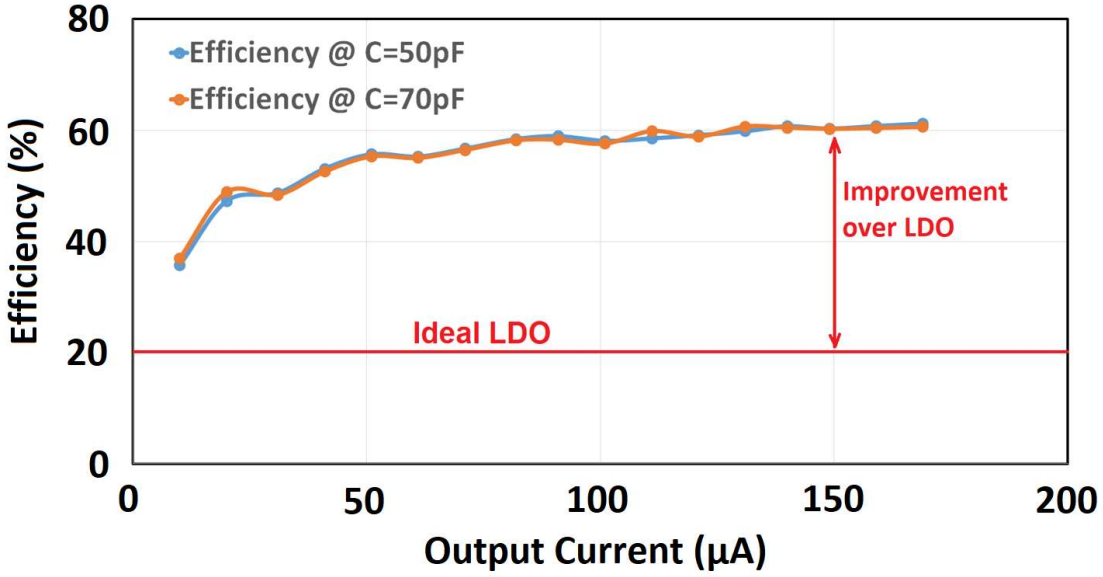


Fig. 2.22. Measured Efficiency vs. I_{out}.

The relationship between the energy efficiency factor (EEF) and I_{out} is illustrated in Fig. 2.23, and it also displays good consistency over the range. The nearly linear dependence of the clock frequency on I_{out} (Fig. 2.24) enables relatively high efficiency and EEF over the range. The V_{out} ripple is plotted against the output current in Fig. 2.25, assuming an output capacitance of 50 pF. Figure 2.26 shows the DC level of V_{out} versus I_{out}. A DC load line of 37.5 mV is observed over the entire operating range which is mainly associated with the delay of the boosting after the comparator's trip. The ripple difference between light and heavy loads also contributes to the DC load-line to some extent since the regulated value is not a DC component of the V_{out} but the minimum V_{out}. In Fig. 2.27(a), the transient response of the converter is depicted as the current is suddenly changed from 10uA to 130uA and back to 10uA. Due to the fast speed of the inverter-comparator, no droops or overshoots are observed, despite the small Cout. A DC load-line of 27 mV can be observed here as well. The activation of the watchdog circuit during an overcurrent event is also shown in Fig. 2.27(b). After approximately 1µs of reset time, the DC-DC converter resumes normal operation. Figure 2.27(c) represents the silicon die photo with corresponding dimensions and the DC-DC converter's location.

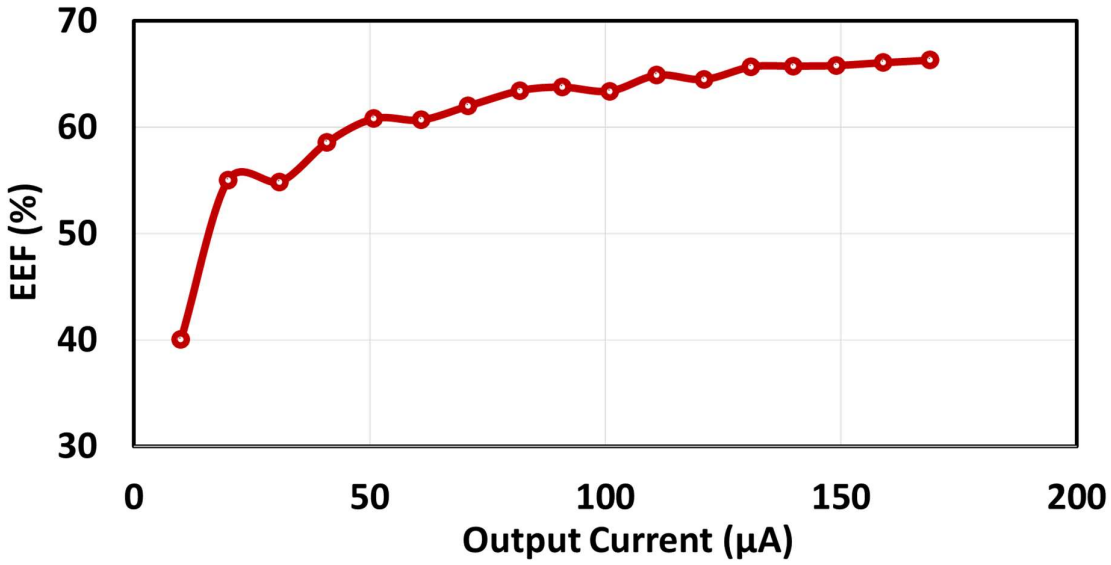


Fig. 2.23. Measures EEF vs. I_{out}

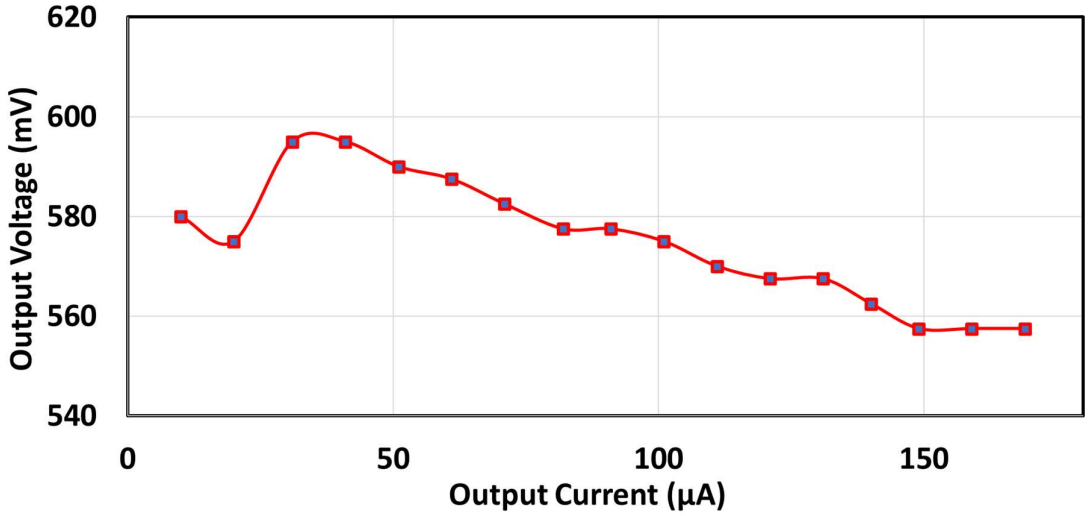


Fig. 2.24. Measured V_{out} vs. I_{out}.

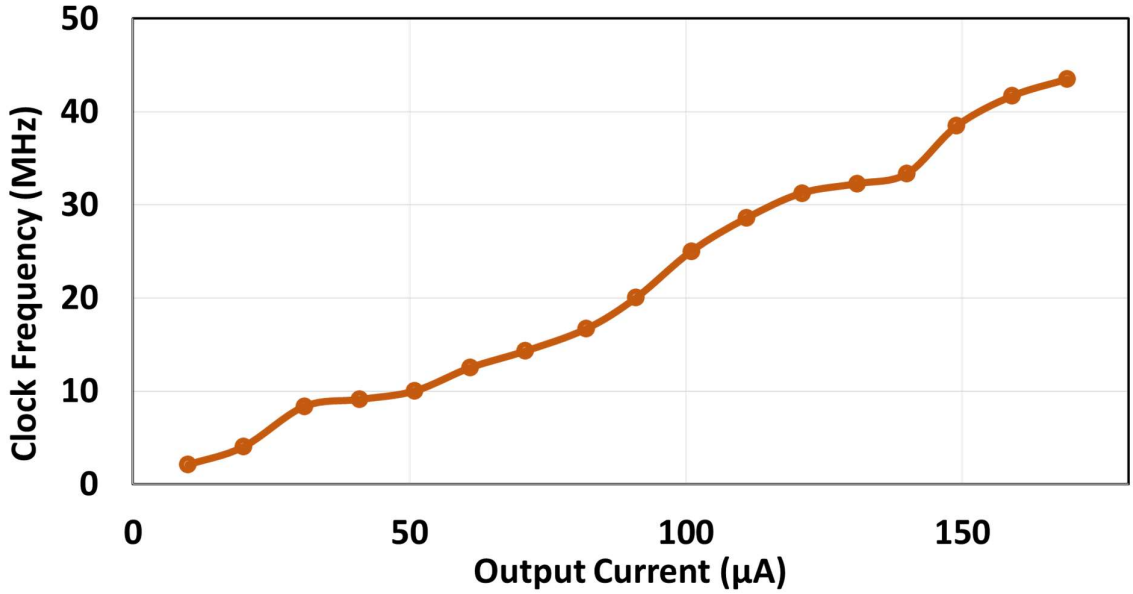


Fig. 2.25. Measured Clock Frequency vs. I_{out}.

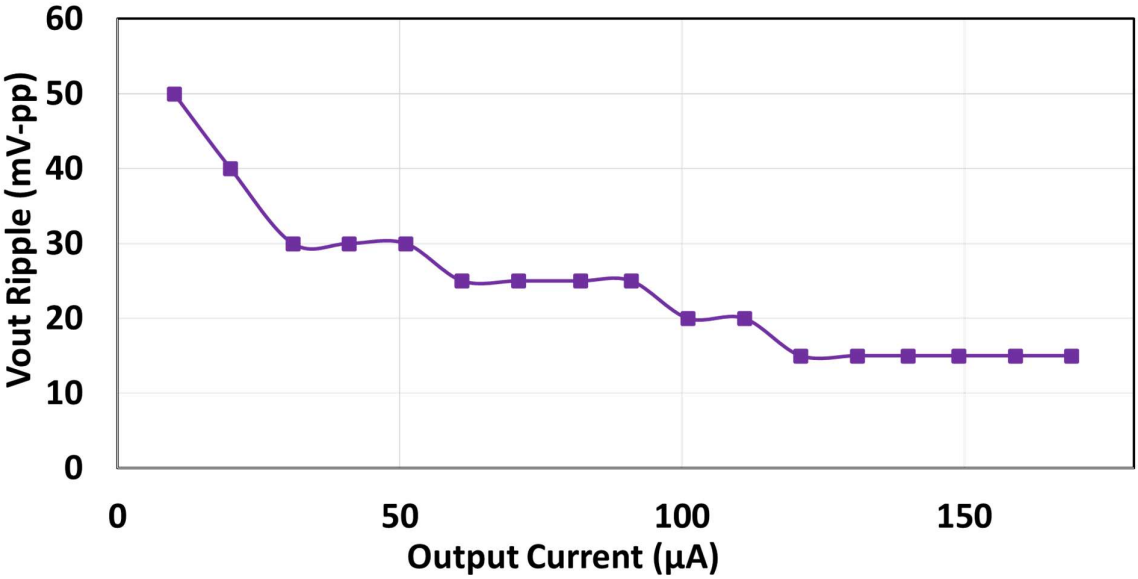


Fig. 2.26. Measured V_{out} Ripple vs. I_{out}.

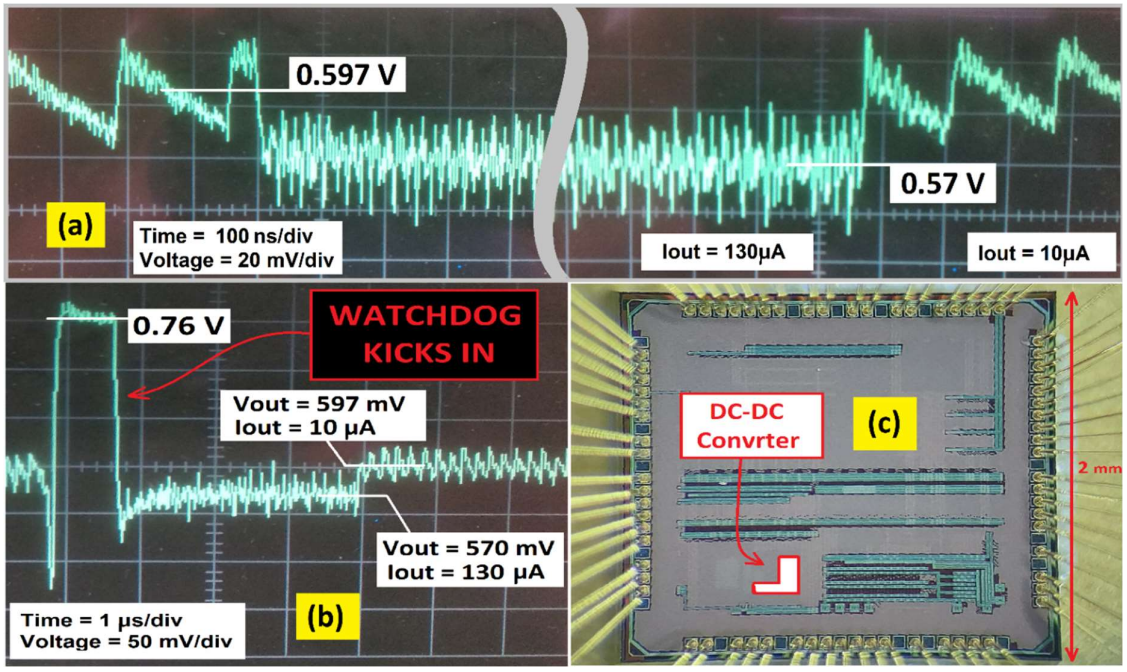


Fig. 2.27. (a) Measured Load transient - 10uA -> 130uA -> 10uA, (b) Load transient as well as a watchdog operation, (c) Die photo.

Discussion

Table 2.1 presents a comparison of the proposed on-die switched capacitor DC-DC converter with previous sub-mW DC-DC converters. Figures 2.28(a,b,c) show a graphical comparison of power density and energy efficiency factor (EEF) for bulk Si switched-capacitor DC-DC converters presented in [4]. The efficiencies and EEFs reported in Table 2.1 were evaluated near or at peak power, where they are typically at the optimal point. It can be observed from [9] that both power density and EEF degrade at very low power, which may be partially attributed to current consumption in the regulation and support circuitry. The proposed DC-DC converter exhibits the best EEF and power density among sub-0.5mW DC-DC converters and is even competitive with converters whose power is two orders of magnitude higher. A graphical presentation of the prior art's power density (Fig. 2.28(b)) clearly indicates that achieving higher power density becomes increasingly harder in low-power domains, which is also the case with other indicators of quality. For this reason, only DC-DC converters in a similar power area should be compared or the parameters should be scaled with power. Figure 2.28(c) illustrates the joined contribution of EEF and Power Density plotted on the graph for sub-mW DC-DC converters. The upper right corner indicates higher performance. It can be observed that the proposed topology scores better than reported prior art DC-DC converters.

Table 2.1. Comparison to other on-die low power switched capacitor converters.

	This Work	[1]	[14]	[15]	[16]	[17]
Tech Node	65nm	180nm	180nm	65nm	130nm	180nm
Actual VCR (topology VCR)	0.2 (1/4)	0.23 (1/3)	0.225 (1/4)	0.83	0.32 (2/5)	(1/3)
C_fly	MIM 6x5pF	-	-	MIM 445pF	800pF	MIM
Power Density (mW/mm^2)	2.56	1.2	0.266	1.3	0.055	0.038
Efficiency	62%	54%	58%	78%	65%	81%
EEF	66%	57%	61%	-7%	51%	44%
Vin	2.5 – 3 V	4.2 V	3.8 – 4.2 V	1.2 V	2.7 – 3.3 V	0.9 – 4 V
Vout	0.55/1.2/1.8 V	0.98 V	0.9/1.2/1.5 V	1 V	1.05 V	0.6/1.2/3.3 V
Max Power (mW)	0.095	0.97	0.45	0.35	0.1	9.7
Area (mm^2)	0.037	0.79	1.7	0.27	1.82	0.25
Ripple peak-to-peak	15mV – 50mV	20 mV	-	40 mV	200 mV	-
C out	50 - 70 pF	1nF	-	1050 pF	-	3 nF
Droop Response	No Droops or Overshoots 10µA -> 130µA	Droop = 230mV Overshoot=200mV 10µA -> 100µA	Droop = 200mV Overshoot = 200mV 10µA -> 50µA	Droop = 50mV No overshoots 10µA -> 250µA	-	Droop=150mV Overshoot=150mV 10nA –> 1µA

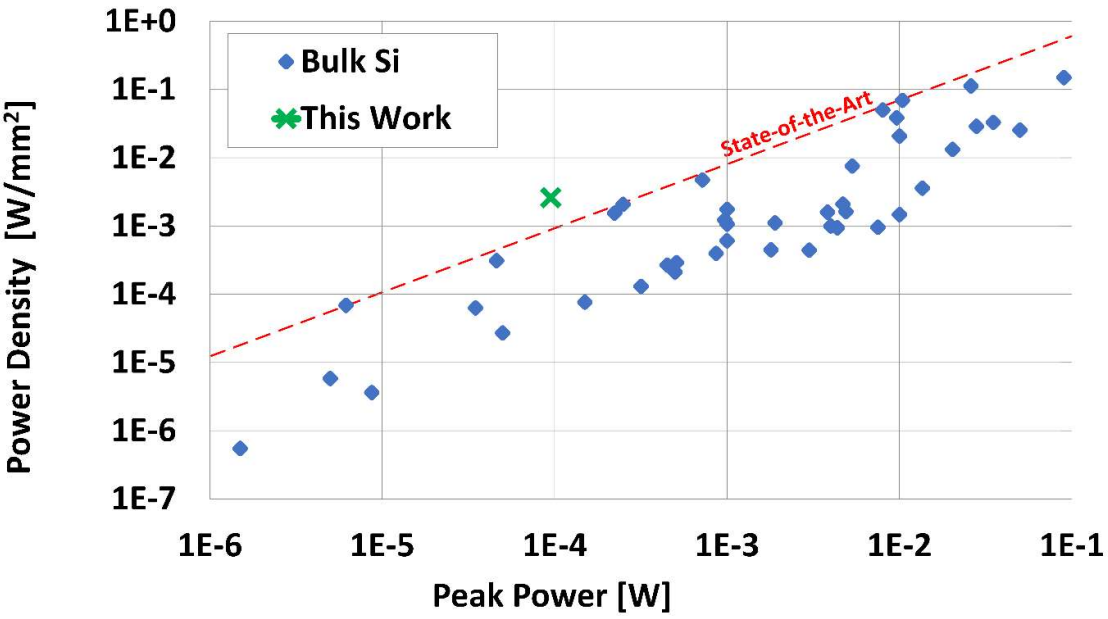


Fig. 2.28(a). Power Density vs. Peak Power for Bulk Si switched capacitor buck and boost DC-DC converters [9].

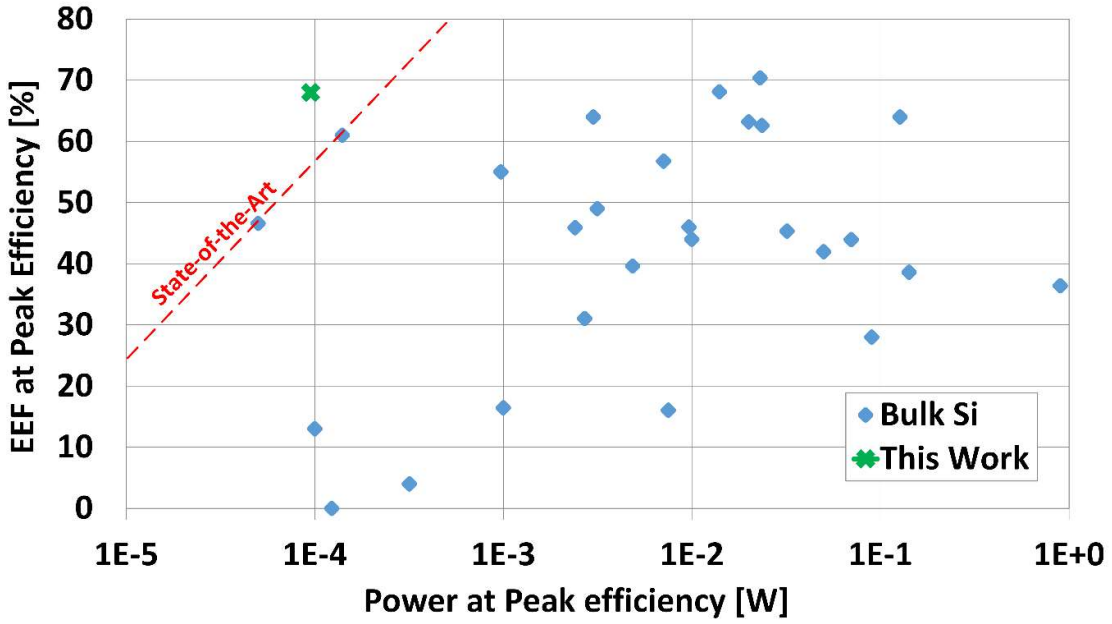


Fig. 2.28(b). EEF vs. Power at Peak Efficiency for Bulk Si switched capacitor Buck DC-DC converters [9].

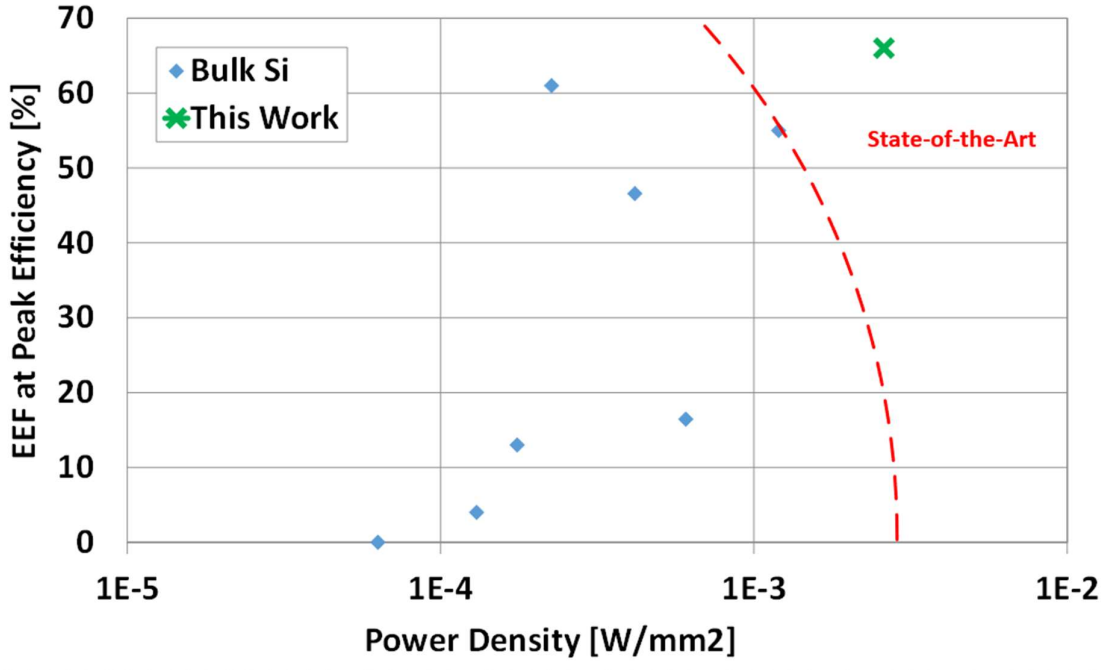


Fig. 2.28(c). Combined contribution of EEF and Power Density (EEF vs Power Density) for sub-mW converters.

Conclusion

The proposed topology employs a supply-regulated inverter, which is the foundation of a highly energy-efficient, high-speed comparator. Regulation is achieved by adjusting a reference voltage that determines the supply voltage of the inverter. This reference can be operated directly from V_{bat}, as it is assumed to consume nW-level power, similar to other adjustable references available in the literature [19]. Despite being low power, the inverter enables a fast response, allowing the proposed DC-DC converter to exhibit the best transient recovery among the circuits in Table 2.1, despite the small load capacitor. This prevents voltage droops that could result in timing failures. As the DC-DC converter is self-clocked, the efficiency and EEF remain relatively stable over most of the operating range. The main output voltage of 0.55V is suitable for always-on digital domains operating at near-Vth. Additionally, voltage domains of 1.2V and 1.8V are available for analog circuits, and the DC-DC converter uses internally generated voltages to power its own circuits. The State-of-the-Art performance in terms of efficiency, speed, and power density of the proposed DC-DC converter makes it a promising solution for always-on circuits in IoT devices.

3. A PHOTOVOLTAIC ENERGY HARVESTER AS PART OF THE IMAGE SENSOR PLATFORM

Introduction

This chapter focuses on a fully integrated energy harvester as part of the image sensor platform [4]. Photodiodes can be utilized for both image sensing and energy harvesting but at opposite polarity. Numerous research works have attempted to create a self-powered imager by flipping the diodes and harvesting them. However, the integration cycle in the image sensing (IS) process is very long, and the chip cannot be harvested while in this mode. In the presented platform, an event detector (ED) function is implemented, whereby the voltage across the photodiode is monitored during harvesting. If there is a significant change in this voltage, then an event is detected, and the chip can take a picture.

Low-power image sensors are used in a large variety of IoT platforms. There have been several works which used the photodiode of the image sensor as a photovoltaic cell in an energy harvesting (EH) mode, to facilitate self-powered image sensors [20], [21], [22], [23], [24], [25]. These could be very useful in remote "edge" applications where it is inconvenient to switch a battery. However, in an image sensor, the photodiode needs to be reverse biased, while an EH photodiode operates at forward bias. Thus, during the long integration time of the image sensor and its readout (10's to 100's of ms), the diodes cannot extract energy. For self-powered image sensors, this "dead time" would be significantly extended since much lower frequencies are used. For many such applications it is not the static image, which is of interest, but rather significant changes in the background, requiring event detection (ED) during EH. A good example of this would be a remote security fence, where any breach or prowler would need to be detected, but frequent changing of the battery is inconvenient or dangerous. In this system, ED is demonstrated during EH mode, whereby the voltages across sections of the forward-biased photodiode array are monitored for changes. If a change is detected, then the chip will flip the diodes and take a photo. In this manner, the chip could be harvesting for a much larger percentage of the time, and the power-consuming imager would take a picture only during relatively unusual events. In [25], motion detection and IS were proposed using two different diodes during EH. However, this required a triple-well process, which is a cost-adder. In this system, the same P+/Nwell photodiode is used for IS, ED, and EH (Fig. 3.1) to utilize a standard (nontriple well) CMOS process.

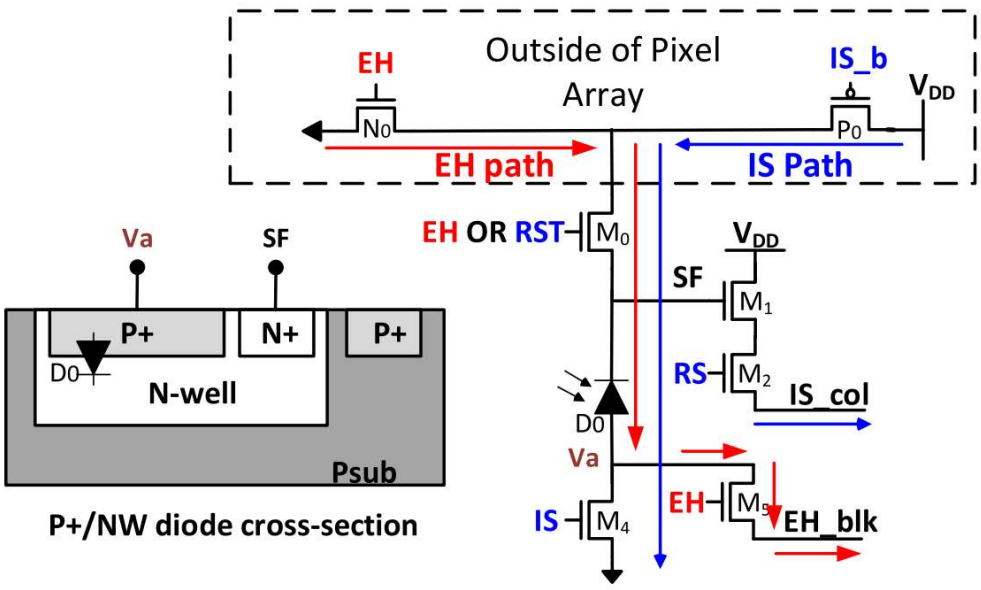


Fig. 3.1. Pixel during EH and IS mode.

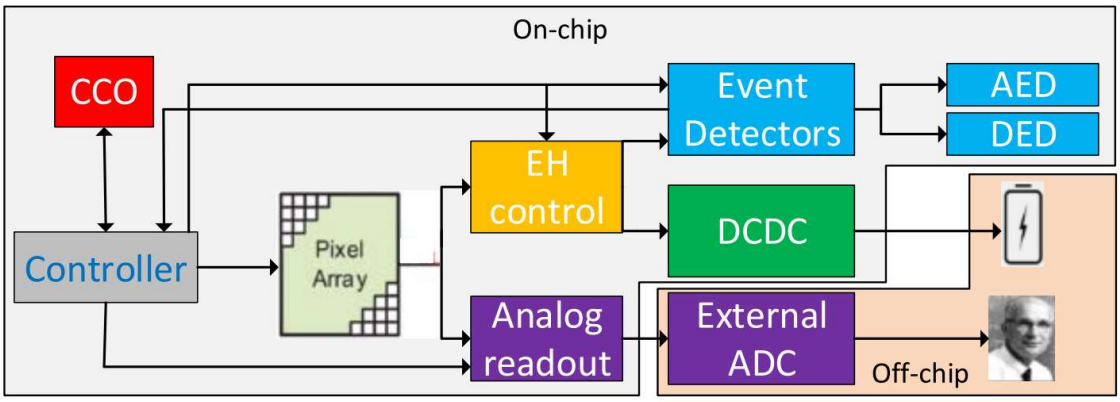


Fig. 3.2. System block diagram.

System Architecture

Fig. 3.1 shows the proposed reversible Pixel which was used for this design. Two power gates outside the array (P0 and N0) apply either Vdd or Vss to the drain of M0. During IS, the signal (IS) is asserted, the pixel is reverse biased, and the cathode of the photodiode discharges SF after reset (RST). The source follower, M1, drives the output to the sensing column (IS_col) for it to be sensed by an ADC for rows selected by the row select (RS) signal. During event

detection, EH is asserted, and the forward-biased photodiode can charge EH_blk, which is common to a block of 512 Pixels. The process used was the standard 180nm TSMC CMOS process. It is recognized that this would have a much lower quantum efficiency than an image sensor process [26] but is sufficient to demonstrate the ED capability. A block-level diagram of the chip is shown in Fig. 3.2. There is a logic controller block that arbitrates between different modes and determines the timings. It is assumed that such a system would have a 32kHz crystal-based system clock, which can be provided at sub-20-nW power [27]. When circuits become active, a 12 to 25-MHz current-controlled oscillator (CCO) clock wakes up to implement ED or IS. There are two types of ED circuits implemented: 1) an analog ED (AED), where the data is stored as an analog signal on a capacitor, and 2) a digital ED (DED), where the data is stored in registers. The EDs can wake up for a short time (1 μs–1 ms) in a long EH cycle (1 ms-seconds) to sample EH_blk (Fig. 3.1) of a pixel block, and this will be compared to the previous sample. The AED is lower power than the DED but can only store data for < 5 ms. Thus, the AED is better optimized for faster events, while the DED would be optimal for slower ones (10 ms—10's of seconds).

During EH mode, a DCDC boost converter converts the photovoltaic voltage to CMOS levels. The charge is stored on a large external capacitor and can be used to either power the chip or recharge a battery. There is also an analog readout to characterize the pixels in IS mode [20]. Some more architectural details are shown in Fig. 3.3, and the timing diagram for ED is shown in Fig. 3.4. The 128x128 array is divided into 32 blocks of pixels (8 rows of blocks times 4 columns). There is a design tradeoff between the block size (512 Pixels) for ED and the power/complexity of the chip. The EH_control* block contains switches and logic which control each row of blocks. Within each 16 by 32 block, the EH_blk signals of the pixels (Fig. 3.1) are shorted, such that there is an EH_blk bus. When the blocks are not sampled in ED, they can be connected to the DCDC input (EH_bus) for EH. In principle, while one row of blocks is sampled in ED, the rest of the rows can be harvested. For simplicity, the logic to do ED and EH simultaneously was not implemented in this chip, although this can be done in a real product. During ED, a row of pixel blocks is connected to EH_col*.

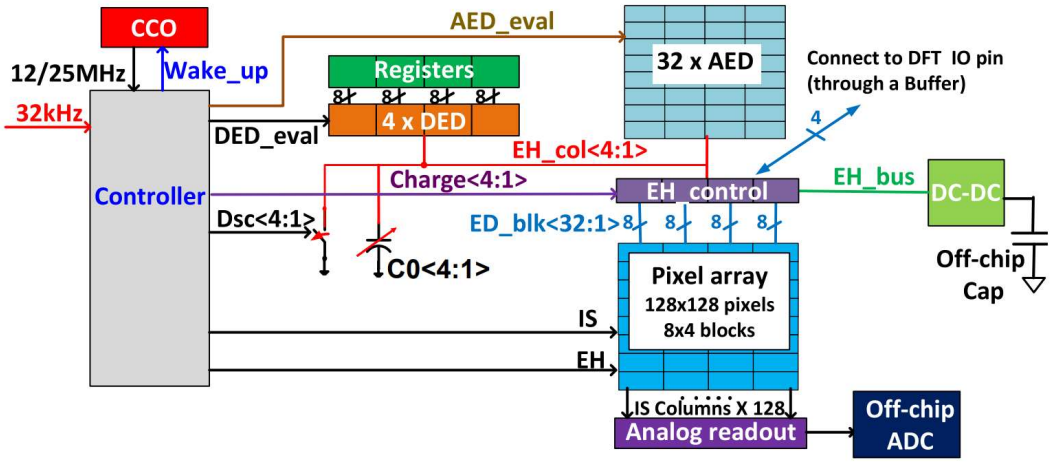


Fig. 3.3. Detailed chip architecture.

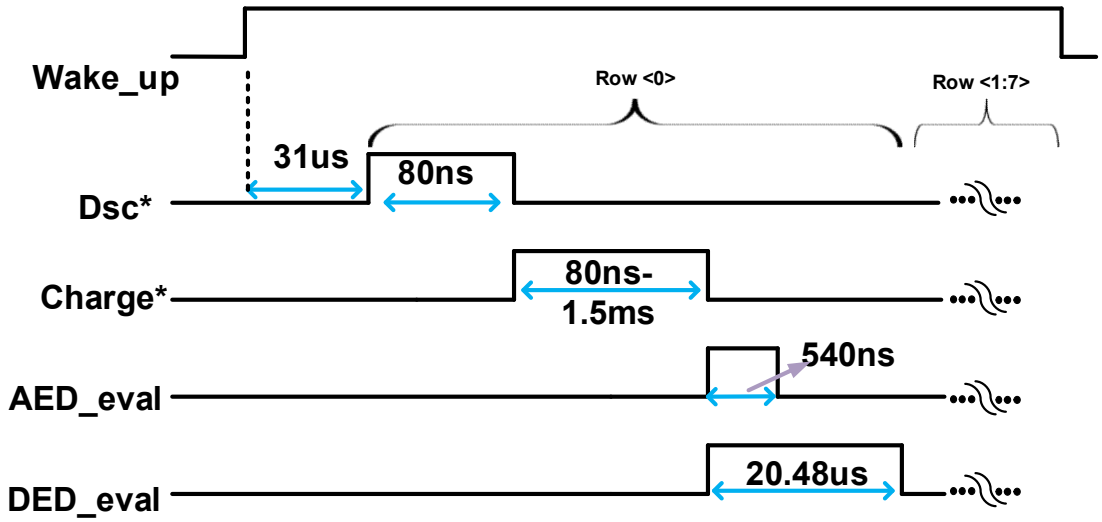


Fig. 3.4. Timing diagram.

When Wake_up asserts, the CCO is enabled to provide the 12–25-MHz clock. Prior to sampling for ED, EH_col* is discharged to Vss when Dsc* asserts, and then it is charged by the pixel block when Charge*=1. Either AED_eval or DED_eval is then asserted that ED wakes up, samples EH_col*, and then evaluates it. The sequence of Dsc*, Charge*, and *ED_eval is repeated for each block row, similar to a rolling shutter operation. When Wake_up drops, all the circuits go to sleep. The configurable Charge* timing (Fig. 3.4) and the trimmable capacitor C0* (Fig. 3.3) will determine how fast EH_col* charges. This allows for control of dynamic

range versus resolution to account for different illumination levels. Each pixel block has its own AED, which samples the voltage onto a capacitor. The DED digitizes the data with a 1-bit Sigma-Delta Modulator (SDM) and stores it in registers. Thus, the DED can be reused between rows of blocks. There are also connections available to sample EH_col* to the IO (through a pMOS source follower buffer) or drive it from the outside.

Harvester Architecture

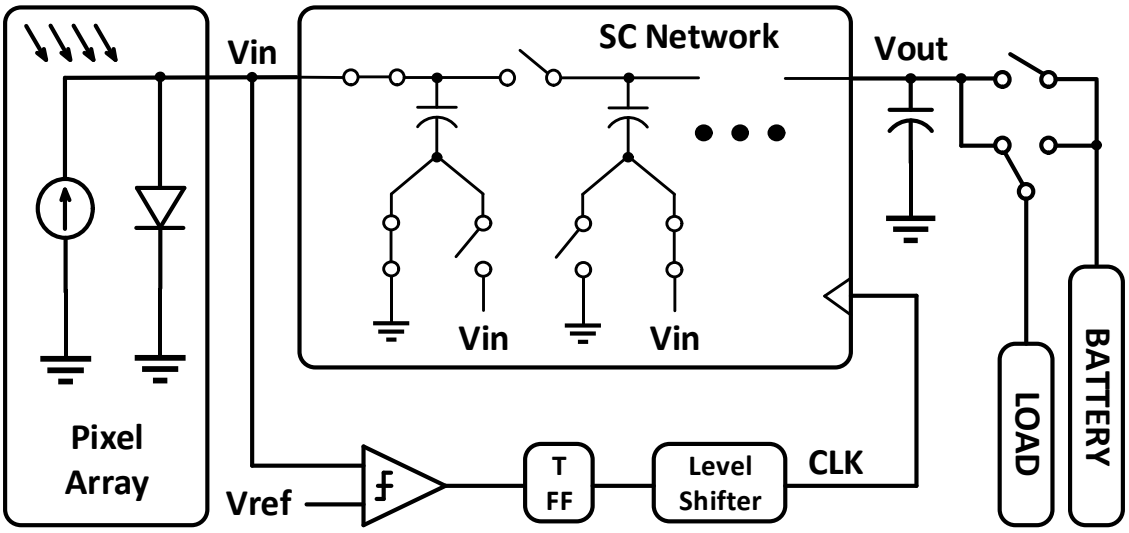


Fig. 3.5. Boost DC-DC converter.

The DC-DC boost converter is shown in Fig. 3.5. The clocked switch-capacitor (SC) network is the ladder-star architecture, similar to [23]. The DCDC is regulated by comparing the input to a reference voltage, V_{ref} (400 mV), which is generated internally by a 2T-based trimmable reference [19] and consumes a nominal static power of ~2 nW. Vin is charged by the array. As soon as it exceeds V_{ref}, a pulse is sent to the SC network which boosts Vout and the charge is drained from the internal capacitors, which results in a ripple at V_{in}. The output voltage, V_{out}, is stored on a large capacitor, which minimizes the output ripple. The DC-DC could either be used to power the chip or recharge a battery. For a photovoltaic source such as this, it is assumed that a battery will be required since it may still have to function in the dark.

Figure 3.6 illustrates the detailed configuration of the SC network. The configuration VCR (maximum output voltage) is equal to N_{SC}+1, where N_{SC} stands for the number of switching capacitors. It can be observed that the SC network has two configuration bits (ctrl), that way

three different VCRs can be accomplished with the same SC network. In this case, the maximum possible VCR is achieved when both switches are conducting (VCR=6). Following that, VCRs of 5 and 4 are also possible with the proper configuration. Since multiple VCRs are implemented, the DC-DC can operate with higher efficiency over a wider range of input and output voltages (additional losses are introduced as soon as the real ratio of Vout to Vin goes away from topology VCR, see Chapter 2).

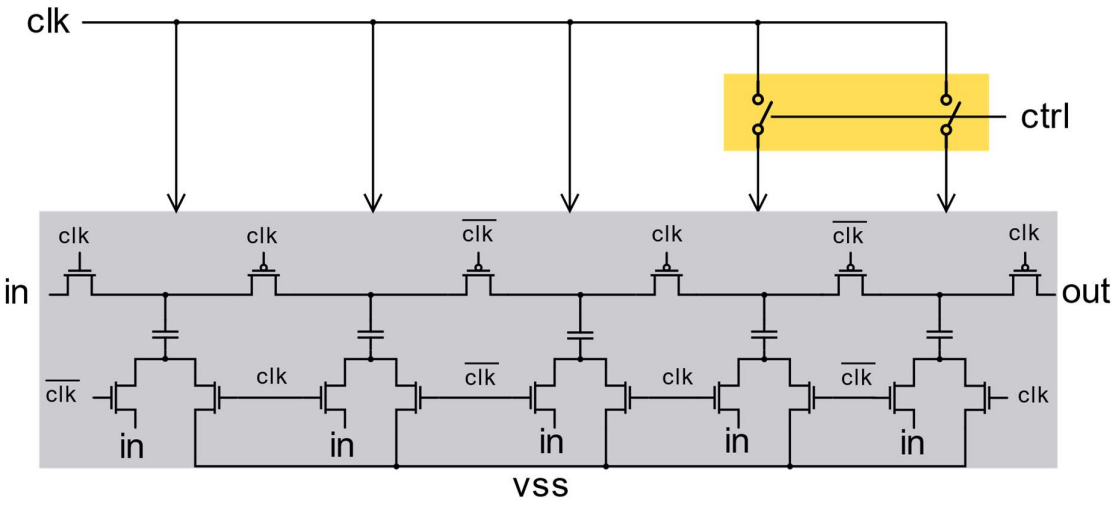


Fig. 3.6. SC network configuration.

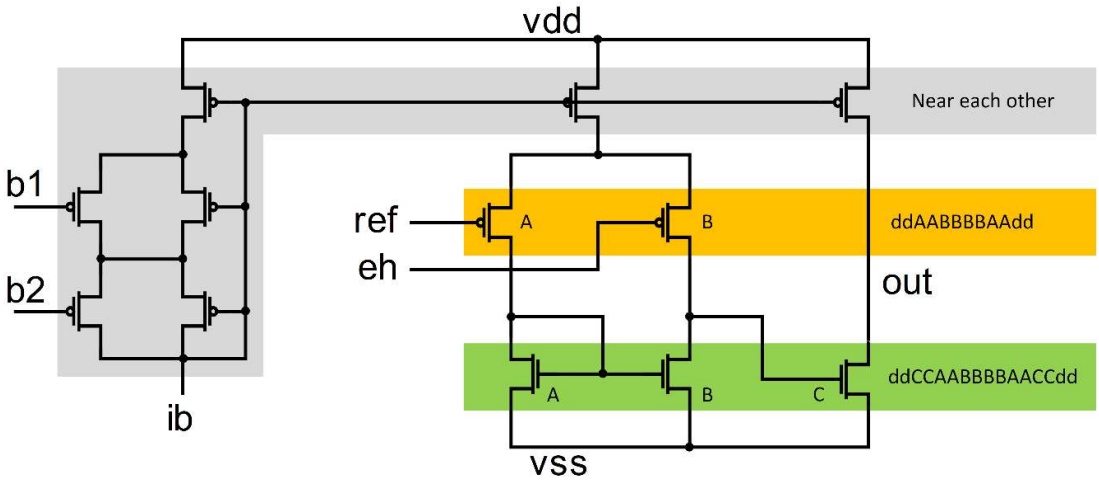


Fig. 3.7. Comparator.

A two-stage miller amplifier with a trimmable bias current is used as a comparator (Fig 3.7). Digital input bits b1 and b1 are used to adjust biasing. Since the output voltage offset is important for this application, the MOSFETs were matched with a common centroid configuration (see Fig. 3.7).

Measured Results

The design was implemented in the TSMC 180nm standard CMOS process. The chip was measured with a configurable LED source. After illumination, the ED data was driven off chip by shift registers. Note that the chip is harvesting between the measured ED cycles. To measure efficiency, the DCDC was driven by an external current source to produce an output near 1.5 V (Fig. 3.8). The input voltage ranged between 0.37V and 0.4 V during these measurements.

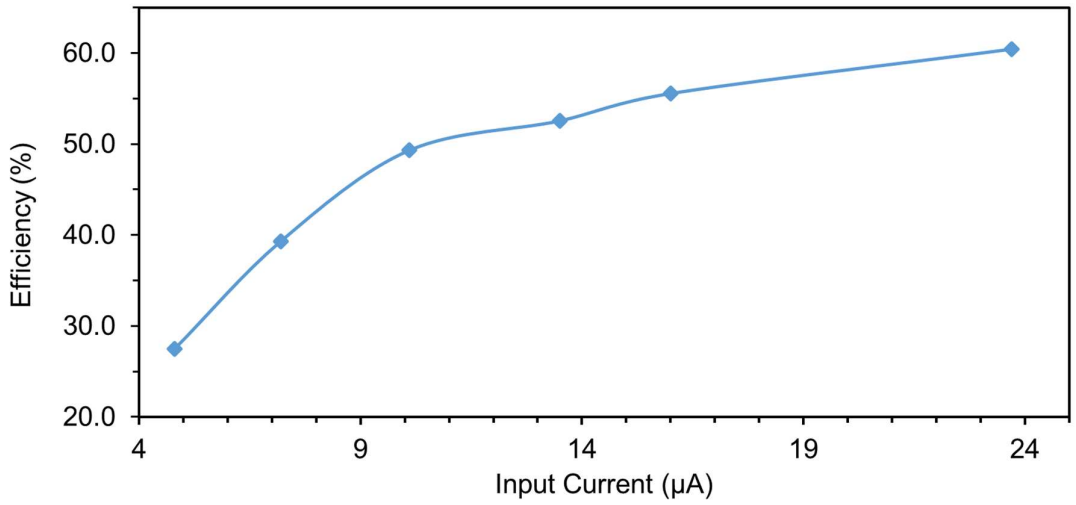


Fig. 3.8. DC-DC Efficiency for an external current at V_{out}=1.5V.

Fig. 3.9 shows the waveforms of Vin, Vout, and Clock for the case Iin = 7.2 μA. Since the input voltage needs to be regulated for energy harvesting, the clock frequency is proportional to the input current that charges the input node (Vin).

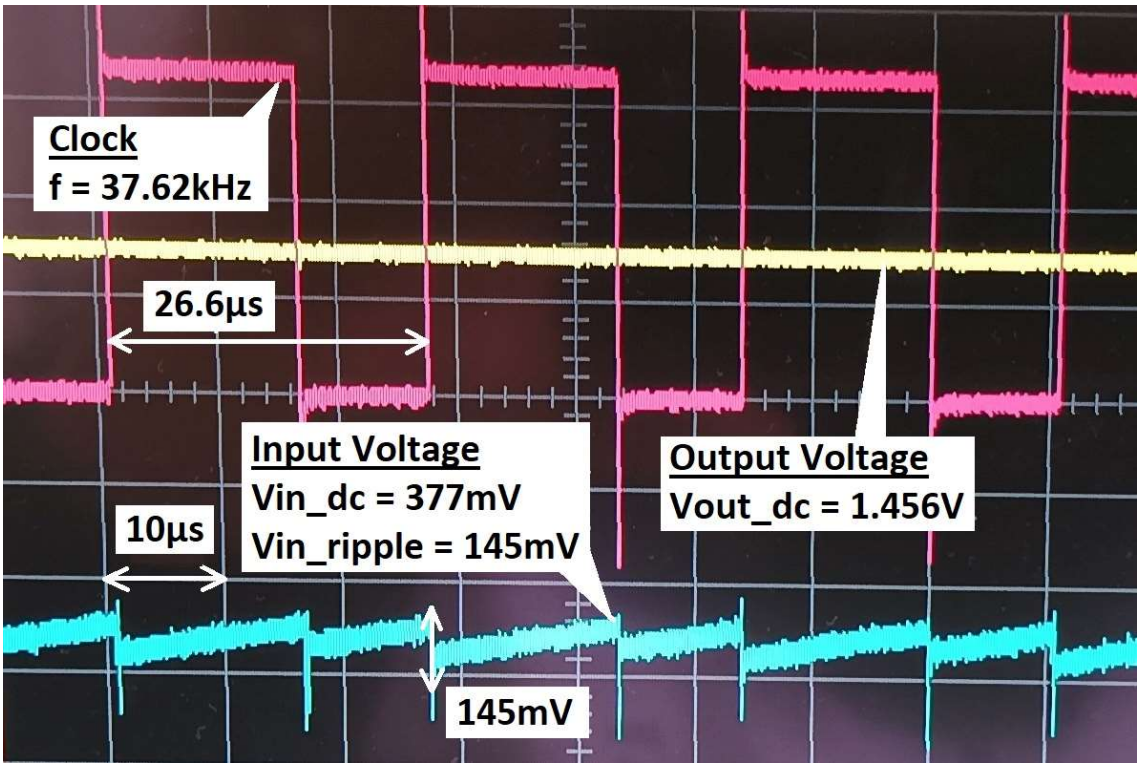


Fig. 3.9. DC-DC converter waves @ I_{in}=7.2µA and I_{out}=1.3µA.

In this case, the DC component of the Vin is equal to 377mV. The Vin ripple of 145mV can be observed, and the clock frequency for this input power is 37.62kHz. An output voltage ripple cannot be observed since the large external capacitor is slowly being charged.

Figure 3.10 shows the DCDC input and output currents at nodes Vin and Vout, respectively, while the pixel array is illuminated. Up to 3.5 µA are produced under the maximum illumination (100 kLux = direct sunlight). Assuming a net 2-µA boosted current and an imaging power like [28], a frame rate of 14 frames/s could be achieved. In an image sensor process, much higher quantum efficiency would be achieved, which would enable higher current levels. Such a system is also expected to include a lens, which would focus the light to provide much higher illumination levels. The pixel readout circuit in IS mode, as well as measurements of several pixels, are shown in Fig. 3.11. The column voltages are sampled on capacitors (C1 in Fig 3.11) located at the bottom of the column. These voltages can be muxed and read out serially via the source follower, P1. In the measurements shown, the pixel integration time is 220 ms. There are well-established techniques to shorten this time and achieve a very wide IS dynamic range (116 dB) in a product [29].

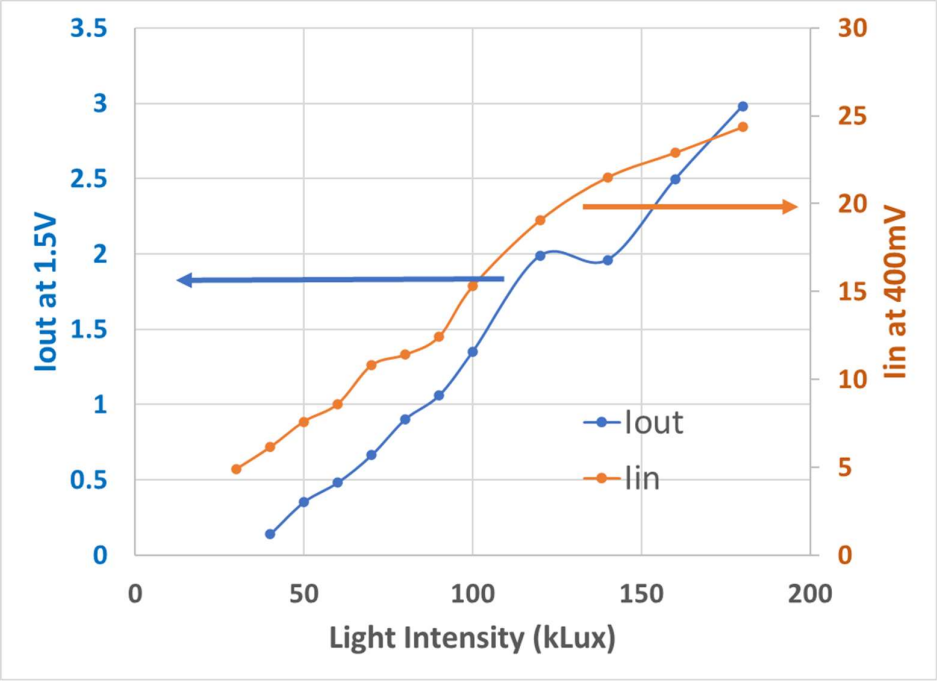


Fig. 3.10. Measured DCDC input current (at Vin) and output current (at Vout) under illumination. Vref = 400 mV and Vout = 1.5 V

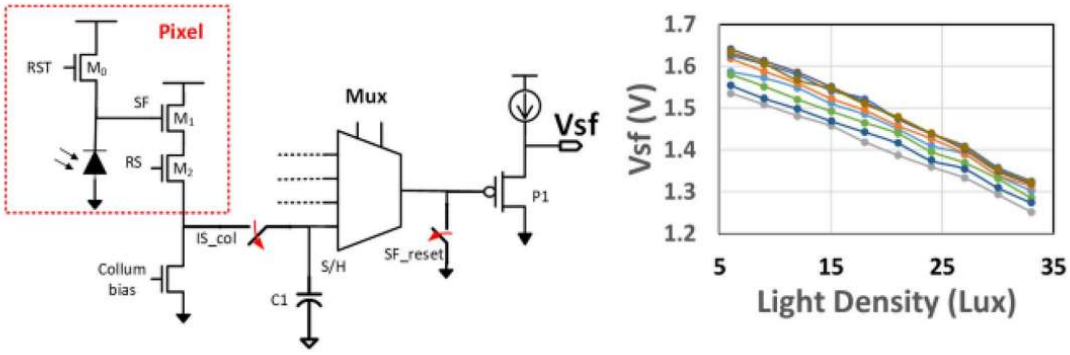


Fig. 3.11. Pixel IS analog readout circuit and measured output of several pixels under illumination.

A comparison to other EH/IS designs is shown in Table 3.1. A die photo and corresponding layout photo are shown in Fig. 3.12. This design utilized the same reversible photodiode for EH, IS, and ED while not requiring a triple well process. This is a completely new feature, to the authors' best knowledge. This could enable longer EH cycles, which could facilitate better self-powered imagers in Edge devices.

Table 3.1. Comparison to other EH/IS designs.

Ref	[21]	[22]	[23]	[24]	[25]	This work
Process	130n	350n	130n	180n tripple well	180n tripple well	180n
Pixel Pitch (μm)	9	23	5	19.5	4.75	10
Fill factor (%)	83/51	44	60	30.6	27.5	41
EH (pW/Lux/mm²)	17.5	865	NA	NA	267	34.6
Boosted Output (V)	1	3.3	0.6/1.8	0.7	none	1.5
Peak Boost Efficiency (%)	48.4	76	52.4	NA	NA	56.2 (illuminated) 60.4 (external)
ED during EH capability	no	no	no	no	yes*	yes
*Diffusion diodes are used for IS/ED, while DNW/Psub are used for EH						

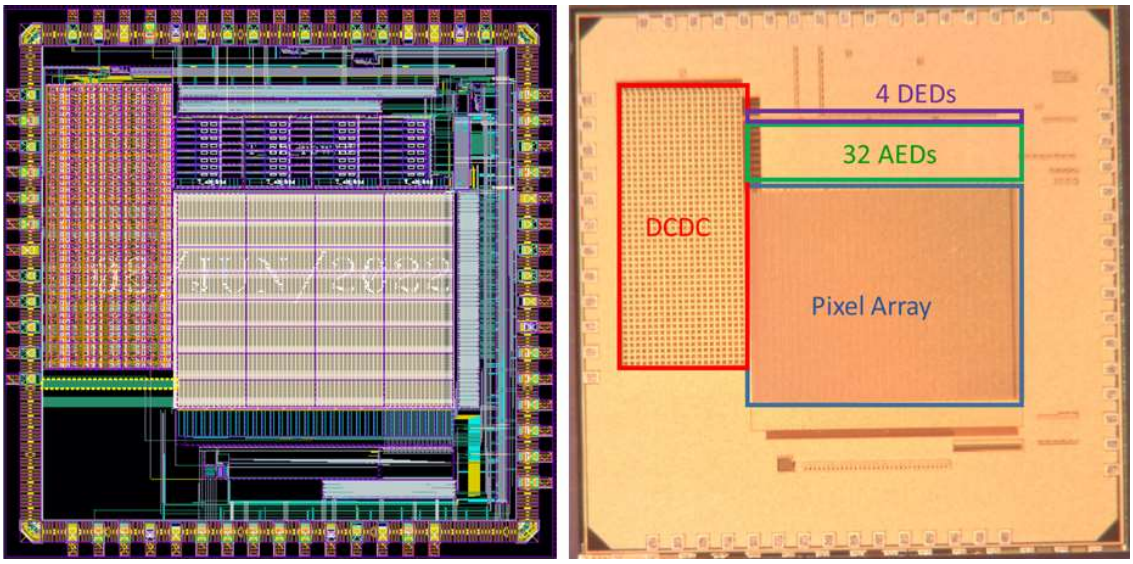


Fig. 3.12. Die photo with corresponding layout.

4. LOW-POWER TEMPERATURE-COMPENSATED CLOCK GENERATOR

Introduction

An essential feature in every digital and mixed-signal System-on-Chip (SoC) design is clock synchronization. The most commonly used clock requirements for various applications are illustrated in Fig. 4.1 [30]. The Phase-locked loops (PLLs) can serve as high-quality clock generators to support mixed-signal designs [31], [32], [33]. However, a PLL usually requires a larger area and has considerable power consumption, making it unsuitable for low-power applications. Therefore, the design of a 'cheap' multiple-frequency clock generator to meet the specific demands of the required application is crucial.

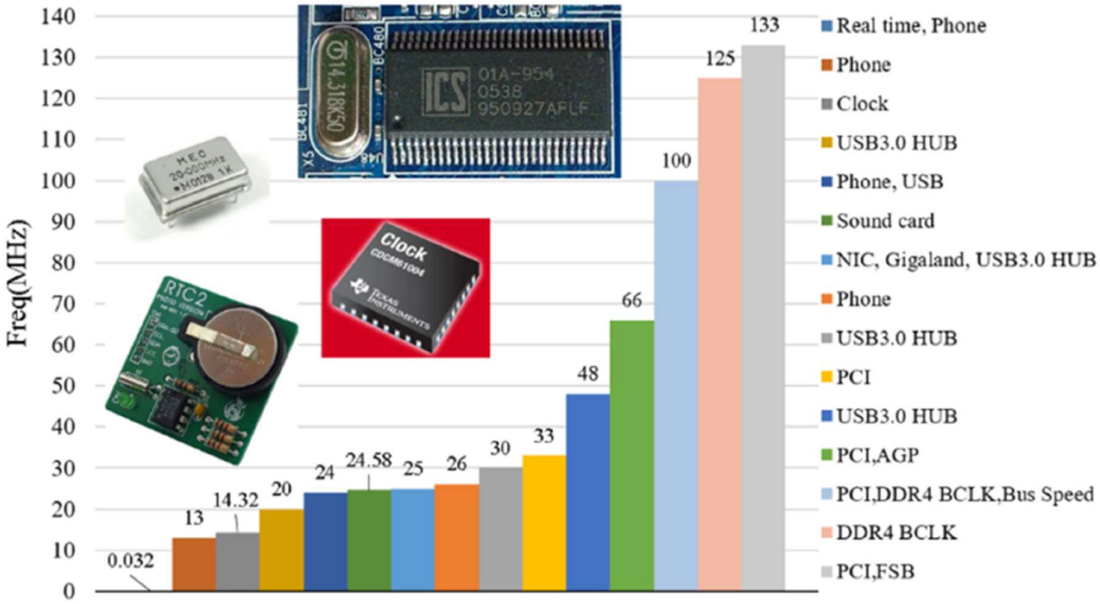


Fig. 4.1. Clock frequencies of modern consumer electronic applications [30].

Power management of IoT devices usually requires a clock signal for one or more voltage regulators. In some cases, the clock signal could be generated externally and connected to the chip. However, if the device is battery-operated and placed in a remote location, an internally generated clock may be inevitable. Furthermore, external active components usually consume much more power, so the clock generation on-die is usually a better option for systems where power efficiency is crucial. The proposed clock generator is designed as part of the image-sensing platform (also mentioned in Chapter 2) and published as a journal paper [4]. The system requirements for the clock frequency were 12MHz/25MHz with temperature and duty cycle

compensation. Furthermore, an option to bring an external clock and fix its duty cycle was required for debugging purposes.

Circuit Architecture and Simulated Results

The current-controlled (CC) ring oscillator is one of the easiest and most efficient ways (both in terms of area and power efficiency) to generate a clock. Oscillations are generated by the cascade of an odd number of inverters, forming a positive feedback loop by short-connection between input and output, as illustrated in Fig. 4.2.

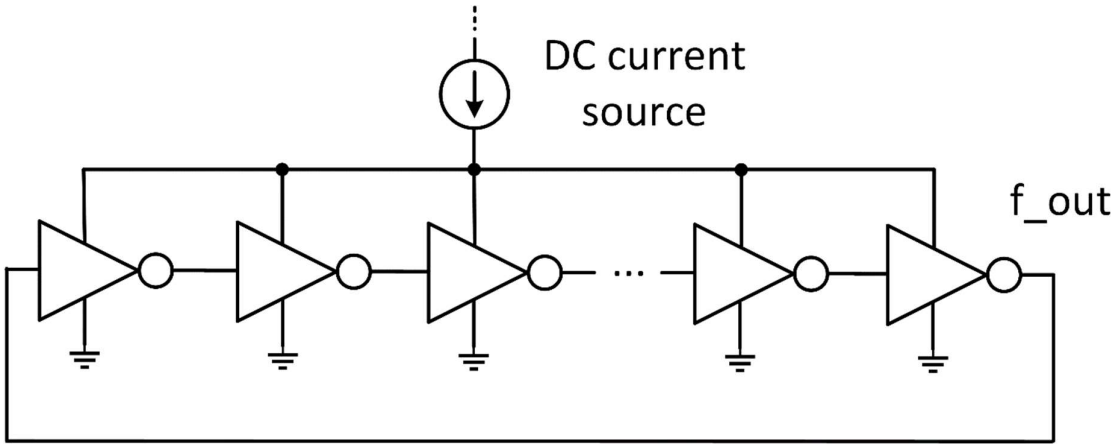


Fig. 4.2. CC Ring Oscillator.

Output frequency (f_out) is proportional to the input DC current, so it can be regulated by changing it. The main problem of this approach is the severe temperature dependence of f_out. Figure 4.3 presents the temperature dependence of the 7-stage 12MHz ring oscillator as an example. It can be observed that f_out varies over the entire temperature range, from 11.22MHz to 13.34MHz, with a relative variation of 17.2%. The temperature coefficient can be obtained by dividing the relative variation by temperature range (140 °C in this case): TC = 1.123 %/°C. A large number of applications (including currently considered image-sensing platform with energy harvester) cannot tolerate such severe temperature dependence.

The proposed solution is to develop a current source (Ibias) with an opposite temperature dependence, which would be able to cancel the Ring Oscillator's temperature dependence to some degree. Figure 4.4 illustrates a block diagram of the system, explaining the concept of temperature compensation together with duty cycle fixation and external clock option.

As mentioned above, the nature of a simple current-controlled oscillator (if the input current is constant) is to have output frequency proportional to absolute temperature (PTAT), as illustrated in Fig. 4.4. and simulated in Fig. 4.3.

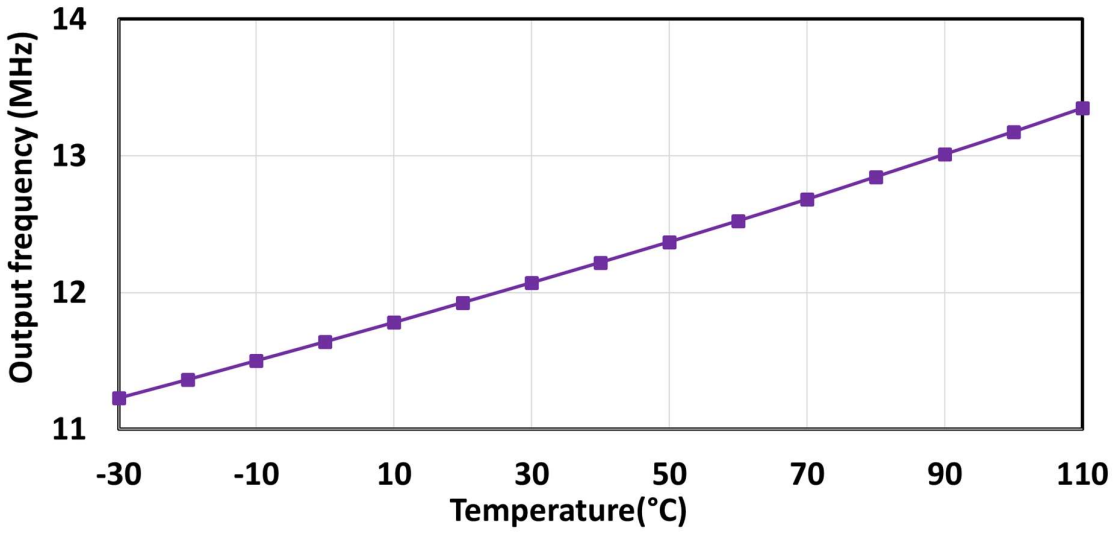


Fig. 4.3. CC Ring Oscillator temperature dependence (f_out vs Temperature) @ 12MHz.

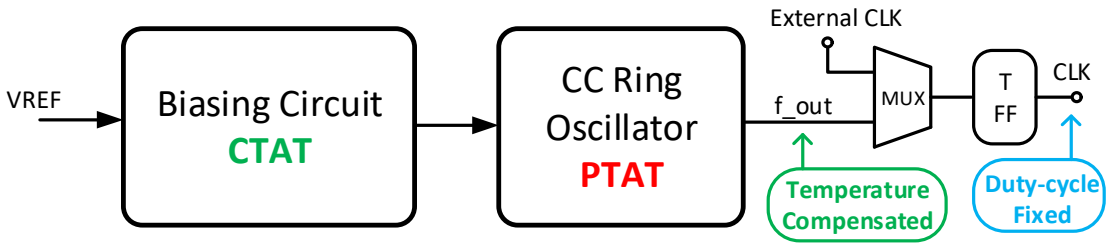


Fig. 4.4. Block diagram.

An introduction of the current bias circuit featuring output current complementary to absolute temperature (CTAT) was implemented as depicted (Fig. 4.4). In that way, the PTAT feature of the ring oscillator is compensated by the CTAT feature of the input current bias. Furthermore, the image-sensing platform required a duty cycle of nearly 50%, which is not the case with the classical CC ring oscillator, especially at process corners and extreme temperatures. For debugging purposes, the external clock option was included in the design as illustrated (Fig.

4.4). The duty cycle was fixed by the T-flip-flop, which divided frequency by a factor of two. In that way, the double frequency needs to be generated by the ring oscillator (50MHz/25Mhz). Note that both external and internal frequency had their duty cycles fixed.

Figure 4.5. shows the configuration of the CC ring oscillator. The cascade of seven inverters was used to produce the required frequency. Since the amplitude of the oscillations is not rail-to-rail (the current source produces some IR voltage drop that varies with input current), the level shifter needs to be utilized to achieve rail-to-rail voltage swing.

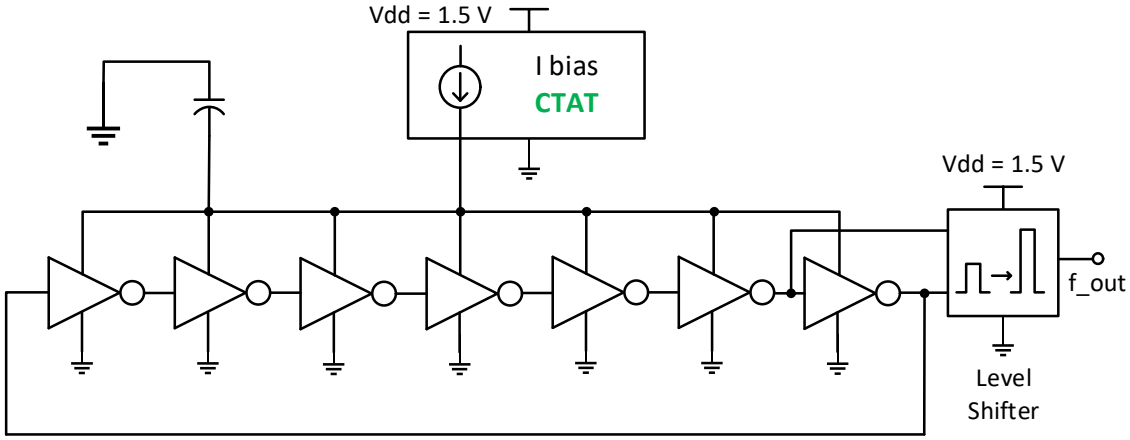


Fig. 4.5. Current-controlled ring oscillator.

The architecture of the CTAT current bias is shown in Fig. 4.6. Initial current I_1 is generated by the voltage across the resistor R_1, which can be fine-tuned by the trimmable voltage reference published in [19]. With the fine-tuning capability, the process variations could be compensated (Vref varies from 400mV to 600mV depending on the MOSFET speed). Current I_1 is copied to I_2 and used to produce CTAT V_{n2}. To achieve CTAT features of I_6 and I_{out}, the voltage across the resistors R_2 and R_3 (V_{n6}) needs to be CTAT as well since the I_6 is defined by the ratio of V_{n6} and total resistance. Finally, the CTAT bias current I_{out} is produced as a copy of I_6. The cascodes of high-threshold-voltage (HVT) and low-threshold-voltage (LVT) MOSFETs were used to achieve higher gain. Due to the difference in threshold voltages, both MOSFETs are in saturation.

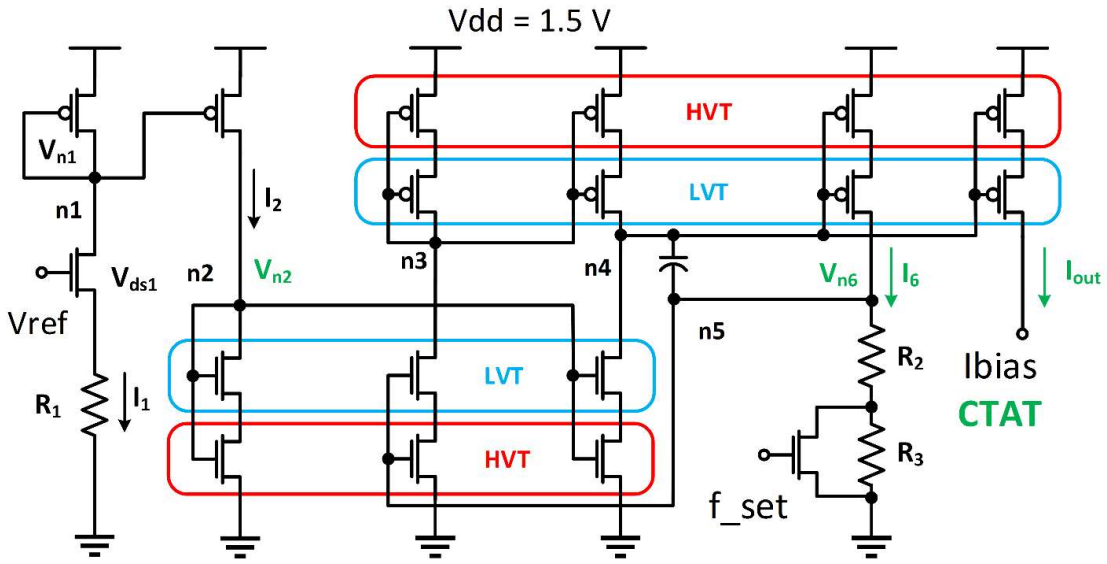


Fig. 4.6. CTAT current bias.

A high-gain level shifter was used to produce rail-to-rail oscillations at the output of the clock generator (Fig. 4.7). To work properly, the level shifter requires in_a and in_b to be complementary to each other (see Fig. 4.5). Simulated waveforms from level shifter are presented in Fig. 4.8. Figure 4.9 presents the simulated waveform of period Jitter, with a simulated RMS value of 337.7ps.

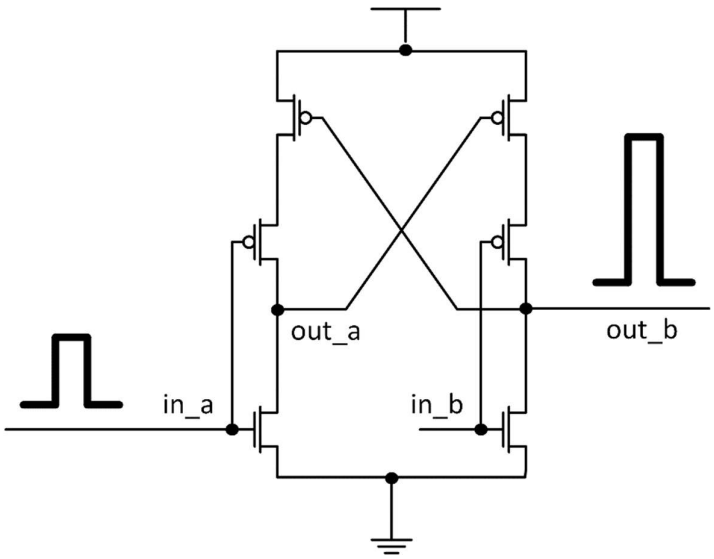


Fig. 4.7. High-gain level shifter.

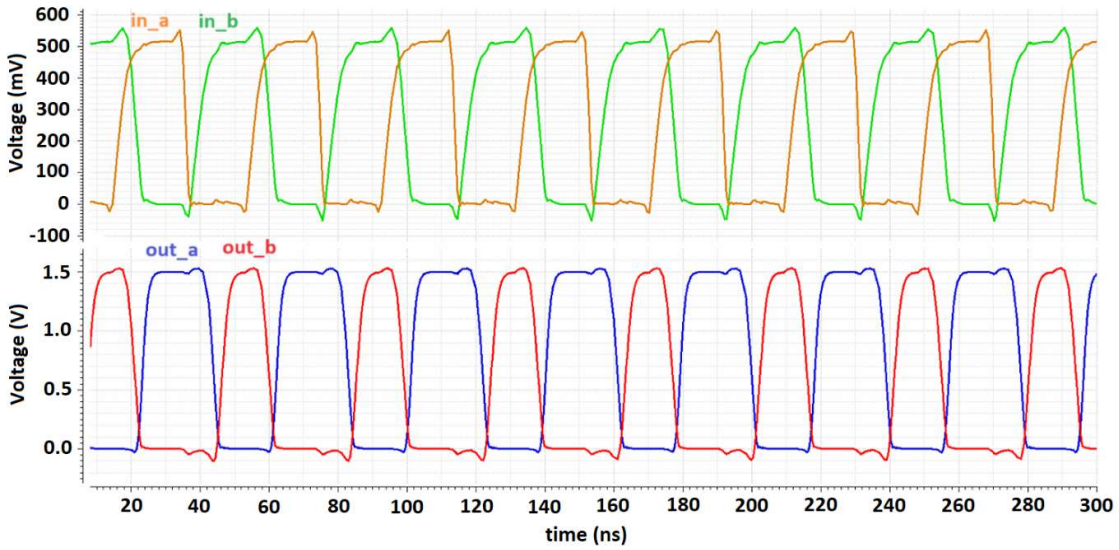


Fig. 4.8. Simulated waveforms of High-gain level shifter @ 12MHz.

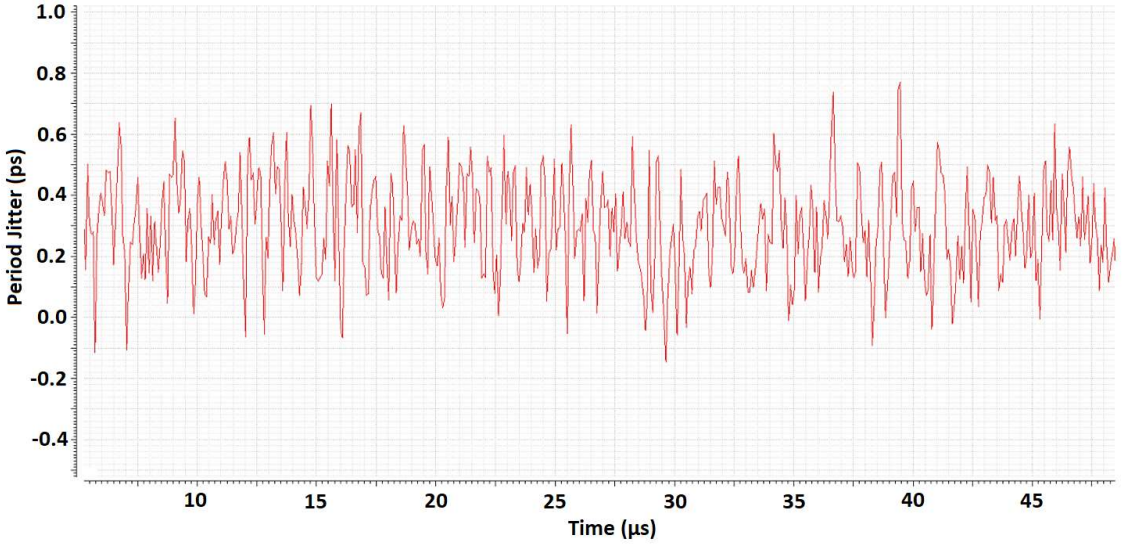


Fig. 4.9. Period Jitter @ 12MHz

Measured Results

Figure 4.10 shows the measured waveform of the output clock, the output frequency is set to 12.35 MHz. The measured duty cycle is 50.9%, sufficiently close to 50%, so the entire system operated without malfunctions. Note that the clock generator was designed to be used as a fully integrated component. Additional noises and distortions were added by bringing the output signal outside of the silicon for measurement.

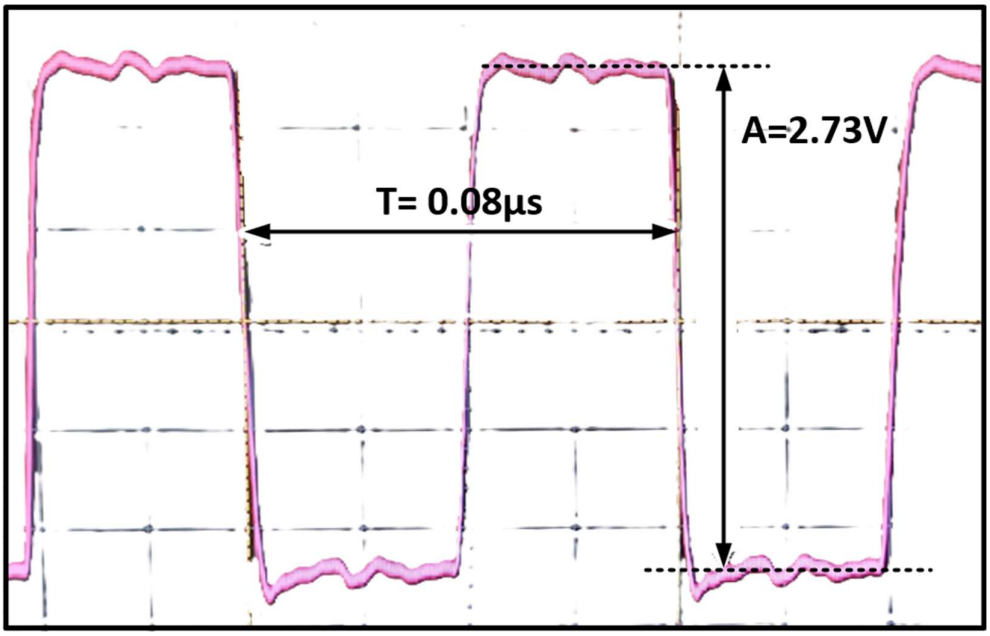


Fig. 4.10. Measured output clock waveform.

The temperature coefficient was measured for 12 MHz and 25 MHz configurations. The measured temperature range was from -30 °C to 110 °C with a step of 10 °C. The measured results are presented in Figs. 4.11 and 4.12.

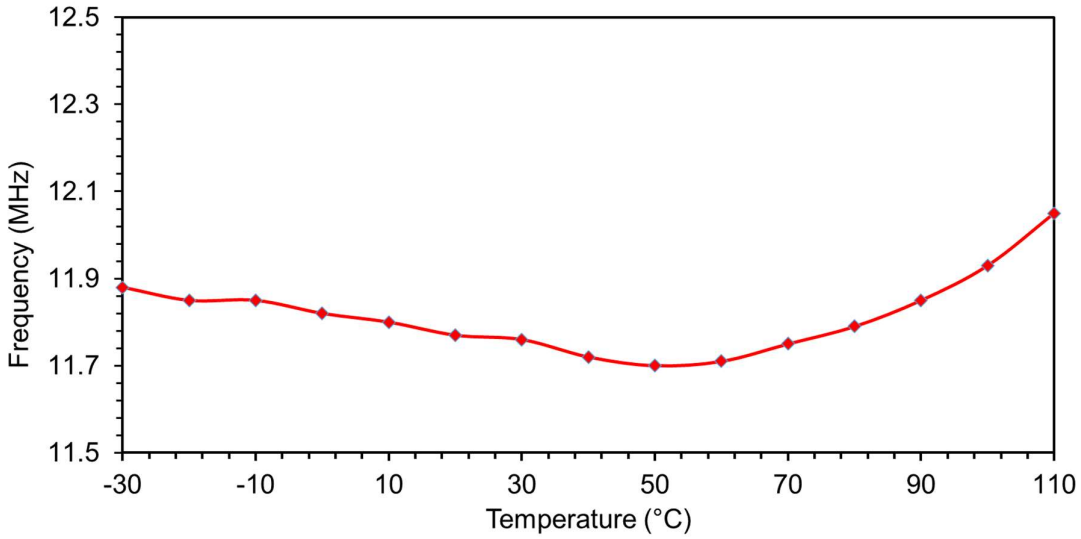


Fig. 4.11. Temperature compensation (12 MHz).

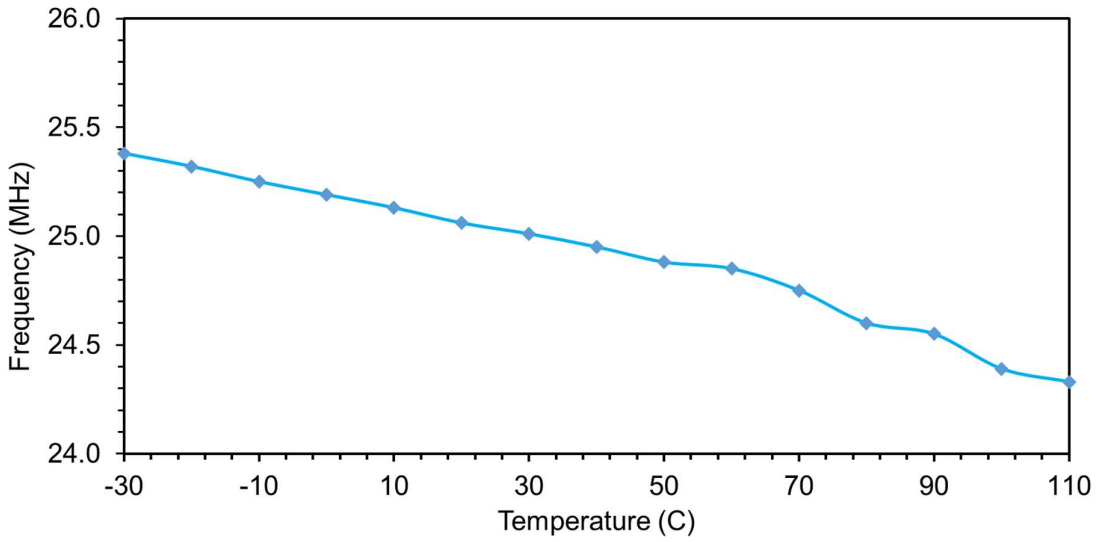


Fig. 4.12. Temperature compensation (25 MHz).

It can be observed that the frequency still has some dependence on the temperature, however, it is much better than in the case of the CC ring oscillator without any compensation. The power consumption of the circuit is 7.5 µW and 15 µW, for 12MHz and 25 MHz, respectively. The startup time is also critical since the clock generator was not always active. The time spent on waking up directly contributes to overall power consumption.

Conclusion

A low-power clock generator in a TSMC 180nm with temperature compensation was presented. The primary function of this circuit is to serve as a cheap (small area and low power consumption) and reliable clock source for the low-power, battery-operated image-sensing platform [4]. Additionally, the duty cycle compensation was implemented. Table 4.1 shows a comparison with similar low-power clock generators [34], [35], [36], [37], [38]. The main advantages of the presented circuit are low power consumption, high power efficiency, and fast wakeup, which makes it suitable for applications where area and low power are critical, while other parameters have somewhat milder system requirements.

Table 4.1. Comparison with the prior art

	This Work	CICC 2021 [30]	ISSCC 2021 [31]	CICC 2022 [32]	VLSI 2019 [33]	JSSC 2019 [34]
Process	180nm	65nm	180nm	65nm	180nm	180nm
Supply Voltage (V)	1.35 – 1.65	1.2	1.8	1/1.8	1.2	0.95
Temperature Range	-30 to 110	-40 to 95	-40 to 85	0 to 80	-20 to 100	-20 to 100
Startup Time	5µs	N/A	N/A	20µs	N/A	N/A
Frequency (MHz)	5 – 32 (10-64)*	100	16	1.5 - 100	13.4	8.2
Power Eff (µW/MHz)	0.6 (0.3)*	1	9.9	7.6@100MHz	11.8	5.6
Power (µW)	7.5/15	101	158.4	575	157.8	46.3
Area (mm^2)	0.019	0.19	0.14	0.072	0.04	0.028
*Frequency is twice as high before duty cycle compensation						

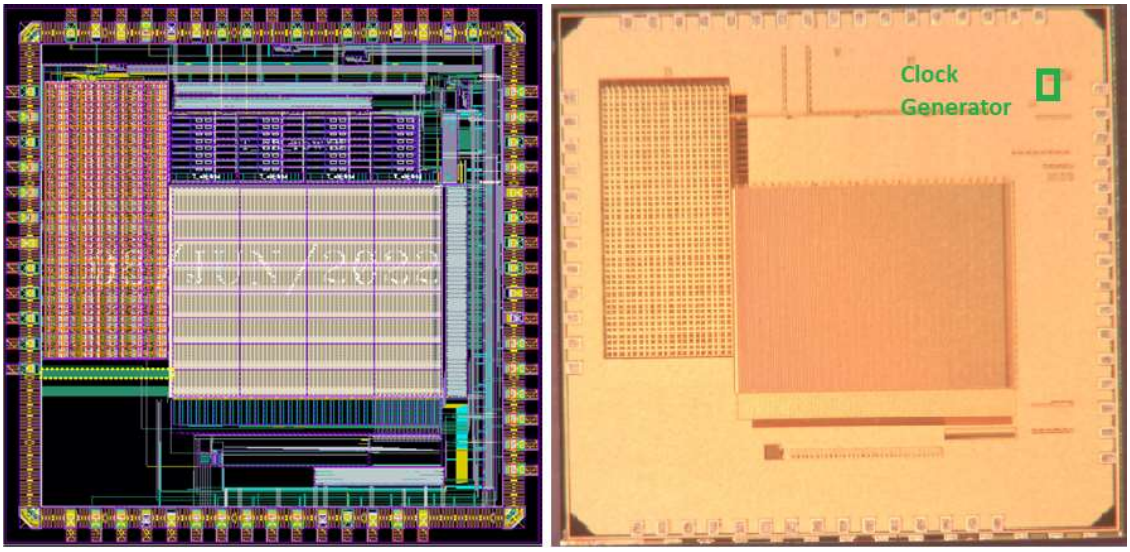


Figure 4.13. shows the silicon photo with the corresponding layout. It can be observed that the clock generator takes up very little space in the whole system.

5. DIGITALLY CONTROLLED FRACTIONAL-ORDER ELEMENTS

Introduction

In recent decades, fractional-order (FO) systems have emerged as a cutting-edge approach in interdisciplinary research. Studies show that FO systems represent continuous-time linear systems more efficiently than integer-order (IO) systems [5], [6]. Based on that fact, FO systems find diverse applications in a variety of fields, such as control theory, material theory, diffusion theory, robotics, signal processing, viscoelasticity, and more.

In the design of the FO filters, the slope of the transition between the passband and stopband is defined by the relationship $20 \cdot (n + \alpha)$, where n is an integer and α is the fractional-order parameter, where $0 < \alpha < 1$. The dependence of the slope on the fractional order α presents an additional degree of freedom and new versatility in filter design.

Due to the irreversible dissipation effects of real electronic components, such as capacitors and inductors, the fractional capacitor is also frequently used in electrical circuit modeling and stability analysis. Due to these dissipative effects, classical integer-order models of electrical circuits cannot accurately describe the complex dynamic behavior of real systems.

Considering the topic of this PhD thesis, an especially interesting application of high-frequency, tunable FOE is the fractional-order switching capacitor DC-DC converter [7,8]. Utilizing the FO capacitor as a Cfly instead of a conventional IO capacitor offers additional degrees of freedom and increases the flexibility of the design in terms of VCR. Since fixed VCR is one of the main disadvantages of conventional (IO) capacitive DC-DC converters (see Table 1.1), and FO capacitors present a promising solution for that problem, the focus of this chapter is the design of fully integrated digitally controlled active FO capacitors.

The application of digitally controllable FOEs (implementing both CPE and FOI) to DC-DC converters operating at high frequencies is beyond the scope of this thesis and will be explored in the future.

Prior research shows that fully integrated active implementations of the FOE work well only at the lower frequency range [39]. The main reason for that lies in the fact that operation transconductance amplifiers (OTAs), used as active components, were not designed for high-speed operation. This type of FO element may find its use in low-frequency applications such as biomedical signal processing, audio signal processing, etc. However, fully integrated DC-

DC converters usually require operation at higher frequencies [1], [2], [9]. This means that a faster and fully integrated FO capacitor needs to be developed for the purpose of fully integrated power management.

The implementation of fractional-order elements, such as an FO capacitor or a constant-phase element (CPE) and an FO inductor (FOI), starts with the transfer function H(s), which represents a differentiator or integrator. It is included in a V/I converter (another OTA), which then converts the transfer function H(s) into a driving point impedance Z(s). It was defined for the first time in [40], and then used in [41]. For low-frequency applications, MOSFETs of the OTAs can operate in the sub-threshold region, consuming lower power but making OTAs slower. However, OTAs used as part of the FO DC-DC converter need MOSFETs in strong inversion, as shown in [5]. The high-frequency range comes at the price of higher power consumption.

If the FOE is built as an active element, it is possible to tune the FOE order with different bias currents for OTAs. In this chapter, the extension of the idea from [39] will be used to tune the parameters of FOEs using digitally controlled bias currents. Additionally, the idea from [39,40] will be utilized to realize integrated FOEs with OTAs operating with MOS transistors in the strong inversion region. The OTAs in this chapter are linearized using source degeneration, as in [42,43]. An optimal operating conditions for the OTAs are presented, and preliminary results of this research can be found in [44].

Fractional-Order Impedance and Transfer Function

Basic Definitions

The description of the FOE, an element required in systems to become FO, is the first step in the process. The approach to realizing FOE is based on [40].

The impedance of the FO capacitor or a constant phase element (CPE) of order $0 < \alpha < 1$ and the pseudo-capacitance C_α with the unit of $[F \cdot s^{\alpha-1}]$, where s is a second, is defined by:

$$Z_{CPE}(s) = \frac{1}{C_\alpha s^\alpha} \tag{5.1}$$

where *s* is the Laplacian operator (complex number).

The impedance of the FO inductance (FOI) of order $0 < \beta < 1$ and the pseudo-inductance L_β $[H \cdot s^{\beta-1}]$ is defined by:

$$Z_{FOI}(s) = L_\beta s^\beta \tag{5.2}$$

Note also that the transfer function:

$$H(s) = (\tau s)^q \tag{5.3}$$

represents the FO integrator when $q < 0$ and represents the FO derivator when $q > 0$, where $0 < |q| < 1$, and the time constant is given by:

$$\tau = \frac{1}{\omega_0} \tag{5.4}$$

In Equation (5.4), ω_0 is the center frequency around which the approximation is usually defined.

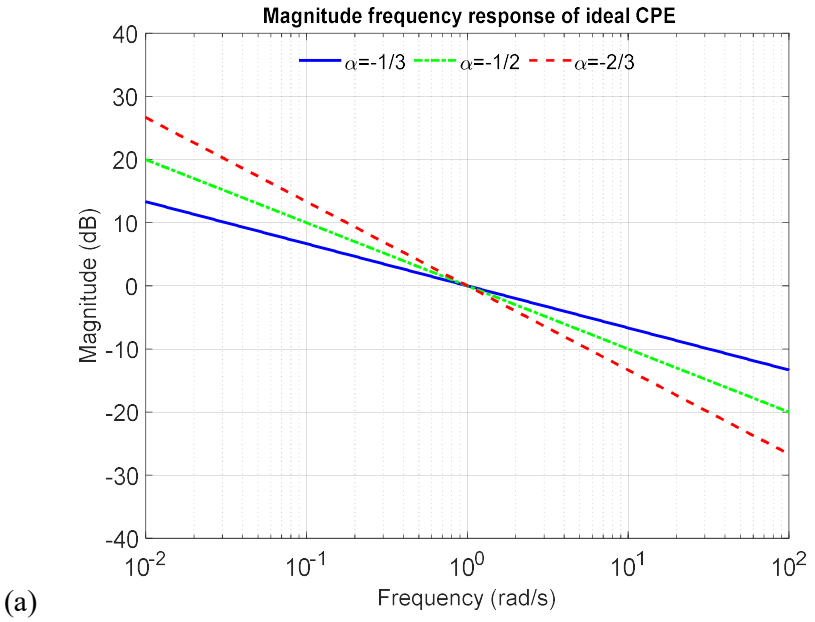
The design equations for a generalized system of order α are obtained by replacing the Laplacian operator s^α in the transfer function of the FO system with its integer approximation.

The example of the nth-order approximation of H(s) in Equation (5.3) in the form of the IO transfer function is given by:

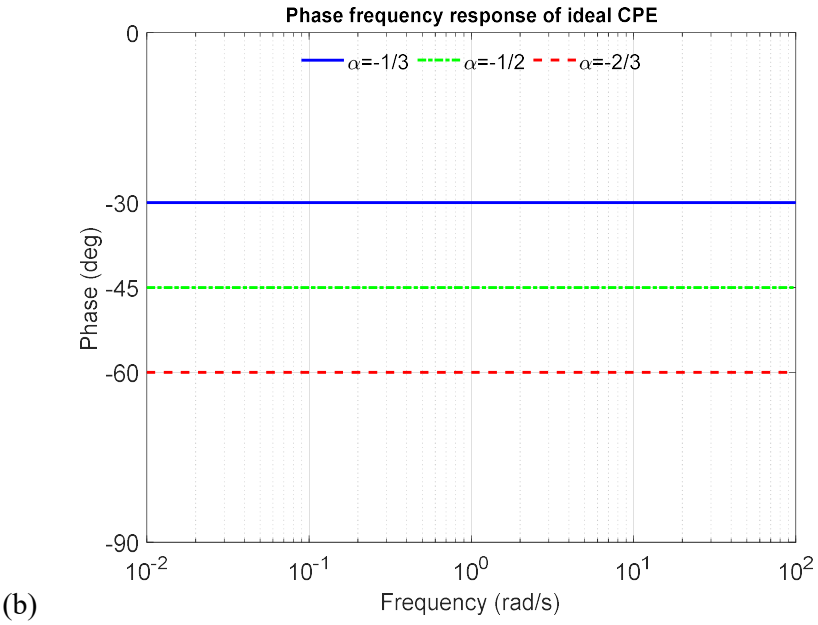
$$H(s) = (\tau s)^\alpha \cong \frac{A_n(\tau s)^n + A_{n-1}(\tau s)^{n-1} + \ldots + A_1(\tau s) + A_0}{B_n(\tau s)^n + B_{n-1}(\tau s)^{n-1} + \ldots + B_1(\tau s) + B_0} \tag{5.5}$$

and it is defined within a few decades around the center frequency ω_0. The IO transfer function H(s) can then be realized with standard IO circuits. If $\tau = 1$ in Equation (5.4), the H(s) is considered normalized.

The magnitude and phase of normalized ideal CPE for $\alpha = -1/3$ ($-30°$), $-1/2$ ($-45°$), and $-2/3$ ($-60°$) are shown in Fig 5.1.



(a)



(b)

Fig. 5.1. (a) Magnitude- and (b) phase-frequency characteristics of normalized ideal CPE for α = −1/3 (−30°), −1/2 (−45°), and −2/3 (−60°).

Approximated Transfer Function H(s) and the Impedance Z(s) of the nth-order

The inverse follow-the-leader (IFLF) multi-feedback topology as in [39,40], constructed using OTAs as active elements and grounded capacitors, is an excellent candidate for the physical realization of H(s) in Equations (5.6) and (5.7) and is shown in Fig. 5.2.

Figure 5.2 shows the IFLF topology, which realizes the voltage transfer function H(s) with a differential input and asymmetrical output.

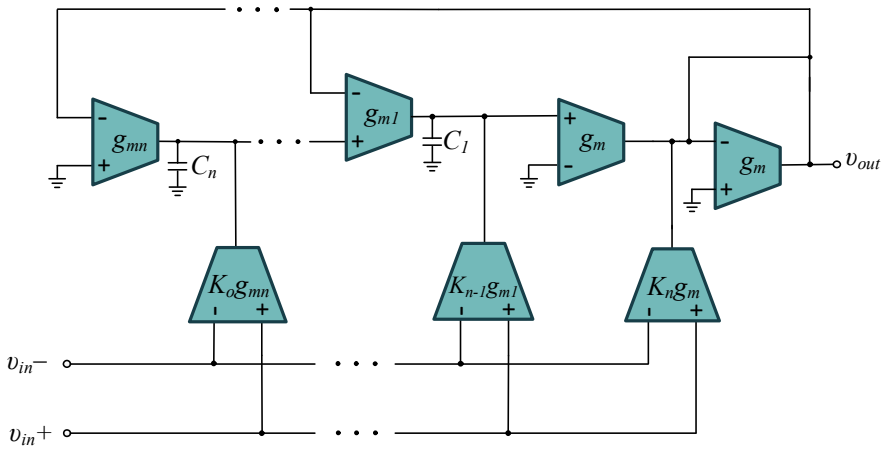


Fig. 5.2. OTA-C implementation of a voltage-excited reconfigurable IFLF structure of an integrator/differentiator with differential input.

The transfer function of the circuit in Fig 5.2 is defined by Equation (5.6):

$$H(s) = \frac{V_{out}(s)}{V_{in\_d}(s)} = \frac{V_{out}(s)}{V_{in+}(s) - V_{in-}(s)} = \frac{G_n s^n + \left(\frac{G_{n-1}}{\tau_1}\right) s^{n-1} + \ldots + \left(\frac{G_0}{\tau_1 \tau_2 \cdot \ldots \cdot \tau_n}\right)}{s^n + \left(\frac{1}{\tau_1}\right) s^{n-1} + \ldots + \left(\frac{1}{\tau_1 \tau_2 \cdot \ldots \cdot \tau_n}\right)} \qquad (5.6)$$

where Vout, Vin+, and Vin− are small signal quantities designated in Fig. 5.2. Note that the differential input is defined by Vin_d =Vin+ − Vin−. The emulation scheme for Z(s) shown in Fig. 5.3 realizes a floating impedance, as shown in [22].

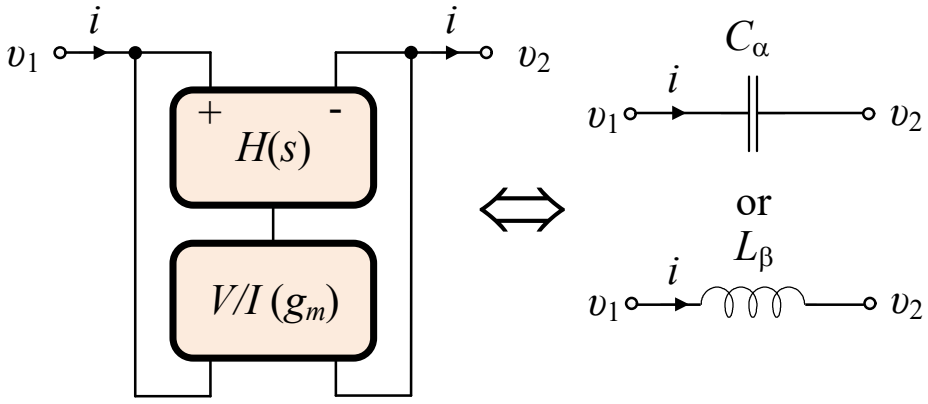


Fig. 5.3. Emulator for the implementation of the voltage-excited floating input impedance from the transfer function H(s) [41].

The input impedance Z(s) of the emulator, which realizes the floating impedance in Fig. 5.3 from the transfer function H(s) shown in Fig. 5.2, is given by:

$$Z(s) = \frac{V_1(s)}{I(s)} = \frac{1}{g_{mVI} \cdot H(s)} \tag{5.7}$$

If Equations (5.1) and (5.7) are compared, the value of the emulated pseudo-capacitance can be obtained:

$$C_\alpha = g_{mVI} \cdot \tau^\alpha \tag{5.8}$$

Figure 5.3 shows the emulation of voltage-excited fractional-order capacitor and inductor impedances, but this topology cannot emulate the current-excited behavior of fractional-order impedances.

In the next section, it will be shown that the design of the IFLF multi-feedback FOE with OTA-C, as shown in Fig. 5.2, requires transconductances (gm) and capacitances (Cs) to be very large for a given frequency range. Therefore, the simplest single-stage OTAs are used, which have moderate MOSFET dimensions and bias currents to save space and power consumption. The goal is to minimize the spread of gm values and use as many identical OTAs as possible in the circuit. The topology that suggests the same value for gm in as many OTAs as possible will be used. Different capacitance values (C1 and C2) are preferable in the design to obtain as many identical OTAs as possible with minimal gm dispersion.

Design Procedure

The FOE circuit is designed for $\alpha = -1/2$, with the center frequency $f_0 = 50$ kHz and the CPE capacitance $C = 500$ pF at f_0. In this thesis, the recently introduced minimax approximation published in [12] is used for the calculations of the minimax coefficients. A minimax approximation used in the design was developed to cover the bandwidth BW = $\omega_H/\omega_L = 50$. The coefficients of $H(s)$ for the second-order minimax approximation (MMX) for the three values of $\alpha = 1/3$, 1/2, and 2/3 are given in Table 5.1.

Table 5.1. Second-order MMX approximation for three positive $\boldsymbol{\alpha}$ values and normalized frequency ω0 = 1.

α (Ø°)	MMX
1/3 (30°)	$\frac{2.83673s^2 + 7.45924s + 1}{s^2 + 7.45924s + 2.83673}$
1/2 (45°)	$\frac{5.03262s^2 + 10.4397s + 1}{s^2 + 10.4397s + 5.03262}$
2/3 (60°)	$\frac{9.85595s^2 + 16.1252s + 1}{s^2 + 16.1252s + 9.85595}$

A step-by-step design of the CPE can be conducted as follows:

(i) For V/I converter: CPE capacitance at f_0 = 50 kHz is C = 500 pF, and therefore its transconductance is $g_{mVI} = C/\tau = C \cdot \omega_0 = 157.08$ μS, where $\omega_0 = 2\pi f_0$.

(ii) For α = 1/2 (45°) from f_0 = 50 kHz, $\tau = 1/\omega_0 = 1/(2\pi f_0) = 3.1831 \cdot 10^{-6}$ s. Using $\tau = 3.1831 \cdot 10^{-6}$ s and Table 5.1 denormalized $H(s)$ can be obtained:

$$H(s) = (\tau s)^{\frac{1}{2}} = \frac{5.03262s^2 + 3.27974 \cdot 10^6 s + 9.8696 \cdot 10^{10}}{s^2 + 3.27974 \cdot 10^6 s + 4.967 \cdot 10^{11}} \quad (5.9)$$

(iii) Including g_{mVI} = 157.08 μS and Equation (5.9) into the Equation (5.6), fractional capacitance can be obtained:

$$Z(s) = \frac{1}{1578.08 \cdot 10^{-6}} \frac{s^2 + 3.27974 \cdot 10^6 s + 4.967 \cdot 10^{11}}{5.03262\, s^2 + 3.27974 \cdot 10^6 s + 5.03262 \cdot 10^{10}} \quad (5.10)$$

The denormalized upper and lower limits of the usable frequency range are f_H = 350 kHz and f_L = 7 kHz, while f_0 = 50 kHz. The parameters of the IFLF circuit are calculated using the design Equation (5.6) compared to Equation (5.5). For the second-order, as in this case, the following parameters can be obtained:

$$G_2 = \frac{A_2}{B_2};\ G_1 = \frac{A_1}{B_1};\ G_0 = \frac{A_0}{B_0};\ \tau_1 = \frac{B_2}{B_1};\ \tau_2 = \frac{B_1}{B_0} \tag{5.11}$$

$$g_{m1} = \frac{C_1}{\tau_1};\ g_{m2} = \frac{C_2}{\tau_2} \tag{5.12}$$

For judiciously chosen capacitances of C1 = 10 pF and C2 = 216.563 pF, the Equation (5.12) can be used to obtain equal values of g_m for $\alpha = 1/2$ (45°). The parameters for the IFLF structure are given in Tables 5.2 and 5.3.

Table 5.2. Second-order MMX approximation (C = 500 pF @ 50 kHz) τi and Gi.

α (Ø°)	-1/3 (-30°)	-1/3 (-30°)	-2/3 (-60°)
τ_1	0.426732 µs	0.304902 µs	0.1974 µs
τ_1	8.37003 µs	6.60306 µs	5.208 µs
G_2	2.83673	5.03262	9.85595
G_1	1	1	1
G_0	0.352519	0.198704	0.10146

Table 5.3. Second-order MMX approximation (C = 500 pF @ 50 kHz) gmi and Ci.

α (Ø°)	OTA	-1/3 (-30°)	-1/2 (-45°)	-2/3 (-30°)
g_{m1}	#3	23.434 µS	32.797 µS	59.659 µS
g_{m2}	#1, 2, 4	25.847 µS	32.797 µS	41.584 µS
G_0g_{m2}	#5	9.1209 µS	6.517 µS	4.219 µS
G_1g_{m2}	#6	25.874 µS	32.797 µS	41.584 µS
G_2g_{m2}	#7	73.39 µS	165.057 µS	409.85 µS
g_m, V/I	#8	157.08 µS	157.07 µS	157.08 µS
C_1	-	10 pF	10 pF	10 pF
C_2	-	216. 56 pF	216. 56 pF	216. 56 pF
Pseudo-cap C_α		2.31 µF/s$^{0.67}$	280.25 nF/s$^{0.5}$	34.0 nF/s$^{0.33}$

The proposed, high-speed OTAs are also referred to as gm cells with different gm values. OTAs (gm cells) are single-stage amplifiers for stability reasons and have a high output impedance because of built-in cascodes. Source degeneration of the input differential pair is implemented by two MOSFETs operating in the triode region (see [42,43] and Section 14.1 in [45]). The wide-swing current mirrors are used to save headroom (see Section 6.3.1 in [46]).

The nominal voltage supply is 4V with a tolerance of +/- 0.5V (typical for the AMS 0.35 technology). The definition of the required bias currents (Ibias) is conducted first. Note that bias currents need to be in the acceptable range for each OTA to achieve the required transconductances (Table 5.3).

Source degeneration also reduces the resulting OTA transconductance compared to input MOSFET transconductance. The optimum ratio between the dimensions of the input MOSFETs and the dimensions of the degeneration MOSFETs (degeneration MOSFETs operate in the triode region) is $N=(W/L)_{input}/(W/L)_{deg} = 6.7$.

The calculation of the transconductances gm1,2 of the OTA input pair MN1,2 based on the required OTA transconductance gm is conducted. For example, to implement gm7=165.057 µS of OTA #7 in Fig. 5.4, an input pair with gm1,2 = 2.675·165.057 µS = 441.53 µS in the electronic realization of the OTA is needed. This is a fairly high value.

To realize the given value of the transconductance, the decision between an NMOS or PMOS differential input stage needs to be conducted depending on the selected bias current Ibias and the acceptable dimensions of the input transistors. PMOS input differential pairs were used for a low transconductance value, while NMOS input differential pairs were used for a medium transconductance value. To achieve a high gm value and obtain a reasonable bias current, an NMOS input differential pair and a symmetric CMOS OTA (see Chapter 7 in [47] and [48]) will be used. This means that three basic topologies of OTAs were used in the design, all of which are required to keep the bias currents within reasonable values. Four versions of OTAs are distinguished: OTA1 through OTA4. OTA1 and OTA2 are used for the realization of medium gm and have the same topology as shown in Fig. 5.4 but differ only in the dimensions of the input NMOS differential pair. OTA3, shown in Fig. 5.5, has a symmetrical CMOS OTA topology and is used for high gm values. OTA4, shown in Fig 5.6, realizes the low gm values and, therefore, has a PMOS input differential pair.

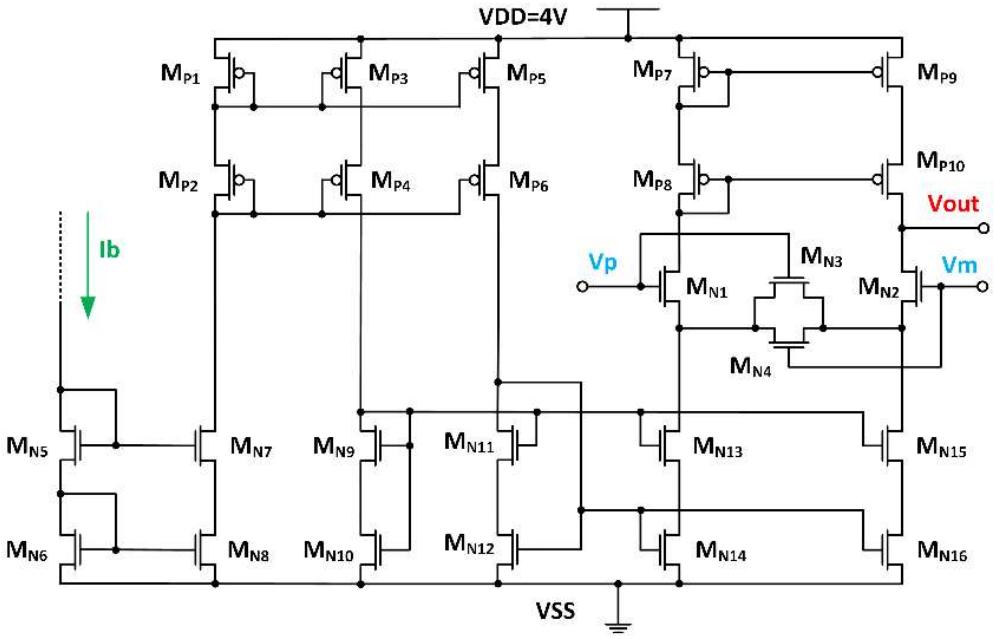


Fig. 5.4. OTA1 and OTA2 schematic.

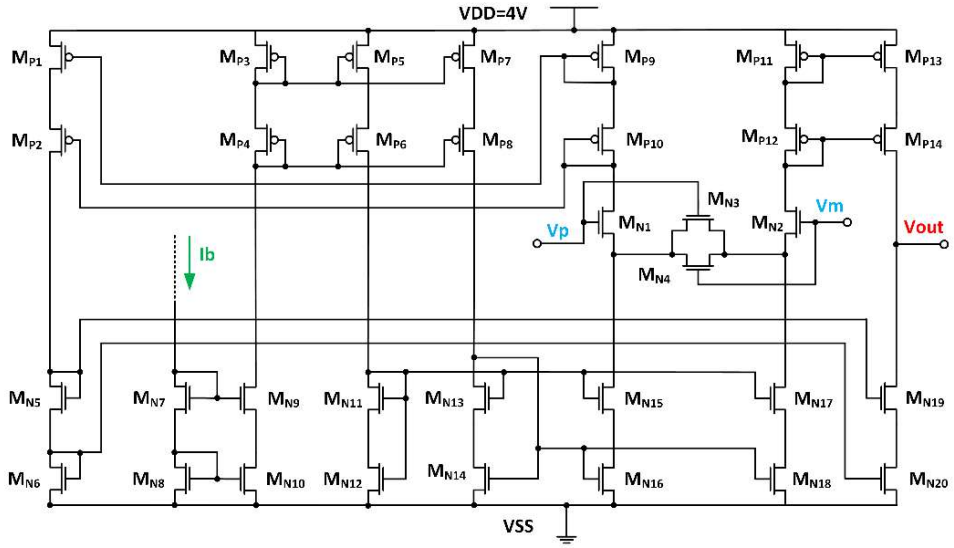


Fig. 5.5. OTA3 schematic.

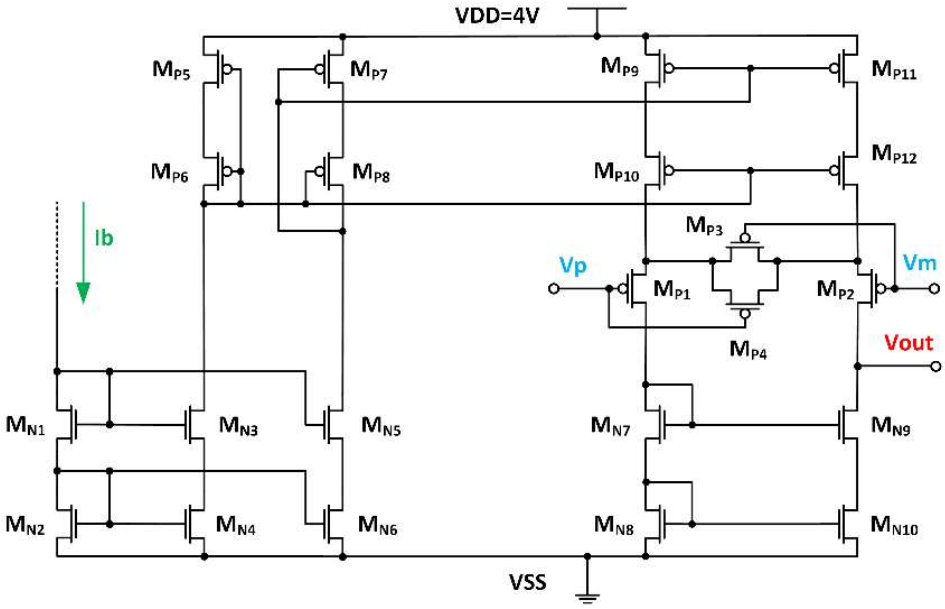


Fig 5.6. OTA4 schematic.

The extracted parameters of the AMS 0.35µm technology are: for NMOS, K'n = µnCox = 117 µA/V2, VTn = 0.507 V, and λn = 0.05 V^{-1}, and for PMOS, K'p = µpCox = −42 µA/V2, VTp = −0.697 V, and λn = −0.08 V^{-1} [12].

Calculated and simulated W/L values [12] can be found in Tables 5.4 – 5.6. Three groups of OTAs were obtained. Tuning for different CPE angles is performed by changing Ibias with all MOSFETs operating safely in saturation. The needed bias currents to obtain the required transconductances from Table 5.3 for different orders α can be found in Table 5.7. To reduce the spread of Ibias currents, OTAs with higher transconductances need to be used. In the previous publication in [44], only one type of OTA was used. The critical bias current range is between the maximum of 280µA and the minimum of 0.9µA (ratio higher than 300). In the design, where different OTA topologies were chosen, the ratio between the maximum and minimum required bias current is 10, which is a 30-fold improvement. The dimensions of the MOSFETs in OTAs are given below in Tables 5.4 – 5.6. The final topology of the realized CPE is shown in Fig. 5.7.

Table 5.4. MOSFET transistor dimensions of OTA1 and OTA2 (NMOS INPUT).

MOSFET	Aspect Ratio OTA-1	Aspect Ratio OTA-2
$M_{P1} - M_{P10}$	20μm/1μm	20μm/1μm
$M_{N1} - M_{N2}$	14.4μm/2μm	9μm/2μm
$M_{N3} - M_{N4}$	2.1μm/2μm	1.4μm/2μm
M_{N9}	2μm/1μm	2μm/1μm
$M_{N5} - M_{N8}$, $M_{N10} - M_{N16}$	10μm/1μm	10μm/1μm

Table 5.5. MOSFET transistor dimensions of OTA3 (NMOS INPUT).

MOSFET	Aspect Ratio OTA-3
$M_{P1} - M_{P2}$, $M_{P13} - M_{P14}$	100μm/1μm
$M_{P1} - M_{P12}$	20μm/1μm
$M_{N1} - M_{N2}$	20μm/2μm
$M_{N3} - M_{N4}$	3μm/2μm
$M_{N5} - M_{N6}$, $M_{N19} - M_{N20}$	50μm/1μm
M_{N12}	2μm/1μm
$M_{N7} - M_{N11}$, $M_{N13} - M_{N18}$	10μm/1μm

Table 5.6. MOSFET transistor dimensions of OTA4 (PMOS INPUT).

MOSFET	Aspect Ratio OTA-4
$M_{P1} - M_{P2}$	3μm/2μm
$M_{P3} - M_{P4}$	1μm/4.5μm
M_{P5}	4μm/1μm
$M_{P6} - M_{P12}$	20μm/1μm
$M_{N1} - M_{N10}$	10μm/1μm

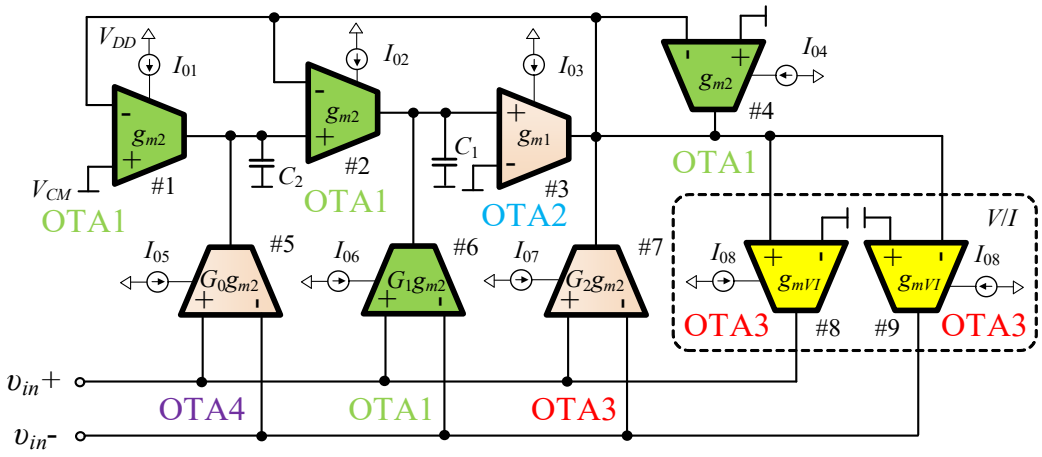


Fig. 5.7. Final OTA-C emulation scheme for the voltage-excited floating FO capacitor.

To reduce the influence of the process and mismatch, the input differential pair has been designed in the form of a common centroid (ABBA/BAAB).

The capacitors are realized as linear "cpoly" capacitors, whereby C1 is an 8×8 array of 64 unit cells with a capacitance of 156.25 fF (12.85µm × 13.7µm) and thus forms 10.0 pF. Capacitor C2 is a 25×25 array of 256 unit cells with a capacitance of 346.6 fF (19.5µm × 20.25µm) and thus forms 216.56 pF.

Table 5.7 shows bias currents (Ibias) for individual OTAs:

Table 5.7. Table of bias currents.

α (Ø°)	OTA	-1/3 (-30°)	-1/2 (-45°)	-2/3 (-30°)
I_{01}	#3 (OTA2)	4.6 µA	8 µA	17.4 µA
I_{02}	#1, 2, 4 (OTA1)	4 µA	5.6 µA	8 µA
G_0I_{02}	#5 [a](OTA4)	7.2 µA	4 µA	2 µA (descending)
G_1I_{02}	#6 (OTA1)	4 µA	5.6 µA	8 µA
G_2I_{02}	#7 [b](OTA3)	1.7 µA	5 µA	21.4 µA
I_0, V/I	#8, 9 (2xOTA3)	1 µA	1 µA	1 µA
[a] For OTA #5, which has small transconductance values, OTA with PMOS input pair was used. [b] For OTA #7, which has high transconductance values, current multiplier x5 was used.				

The circuit in Fig. 5.8 is used to provide bias currents. The main bias generation circuit (blue block) is used to generate a stable bias current, which is later mirrored (green block) with a

factor suitable for the individual OTAs. Since each OTA needs three different currents to implement different phases (-30°, -45°, and -60°), the mirroring factor can be digitally controlled with 2 bits (T1 and T2). A manual startup was implemented as a failsafe mechanism to ensure the necessary initial conditions.

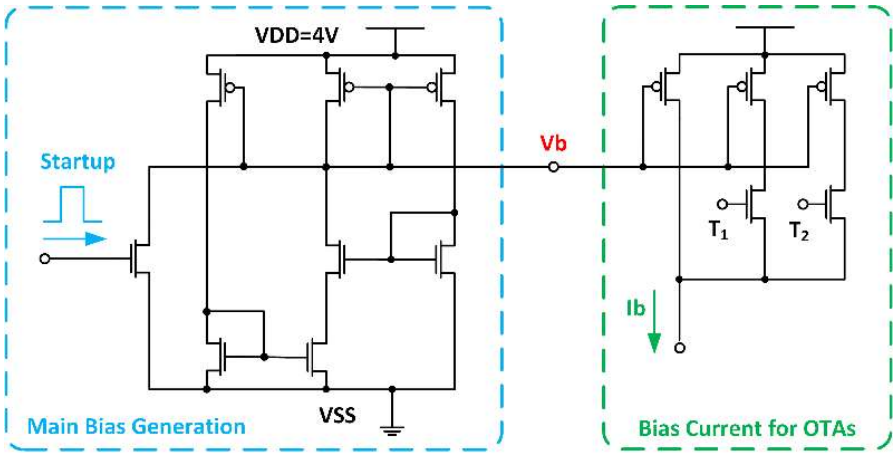


Fig. 5.8. Bias current generation.

The whole system was implemented in the AMS 350 nm technology node using Cadence Virtuoso tools for the design process. Figure 5.9 presents the layout showing the size and location of the subcircuits, indicating a total area of 710 × 1127 µm2. The post-layout study with corresponding simulated results was conducted as a proof of concept, and it is presented in the next section.

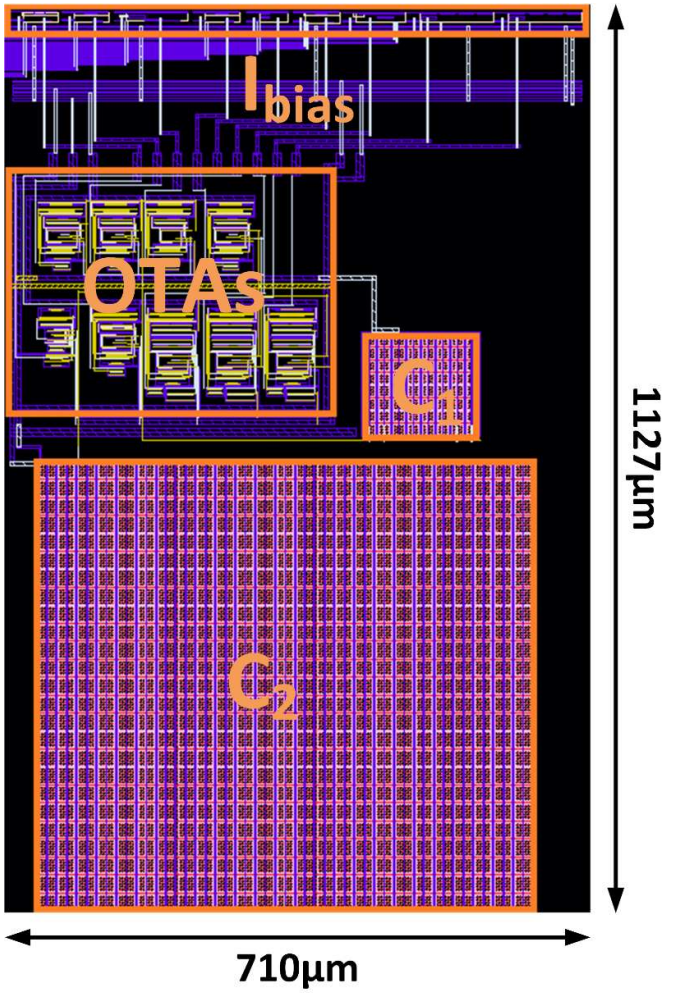


Fig. 5.9. Layout with block dimensions and floorplan.

Simulated Post-Layout Results

AC Analysis

The post-layout (solid) and pre-layout (dashed) results of the AC analysis are demonstrated in Fig. 5.10. Figure 5.10a shows the magnitude-frequency characteristics of the implemented CPE element for three characteristic angles (−30°, −45°, and −60°). It can be observed that the slope by which magnitude falls with frequency corresponds with the implemented angle. For the classical capacitor, the slope would always be −20 dB per decade. Since the fractional order capacitors are presented, slopes are −6.67 dB, −10 dB, and −13.33 dB per decade for -30°, -45°, and -60°, respectively. The phase-frequency characteristics for three implemented angles are shown in Fig. 5.10b. A difference between post-layout and pre-layout data can be observed only at higher frequencies due to the additional parasitic capacitors introduced in the form of metal lines that connect elements. The difference between post-layout and pre-layout

simulations is not significant, as the FOC emulator circuit under consideration is quite simple. Note that demonstrated fractional elements operate as such only within a certain frequency range, resulting from the approximation.

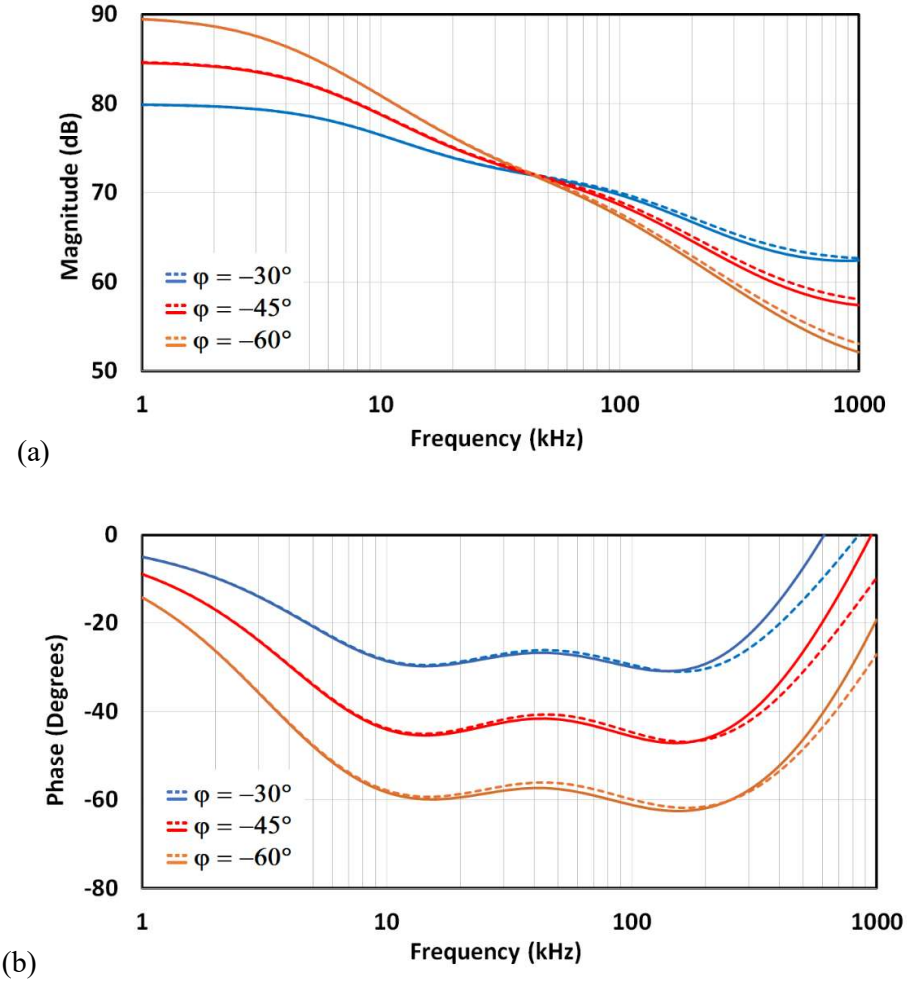


Fig. 5.10. (a) Magnitude- and (b) phase-frequency characteristics (φ = −30°, −45°, −60°). The dashed lines represent the pre-layout analysis, while the solid lines represent the post-layout analysis.

Transient Analysis

Figures 5.11 – 5.13 present the results of the post-layout transient analysis. The circuit was tested for each angle with a sine wave of 50 kHz (the central frequency within an operating range) and a 20mV peak-to-peak amplitude. As expected, the corresponding phase shift between input voltage and input current was observed (−30°, −45°, and −60°). Since the

amplitude of the input signal is relatively small and the OTAs used for the approximation are linear in this range, the input current distortion cannot be noticed.

Since the emulator of the CPE is a voltage-excited type, the excitation is defined by the voltage source in the form of an input voltage, and the response is in the form of a current waveform at the same input port as the driving-point impedance under test. The transient analysis enables comprehensive testing and simulation of the circuit's operation, including all parasitic effects and a large number of parameters, in contrast to AC analysis, which uses simplified small signal simulation and could sometimes be misleading. The results of the transient analysis confirm the correct operation of the circuit and the correct phase shift of the current at the input in response to the excitation in the form of a voltage at the same input terminal.

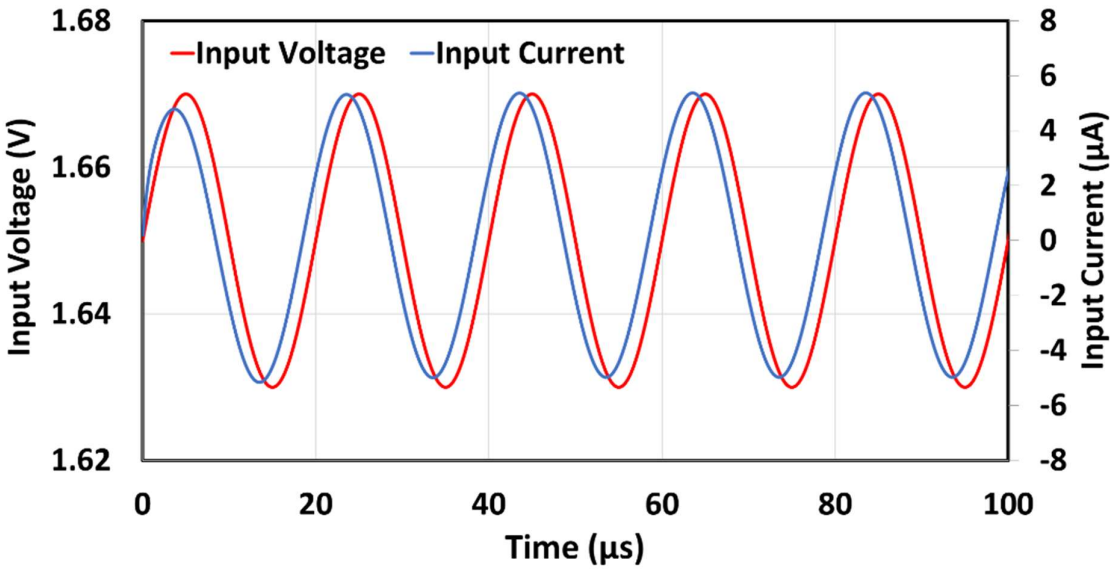


Fig. 5.11. Transient analysis (φ = −30°).

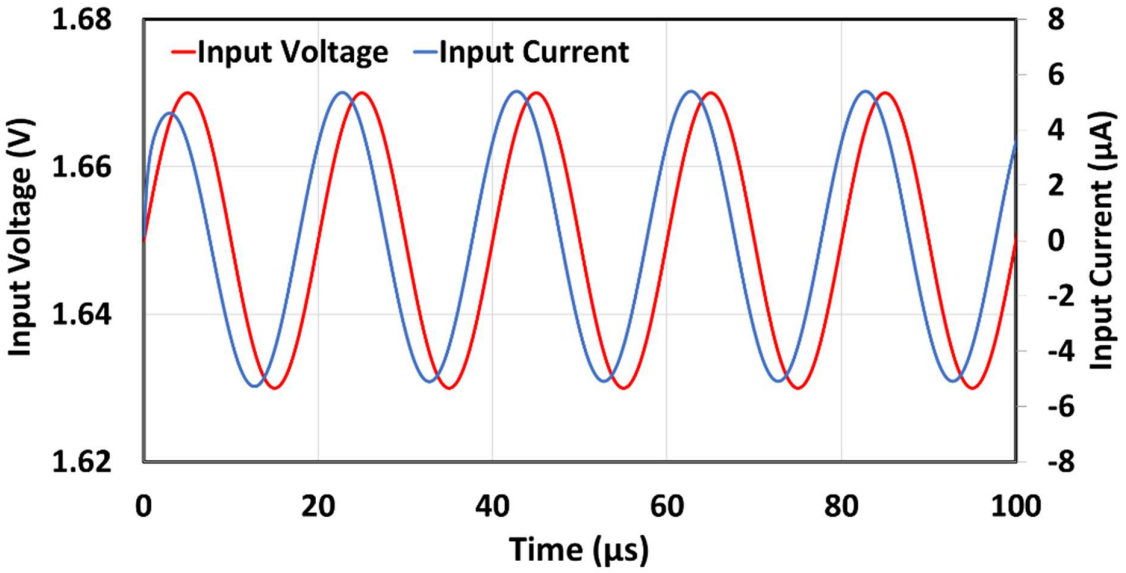


Fig. 5.12. Transient analysis (φ = −45°).

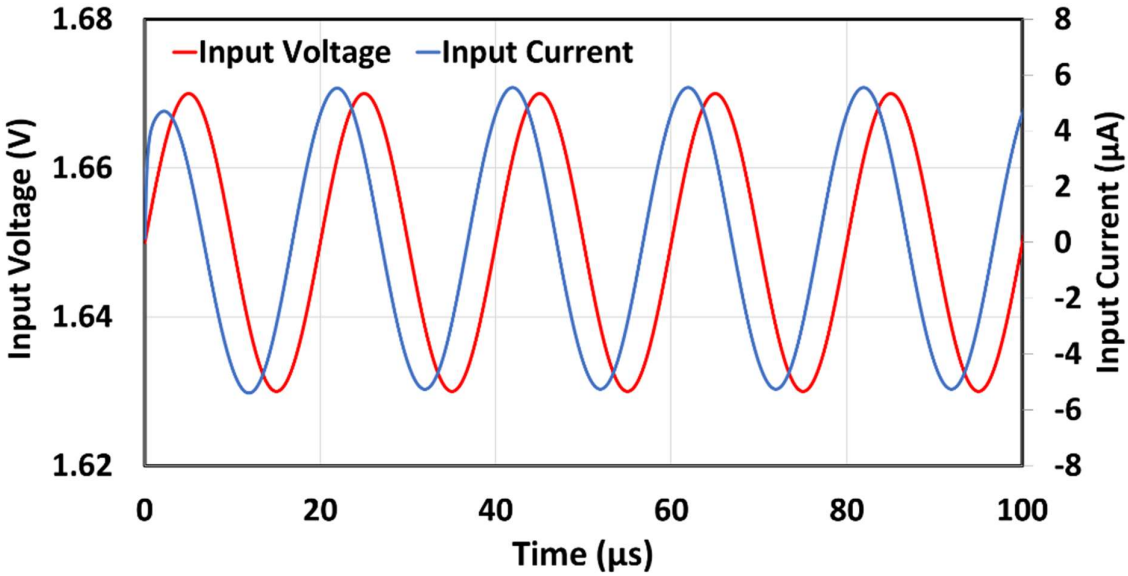


Fig. 5.13. Transient analysis (φ = −60°).

PVT Corner Analysis

The PVT corner analysis was conducted for the extreme cases in the process (ss, ff, sf, fs), temperature (−10 °C and 110 °C), and supply voltage (3.5 V and 4.5 V). The resulting magnitude-frequency and phase-frequency characteristics for the implemented angles are shown in Figs. 5.14 – 5.19. It can be observed that the dispersion of the characteristics is lower as the angle is closer to -90°, i.e., a classical capacitor. Further investigation showed that the

supply voltage has very little effect on the characteristics, so the process and temperature are the main contributing factors to the dispersion.

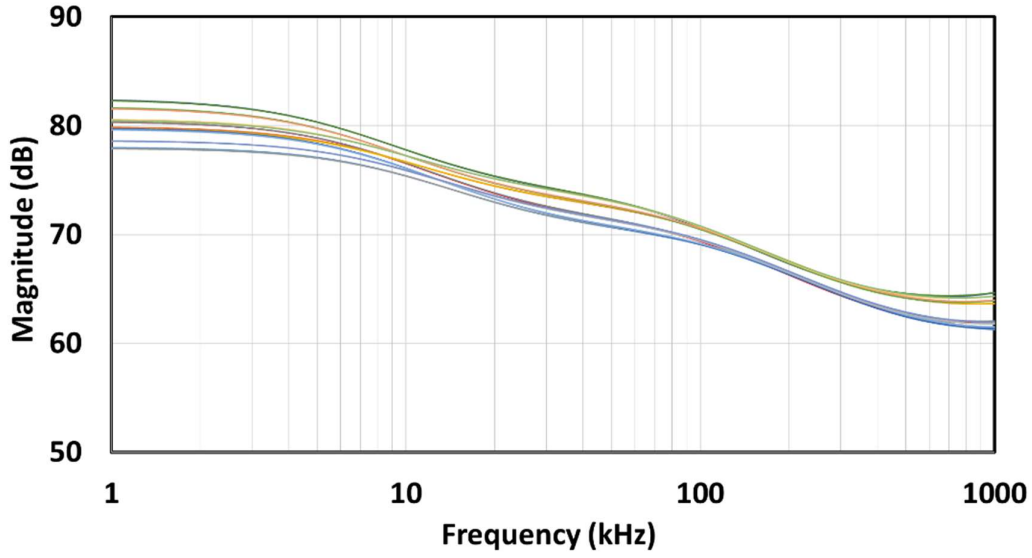


Fig. 5.14. Magnitude-frequency characteristics (φ = −30°).

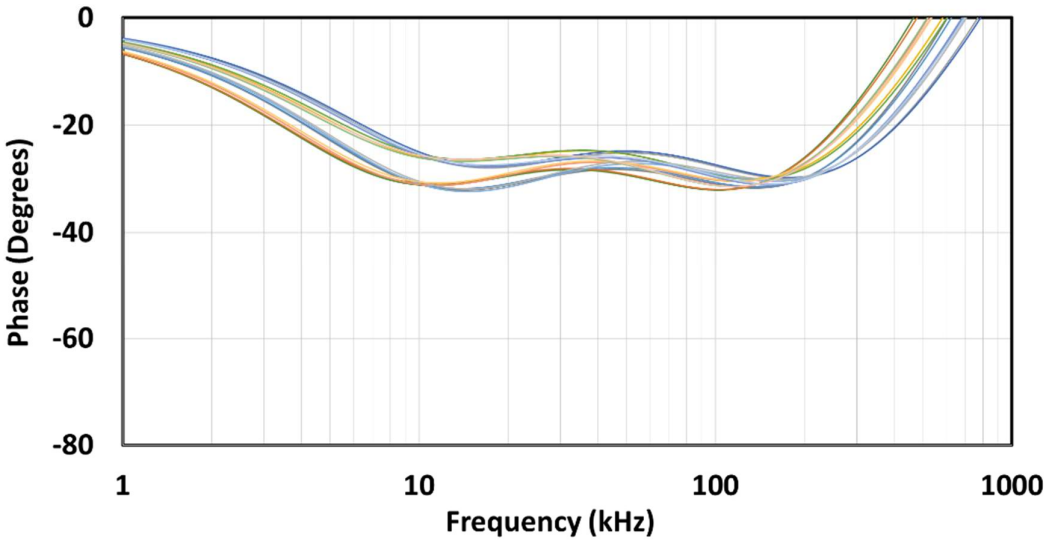


Fig. 5.15. Phase-frequency characteristics (φ = −30°).

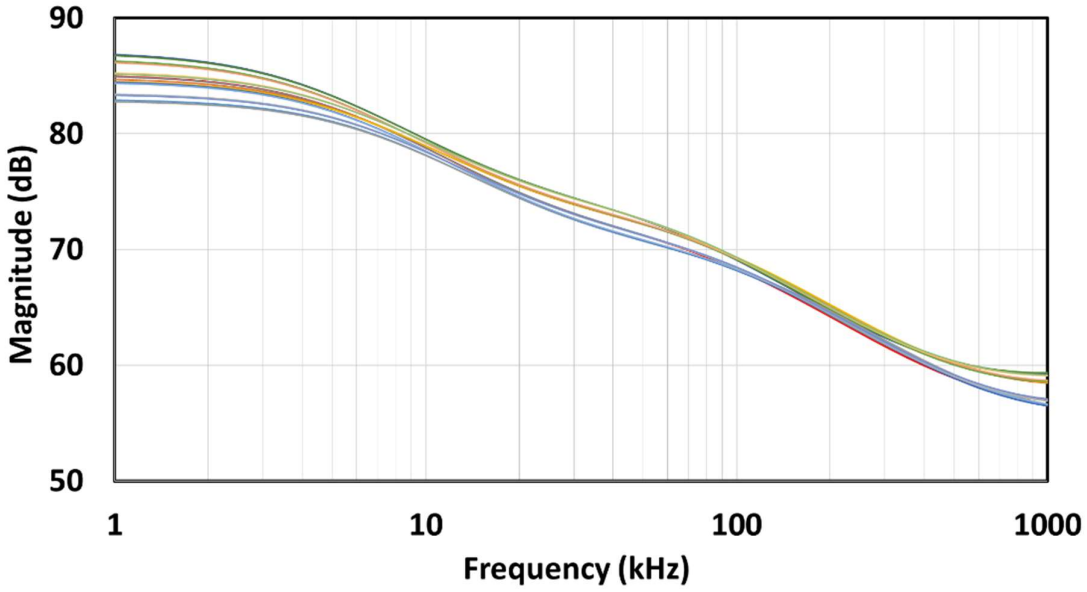


Fig. 5.16. Magnitude-frequency characteristics (φ = −45°).

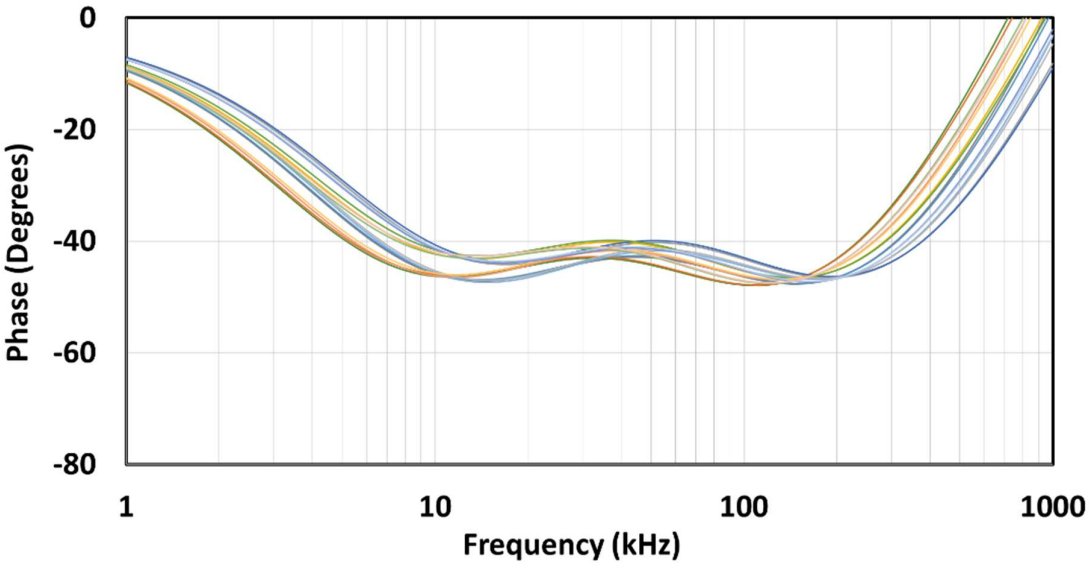


Fig. 5.17. Phase-frequency characteristics (φ = −45°).

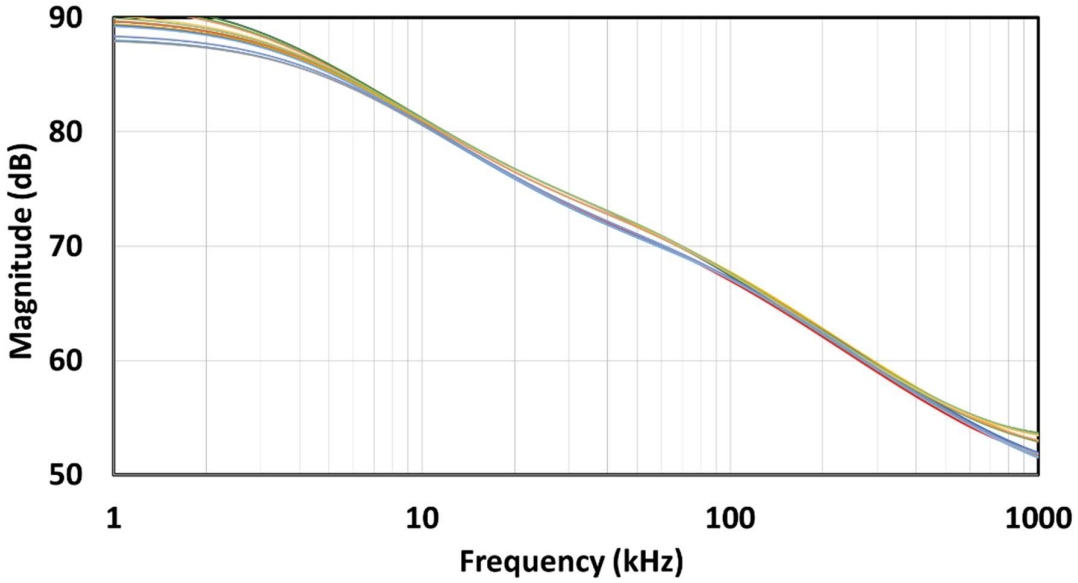


Fig. 5.18. Magnitude-frequency characteristics (φ = −60°).

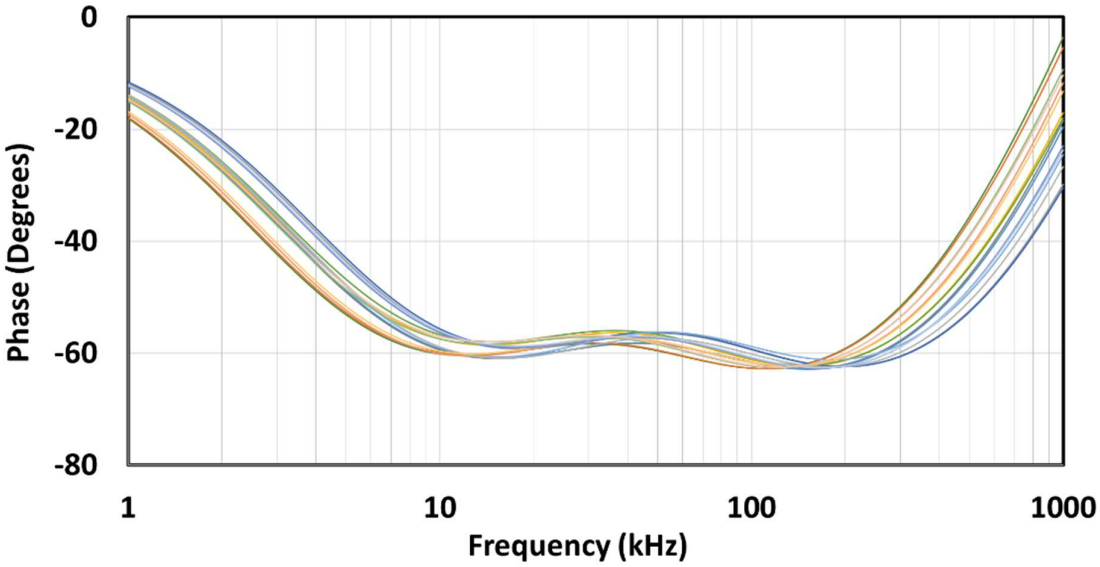


Fig. 5.19. Phase-frequency characteristics (φ = −60°).

Monte Carlo Analysis

As an important part of the verification process, the Monte Carlo (MC) analysis for process and mismatch combined was conducted (100 samples for each angle). The results, presented in Figs. 5.20 – 5.22 are in the form of histograms, showcasing the variations in average phase shifts. The MC results also indicate greater variations as the angle is further away from 90°.

The observed standard deviations, a key measure of the variations, are 2.696 °, 2.083 °, and 1.425 ° for angles of -30 °, -45 °, and -60 °, respectively.

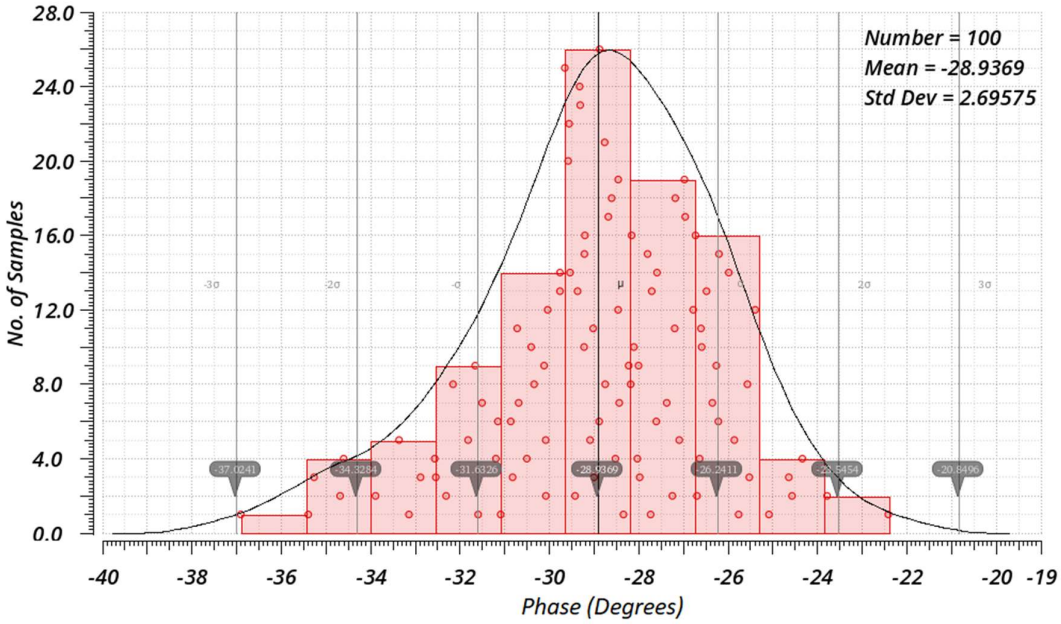


Fig. 5.20. MC variations due to process and mismatch (φ = −30°).

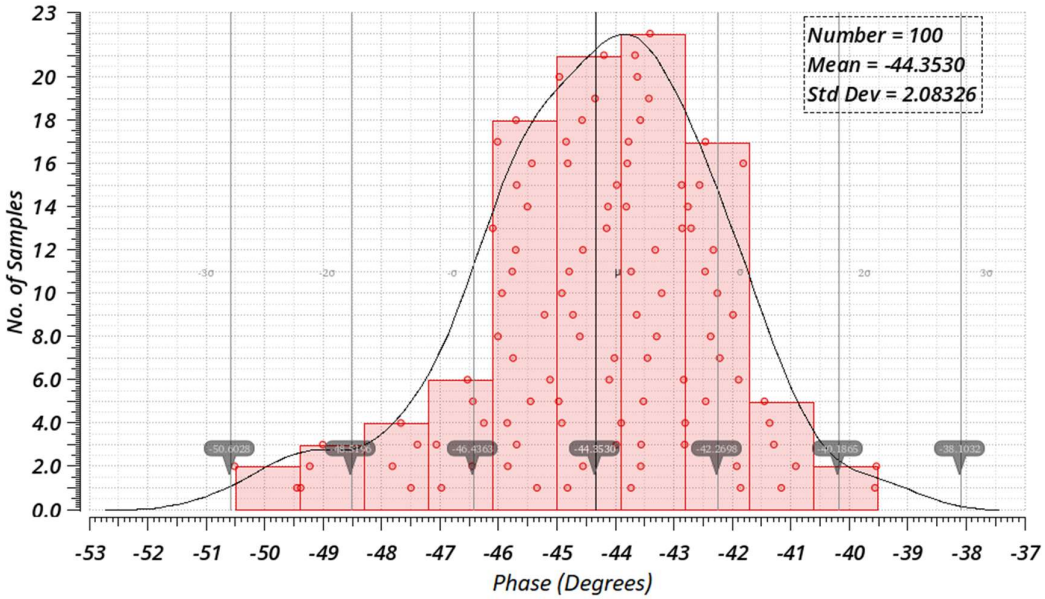


Fig. 5.21. MC variations due to process and mismatch (φ = −45°).

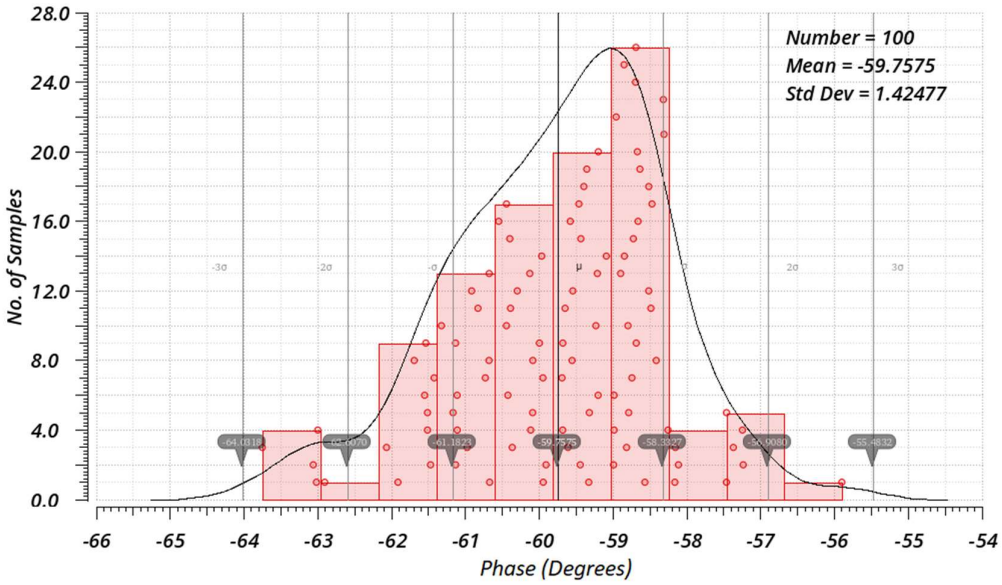
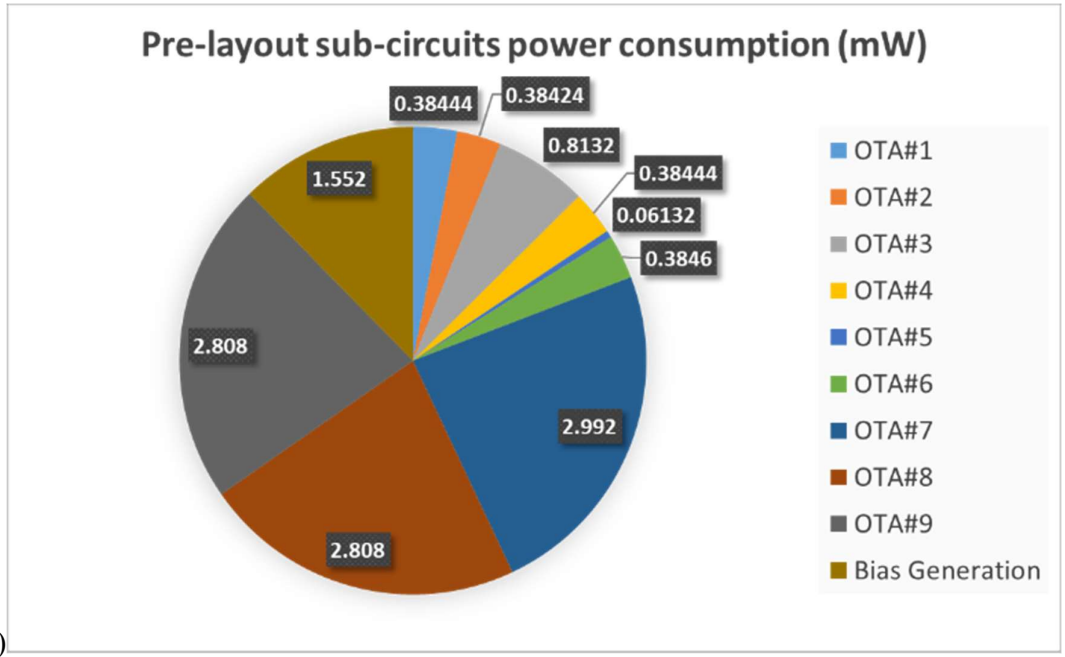


Fig. 5.22. MC variations due to process and mismatch (φ = −60°).

Power Consumption

The power consumption of the entire system is 12.37 mW (12.57 mW pre-layout). Figure 5.23 shows the power consumption of the individual sub-circuits for pre-layout (Fig. 5.23a) and post-layout (Fig. 5.23b) analysis.

(a)



(b)

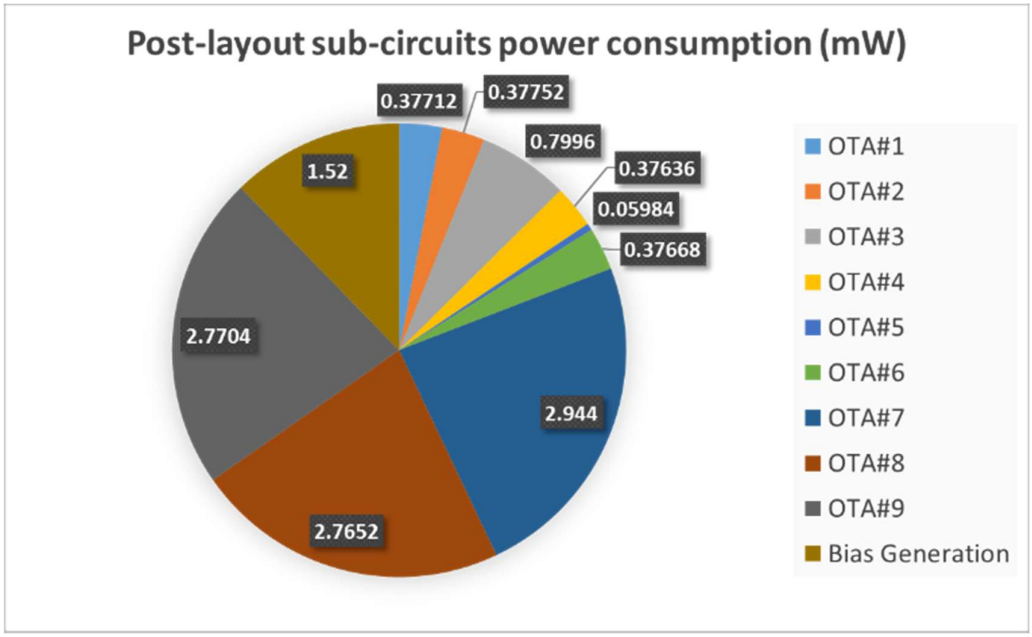


Fig. 5.23. Power consumption of the individual sub-circuits. (a) Pre-layout. (b) Post-layout.

It can be observed that most of the power (together, 68%) is consumed by OTA#7, OTA#8, and OTA#9 (all of type OTA3). The generation of the bias current also consumes a significant part of the power (12%), while the other OTAs together consume the rest (20%). There are slight differences between the results of the pre-layout and post-layout values. The results presented were simulated at the center frequency (50 kHz) and at an angle of −60°, which is the worst angle for power consumption due to the highest bias currents. Note that the power consumption is slightly lower in the post-layout simulations because some parasitics limit the current spikes drawn from the VDD.

Conclusion

This Chapter presents the design of a constant-phase element realized with active elements such as OTAs and grounded capacitors. The OTAs are designed in a linearized version with all transistors in strong inversion. This approach is suitable for operation at high frequencies. The phase is tunable by changing the bias currents for each OTA. The digital tuning scheme has been proposed for the first time. There are various one-stage OTAs in use that achieve a very reasonable ratio between Ibias values, with a maximum ratio of 10. The post-layout simulation results in Cadene Virtuoso confirmed the feasibility and functionality of the proposed approach. In previous works, authors have developed OTA-C CPE with sub-threshold MOSFETs. Therefore, the contribution is achieved through an investigation of OTA-C CPE with

MOSFETs in strong inversion, operating at high frequencies, and digitally controlled, which has been successfully demonstrated.

Future research topics include the construction of electronically controlled OTA-C constant-phase elements in which a large number of parameters, such as center frequency, impedance, and element order, can be controlled in fine steps. The design of digitally controllable FOEs (implementing both CPE and FOI in all four quadrants) operating at high frequencies and increasing the approximation order to higher than two is also a future research topic.

6. CONCLUSION

The scientific contribution to the field of integrated power management was conducted in two main aspects: power efficiency and speed. Four distinct integrated circuits were designed: a step-down DC-DC converter in TSMC 65nm, a boost DC-DC converter in TSMC 180nm, a low-power clock generator in TSMC 180nm, and a digitally controlled fractional-order capacitor in AMS 350nm. The results were measured and partially published [4], [10], [11], [12]. This thesis includes some content that has not yet been published, mainly concerning the low-power clock generator. The main scientific contribution, both in the aspect of power efficiency and speed, is described in Chapter 2 and published as a conference paper [10] with journal extension [11]. An inverter-based step-down DC-DC converter is demonstrated as a state-of-the-art by its peak EEF of 66%, power density of 2.56 mW/mm^2, and by the fast transient response that shows no droops or overshoots. The speed of the presented DC-DC converter enables it to operate with a minimal decoupling capacitor of 50pF, which saves silicon area furthermore. The main novel feature that enabled state-of-the-art results was the utilization of the inverter's high-speed, low-power characteristics. The downsides of the inverter-based comparator were overcome by the second regulation loop for the inverter supply voltage. Precision analog techniques were used to accomplish some additional features, such as intermediate output voltages and smaller switching losses. The proposed DC-DC converter's efficiency, speed, and power density make it a useful solution for always-on circuits in IoT devices.

Additional scientific contributions were demonstrated in Chapters 3, 4, and 5. The boost DC-DC converter as part of the image-sensing platform [4] was described in Chapter 3. The main purpose of the DC-DC converter in this application was to serve as a crucial part of the energy harvesting process, thus improving the energy efficiency of the entire system. The energy was harvested from the charge gathered from the photodiodes. Since the photodiodes start leaking current near the threshold voltage level (~500 mV), the voltage node that collects charge needs to be kept under that level (~450 mV). An implemented DC-DC converter is used to boost the diode voltage to the level suitable for battery recharge (~1.5 V) with a peak efficiency of 60%. Note that the same photodiodes that are used for harvesting are also used for sensing, and event detection is conducted during the harvesting. This new feature enables longer energy harvesting cycles, which could facilitate better self-powered imagers in Edge devices.

A low-power clock generator with implemented temperature and duty cycle compensation is described in Chapter 4. The circuit application was demonstrated in the image-sensing platform [4], also mentioned in Chapter 3. An additional improvement in the system's power efficiency was achieved by using the low-power clock generator designed specifically for this purpose. A current-controlled ring oscillator is used to produce the initial signal, which is then level-shifted, and the duty cycle is fixed. The main obstacle in this approach was the large temperature dependence of the current-controlled ring oscillator. This issue was overcome by the introduction of novelty in the form of an opposite temperature-dependent source of the bias current, which compensated for the temperature dependence of the current-controlled ring oscillator. The clock exhibited state-of-the-art performances regarding area and energy efficiency.

Chapter 5 describes a digitally controlled fractional-order capacitor operating in the frequency range relevant to the switching-capacitor DC-DC converter. The designed FO capacitor can achieve three different phase shifts: -30°, -45°, and -60°. In that way, the FO capacitor acts as a fraction of the standard capacitor (1/3, 1/2, and 2/3). If used as a C_{fly} inside the DC-DC converter, fractional elements provide additional freedom in terms of VCR, thus enabling better performances of the entire power management system.

The integrated circuits described in this thesis improved the area of fully integrated power management in several aspects, which makes them inspiring solutions for the low-power applications of IoT devices.

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Biography

Edi Emanović was born in Nova Gradiška, where he completed primary and secondary education. He graduated from the Faculty of Electrical Engineering and Computing in 2016 on the subject of active, fully integrated, electrical filters in CMOS technology. In the same year, he began his doctoral studies at the Faculty of Electrical Engineering and Computing and went to Bar-Ilan University in Israel for professional training. At the Bar-Ilan, he begins his research on fully integrated DC-DC converters in collaboration with the ENICS laboratory team. The application of DC-DC converters in state-of-the-art power management systems has become his main preoccupation and the topic of his doctoral thesis. In addition to academic involvement at the University of Zagreb and Bar-Ilan University in Israel, he also participates in numerous industrial projects in cooperation with various companies, the most prominent of which are KONČAR-Institute for Electrical Engineering and Xylon.

Publications:

(1) E. Emanović, J. Shor and D. Jurišić, "An Inverter-Based, Ultra-Low Power, Fully Integrated, Switched-Capacitor DC-DC Buck Converter," *ESSCIRC 2021 - IEEE 47th European Solid-State Circuits Conference (ESSCIRC)*, Grenoble, France, 2021, pp. 359-362.

(2) E. Emanović, D. Jurišić and J. Shor, "A Fully Integrated, Switched-Capacitor DC-DC Buck Converter featuring an Inverter-Based Comparator," in *IEEE Access.*

(3) E. Emanovic et al., "Digitally Controlled Fractional-Order Elements Using OTA-C Structures," *MDPI Electronics*. 2024; 13(11): 2066.

(4) D. Zagouri *et al*., "A Photovoltaic Energy Harvester/Image Sensor Platform With Event Detection Capability in 180 nm," in *IEEE Solid-State Circuits Letters*, vol. 7, pp. 62-65, 2024.

(5) E. Emanovic, D. Jurisic and G. S. Moschytz, "Low Sensitivity Coupled CMOS CCII Biquads," *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019, pp. 365-368.

(6) E. Emanovic, D. Jurisic and G. S. Moschytz, "Influence of CMOS CCII Parasitics in Realization of Two-Integrator Band-Pass Filter," *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 89-92.

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(9) E. Emanović and D. Jurišić, "Dynamic range optimization and noise reduction by low-sensitivity, fourth-order, band-pass filters using coupled general-purpose Biquads," *2017 40th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, Opatija, Croatia, 2017, pp. 141-145.

Životopis

Edi Emanović rođen je u Novoj Gradiški, gdje je završio osnovnu i srednju školu. Diplomirao je na Fakultetu elektrotehnike i računarstva 2016. godine na temu aktivnih, potpuno integriranih, električnih filtara u CMOS tehnologiji. Iste godine započinje doktorski studij na Fakultetu elektrotehnike i računarstva te odlazi na stručno usavršavanje na Sveučilište Bar-Ilan u Izraelu. Na Bar-Ilanu započinje svoje istraživanje o potpuno integriranim DC-DC pretvaračima u suradnji s timom laboratorija ENICS. Primjena DC-DC pretvarača u najsuvremenijim sustavima upravljanja napajanjem postala je njegova glavna preokupacija i tema njegovog doktorskog rada. Uz akademski angažman na Sveučilištu u Zagrebu i Sveučilištu Bar-Ilan u Izraelu, sudjeluje i u brojnim industrijskim projektima u suradnji s raznim tvrtkama od kojih su najistaknutije KONČAR-Institut za elektrotehniku i Xylon.