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Sveučilište u Zagrebu

FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA

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ARHITEKTURE RELAKSACIJSKOGA OSCILATORA S KOMPENZACIJOM KAŠNJENJA I NAPONA POMAKA

DOKTORSKI RAD

Mentor: prof. dr. sc. Adrijan Barić

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About the Supervisor

Adrijan Barić was born in Zagreb in 1958. He received the Dipl. Ing. degree in 1982 and the M.Sc. degree in 1985 from the University of Zagreb (UniZag), Faculty of Electrical Engineering and Computing (FER), Croatia. He received the PhD degree in 1995 from the Dublin City University, Ireland. He has been employed by FER since 1984. He was a visiting researcher at the Rutherford Appleton Laboratory, England, and at the Ghent University, Belgium. He was promoted to Full professor in 2013. He was a principal investigator of two projects funded by the Ministry of Science, Education and Sports of Croatia, one BICRO project, and he coordinated the FER research team in one EU FP6 project, one EU FP7 project, and several bilateral and multilateral projects with European companies and universities. He presently coordinates the project "Sensor Fusion" funded by ams–OSRAM AG, Austria, and the project "Fast switching converters based on GaN devices and resonant architectures" funded by the Croatian Science Foundation. He published over 100 papers in scientific journals and scientific conference proceedings in the area of integrated circuits and electromagnetic compatibility. He was the President of the Committee for Research, Development and Technology of the UniZag from 2008 to 2011 and the President of the Council of Technical Faculties of the UniZag from 2013 to 2017. He was a General Chair or Co–Chair of two IEEE conferences, the Finance Chair of one IEEE conference, and the Technical Programme Chair of the IEEE conference EMC Compo 2011. He is a member of IEEE, HD MIPRO, KoREMA, and AMAC–FER societies. In 2015, he received the Gold Plaque "Josip Lončar" from FER.

O mentoru

Adrijan Barić rođen je u Zagrebu 1958. Diplomirao je 1982. i magistrirao 1985. na Fakultetu elektrotehnike i računarstva (FER) Sveučilišta u Zagrebu (SuZ). Doktorirao je 1995. na Dublin City University, Irska. Na FER–u radi od 1984. Bio je gostujući istraživač na Rutherford Appleton Laboratory, Engleska te na Ghent University, Belgija. Za redovitog profesora u trajnom zvanju izabran je 2013. Bio je glavni istraživač na dva projekta MZOS–a, jednom BICRO projektu te je vodio FER–ov tim u jednom EU FP6, jednom EU FP7 projektu te više bilateralnih i multilateralnih projekata s europskim tvrtkama i sveučilištima. Trenutno vodi projekt HRZZ–a „Brzi prekidački pretvornici zasnovani na GaN elementima i rezonantnim arhitekturama" te projekt „Sensor Fusion" s tvrtkom ams–OSRAM AG, Austrija. Objavio je više od 100 radova u znanstvenim časopisima i zbornicima znanstvenih konferencija iz područja integriranih sklopova i elektromagnetske kompatibilnosti. Bio je predsjednik Odbora za istraživanje, razvoj i tehnologiju SuZ–a od 2008. do 2011. te predsjednik Vijeća tehničkog područja SuZ-a od 2013. do 2017. Bio je predsjedatelj ili supredsjedatelj dviju IEEE konferencija, financijski voditelj jedne IEEE konferencije te voditelj programa IEEE konferencije EMC Compo 2011. Član je udruga IEEE, HD MIPRO, KoREMA i AMAC–FER. Godine 2015. primio je FER-ovu Zlatnu plaketu „Josip Lončar".

A designer knows he has achieved perfection not when there is nothing left to add, but when there is nothing left to take away.

Antoine de Saint–Exupéry

Preface

This PhD thesis was done within the *High Precision Oscillator* project funded and supported by ams OSRAM in cooperation with the ZEMRIS department at the Faculty of Electrical Engineering and Computing (FER), University of Zagreb. Over the last seven years (2016–2022), the research driven primarily by industry requirements has delivered a number of considerable improvements and contributions in almost all relevant aspects: from modeling and design to manufacturing and test development. The most important scientific contributions were published in several journals, conferences, and patents and eventually compiled within this thesis.

And what a journey it was. Unquestionably, it began long before the PhD project itself, as it was not only the time spent in front of the screen or in the lab that counted, but also the knowledge, belief, and determination at the onset of such an endeavor. Therefore, I must feel grateful to my family, especially my parents and sisters, who had seemingly done something to raise my stubborn side to the full potential that just refuses to give up. I'm also beyond grateful to my wife Antonija – you believed in me even when I didn't. To my dear professor Adrijan, who's been there for my entire academic and professional career – I can't thank you enough. Deepest gratitude to my supervisors who conceived this project and made everything possible: Josi, thank you for the relentless support, and Gregor, thank you for teaching me how to be an engineer. Special thanks must go to my ams OSRAM colleagues, especially the BASE IP office, the CGB group, and the coffee machine – it was, and still is, a pleasure being there. Two Ivans from Austria – thanks for the jokes, and everything else. All the colleagues from the third floor of the FER D–building, the place that always feels like home – thank you. I will also never forget the experience from the student exchange at KU Leuven – it was the year that placed the foundations of my scientific and engineering career. To my irreplaceable friends and colleagues, Marko, Vlatko, Tomo, and Tomislav – thanks for being the inspiration and always having my back. Big thanks to my online gaming party – good game, well played. Also, thank you Ivan for the standard coffee break at nine o'clock. In the end, my deepest gratitude goes to all the others that helped either personally or professionally during this incredible voyage.

Josip Mikulić

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Abstract

This thesis presents the detailed theoretical analysis, measurements, and performance comparison of several novel relaxation oscillator architectures, having the main focus on the compensation of the propagation delay and offset voltage of the comparator stage. The first architecture introduces two replica comparators that imitate the behavior of the sensing comparators and compensate for their influence on the timing. Next, a further enhancement of the relaxation oscillator core architecture is proposed, comprising a self–compensating chopped comparator pair that entirely cancels the propagation delay and offset voltage of the comparators while being more efficient in power consumption and area. The third architecture introduces additional integrating unit that is used for measurement and compensation of the propagation delay, being compatible with low supply environments and advanced technology nodes. Furthermore, the fourth relaxation oscillator core architecture comprises replica chopped comparator, providing an efficient delay and offset cancellation with minimal influence on power, area, and signal integrity. Eventually, a cost–efficient methodology for a post–manufacturing temperature calibration that significantly reduces the temperature drift of the output frequency is proposed and demonstrated on a manufactured self–sustaining oscillator prototype.

Key words: relaxation oscillator, offset voltage, delay cancellation, temperature calibration, process calibration, on–chip design

Prošireni sažetak

Arhitekture relaksacijskoga oscilatora s kompenzacijom kašnjenja i napona pomaka

Ubrzani rast industrije mobilnih i nosivih uređaja nameće standard minijaturizacije električnog sklopovlja, što u većini slučajeva podrazumijeva potpunu integraciju sustava na silicijske pločice. Dodatni zahtjevi odnose se na što duže trajanje baterijskog napajanja i nisku cijenu proizvodnje. Posljedično, kristalni oscilatori visoke preciznosti rijetko su prihvatljivi u takvim sustavima zbog potrebe za vanjskom komponentom relativno velikih dimenzija. Slično vrijedi i za oscilatore s LC i MEMS rezonatorima koji su kompatibilni s integracijom na silicij, ali nerijetko ih karakterizira visoka potrošnja energije i skupa ugradnja. Nasuprot tome, relaksacijski oscilatori prikladna su rješenja za potpuno integrirane sustave zbog njihove karakteristične male potrošnje, malih dimenzija i jednostavnosti implementacije. Također, pokrivaju jako širok raspon snaga (nW do mW) i frekvencija (Hz do MHz), imaju kratko vrijeme stabilizacije te su primjenjivi pri ekstremnim uvjetima napajanja (< 1 V) i temperatura (< -40 °C i > 150 °C). Međutim, njihova preciznost uvjetovana je brojnim tehnološkim ograničenjima, od kojih su najznačajniji kašnjenje i napon pomaka komparatora te temperaturna varijacija referentnih elemenata (otpornika i kondenzatora). Poboljšanje preciznosti relaksacijskih oscilatora eliminacijom utjecaja komparatora može se provesti na različite načine što je predočeno rezultatima brojnih znanstvenih istraživanja koja uključuju: korištenje preklopnih komparatora, repliciranje dijelova sklopa, integraciju pogreške frekvencije s povratnom vezom te korištenje digitalnih kompenzacijskih petlji, dok se dodatno poboljšanje nakon izrade čipova postiže temperaturnom kalibracijom sustava i implementacijom naponskog regulatora. U krajnjem slučaju, frekvencija RC relaksacijskih oscilatora određena je vremenskom konstantom referentnog otpornika i kondenzatora čija se temperaturna ovisnost može dodatno ograničiti ugradnjom preciznih elemenata uz povećanu cijenu proizvodnje.

Utjecaj kašnjenja i napona pomaka komparatora predočen je na konvencionalnoj topologiji relaksacijskoga oscilatora, gdje simulacije provedene na prototipu jezgre oscilatora izvedene u 350 nanometarskoj tehnologiji predviđaju relativni pomak frekvencije takta od nekoliko postotaka. Iako je moguće reducirati utjecaj komparatora povećanjem iznosa struje i dimenzija tranzistora, nije ga moguće potpuno otkloniti zbog čega se nameće potreba sklopovske kompenzacije. Prva predložena arhitektura jezgre relaksacijskog oscilatora s replicirajućim komparatorima (eng. *relaxation oscillator core with replica comparators*) kompenzaciju kašnjenja i napona pomaka zasniva na dva dodatna replicirajuća komparatora koja procjenjuju utjecaj očitavajućih komparatora na period izlaznog signala. Mjerenje utjecaja komparatora izvedeno je kombinacijom suprotnog nagiba integracijskog signala i protufaze dvaju ulaza replicirajućih

komparatora, pri čemu se točnost mjerenog signala zasniva na usklađenosti kašnjenja i napona pomaka očitavajućih i replicirajućih komparatora. Nadalje, izmjereni utjecaj se kompenzira povratnom vezom, odnosno privremenim ubrzavanjem integracije referentnog signala u integratoru aktiviranjem dodatnog strujnog izvora.

Prototip arhitekture jezgre relaksacijskog oscilatora s replicirajućim komparatorima izrađen je u 350 nanometarskoj tehnologiji s nominalnom frekvencijom takta od 1 MHz. Prilikom mjerenja, referentni napon i referentna struja dovedeni su izvana. Izmjerena je temperaturna ovisnost na osam uzoraka prototipa jezgre $\pm 0,30$ % u rasponu temperature od -40 °C do 125 °C, što ukazuje na značajno poboljšanje preciznosti frekvencije od oko četiri puta u odnosu na konvencionalnu jezgru, dok je izmjerena ovisnost o naponu napajanja poboljšana oko tri puta te iznosi $\pm 0,19$ % pri napajanju od $3,0$ V do $4,5$ V. Dodatno, simulacije osjetljivosti na kašnjenje i sustavni napon pomaka ukazuju na poboljšanje od preko 100 puta, međutim, osjetljivost na napon pomaka uslijed slučajnih efekata nije značajno promijenjena. Predložena arhitektura ima i mnogo bolju linearnost frekvencije prilikom modulacije ulazne referentne struje ($HD_2 = -61,1$ dB i $HD_3 = -84,7$ dB, pri $\Delta f_{osc} = 500$ kHz) te slične parametre šuma ($\mathscr{L}(f) = -93$ dBc/Hz pri $f_m = 10$ kHz, $\sigma_{Tosc} = 230$ ppm te $\sigma_y = 13$ ppm) u odnosu na konvencionalnu arhitekturu. S druge strane, površina na siliciju ($0,04$ mm^2) i potrošnja (210 µW uz $V_{DD} = 3,3$ V) unaprijeđene jezgre nešto su veće zbog prisustva dvaju dodatnih komparatora unutar sklopa.

Druga unaprijeđena arhitektura jezgre oscilatora sa samokompenzirajućim preklopnim parom komparatora (eng. *relaxation oscillator core with self–compensating chopped comparator*) donosi daljnja poboljšanja u odnosu na prvu predloženu arhitekturu jezgre s replicirajućim komparatorima. U ovoj arhitekturi, par komparatora implementiran je unutar preklopnog sklopa od kojih je jedan očitavajući komparator, a drugi replicirajući komparator pomoću kojeg se mjeri utjecaj očitavajućeg komparatora na stabilnost frekvencije. Slično kao i u prvoj arhitekturi, mjerenje utjecaja izvedeno je kombinacijom suprotnog nagiba integracijskog signala i protufaze dvaju ulaza replicirajućeg komparatora u odnosu na očitavajući komparator. Dakle, metoda preklapanja komparatora u svakoj poluperiodi izmjenjuje replicirajući i očitavajući komparator, čime se u potpunosti eliminira utjecaj komparatora na frekvenciju signala, uključujući napon pomaka i kašnjenje.

Prototip jezgre relaksacijskog oscilatora sa samokompenzirajućim preklopnim parom komparatora izrađen je u 350 nanometarskoj tehnologiji s nominalnom frekvencijom takta od 1 MHz. Prilikom mjerenja, referentni napon i referentna struja dovedeni su izvana. Mjerenja izvedena na osam testnih uzoraka oscilatora ukazuju na značajno poboljšanje stabilnosti frekvencije

takta, postižući oko pet puta veću preciznost prilikom promjene napona napajanja i temperature u odnosu na konvencionalnu jezgru, pri čemu je varijacija frekvencije jednaka $\pm 0,24$ % za temperaturni raspon od -40 °C do 125 °C, dok pomak frekvencije u odnosu na promjene napona napajanja iznosi $\pm 0,12$ % za napone od $3,0$ V do $4,5$ V. Simulirana osjetljivost na kašnjenje i napon pomaka poboljšani su više od 100 puta, uključujući i slučajne efekte, što ukazuje na to da, za razliku od jezgre s replicirajućim komparatorima, preciznost oscilatora ne ovisi o usklađenosti dvaju komparatora. Linearnost pri modulaciji frekvencije također je dodatno poboljšana, gdje parametri distorzije iznose $HD_2 = -61,7$ dB i $HD_3 = -93,2$ dB uz $\Delta f_{osc} = 500$ kHz, dok su parametri šuma ($\mathscr{L}(f) = -92$ dBc/Hz pri $f_m = 10$ kHz, $\sigma_{Tosc} = 235$ ppm te $\sigma_y = 15$ ppm) slični kao i kod konvencionalnog oscilatora. Za razliku od prve jezgre, predložena je arhitektura neosjetljiva na neslaganje komparatora te ne zahtijeva znatno veću površinu ($0,032$ mm^2) i potrošnju (160 µW uz $V_{DD} = 3,3$ V) u odnosu na konvencionalnu jezgru.

Treća predložena arhitektura jezgre relaksacijskog oscilatora s replicirajućim integratorom (eng. *relaxation oscillator core with replica integrator*) prilagođena je manjim naponima napajanja ($< 1,2$ V) i naprednijim tehnološkim procesima (< 100 nm) gdje je izraženiji utjecaj komparatora. Za razliku od prve dvije jezgre oscilatora, strujni izvori unutar integratora u predloženoj arhitekturi imaju identičan smjer što omogućuje neometano funkcioniranje sklopovlja pri niskim naponima napajanja, posebice uz nisku razinu signala referentnog napona. Jezgra predloženog relaksacijskog oscilatora sastoji se od dvaju referentnih integratora čiji se signali uspoređuju s referentnim naponom i polovicom referentnog napona te trećim, replicirajućim integratorom, čiji se signal uspoređuje s polovicom referentnog napona. Nadalje, tri komparatora integracijskih signala jezgre implementirani su s preklapajućim sklopovima. Replicirajući integrator mjeri kašnjenje očitavanja komparatora, što se zasniva na usklađenosti brzine integracije dvaju referentnih integratora i replicirajućeg integratora te međusobnoj usklađenosti kašnjenja triju komparatora. Povratnom se vezom ubrzava integracija referentnog signala aktivirajući dodatni strujni izvor unutar integratora, čime se kompenzira utjecaj kašnjenja komparatora na stabilnost frekvencije. S druge strane, preklopno sklopovlje komparatora osigurava kompenzaciju napona pomaka.

Prototip jezgre relaksacijskog oscilatora s replicirajućim integratorom dizajniran je u 110 nanometarskoj tehnologiji s nominalnom frekvencijom takta od 2 MHz. Simulirana je preciznost prototipa jezgre s replicirajućim integratorom $\pm 0,50$ % uslijed promjena temperature u rasponu od -40 °C do 125 °C te $\pm 0,33$ % uslijed promjena napona napajanja u rasponu od $1,08$ V do $1,32$ V. Potiskivanje kašnjenja (> 20 puta) i napona pomaka komparatora ($>$ 10 puta) te linearnost frekvencije pri modulaciji ($HD_2 = -62,6$ dB i $HD_3 = -98,3$ dB pri

$\Delta f_{osc} = 500$ kHz) također su značajno unaprijeđeni u odnosu na konvencionalnu jezgru oscilatora, dok je šum ($\sigma_{Tosc} = 1100$ ppm) povećan u odnosu na prethodne jezgre zbog izrazito manjeg raspona integracijskog napona. Površina je jezgre oscilatora $0,045$ mm^2, a snaga pri naponu od $V_{DD} = 1,2$ V iznosi $39,6$ µW.

Zatim, predložen je dizajn relaksacijskog oscilatora u 180 nanometarskoj tehnologiji s mogućnošću namještanja nominalne vrijednosti i temperaturnog koeficijenta izlazne frekvencije. Prototip oscilatora sastoji se od referentnih blokova (generatora referentnog napona, naponsko–strujnog pretvarača i strujnog zrcala) te jezgre relaksacijskog oscilatora s replicirajućim preklopnim komparatorom (eng. *relaxation oscillator core with replica chopped comparator*). Generator referentnog napona sastoji se od generatora struje proporcionalne apsolutnoj temperaturi te generatora struje obrnuto proporcionalne apsolutnoj temperaturi, koje su nadalje kombinirane u jednu struju s niskom temperaturnom ovisnošću, čime se preko izlaznog otpora dobiva referentni napon. Naponsko–strujni pretvarač, čiji je ulaz izlazni napon generatora referentnog napona, definira odnos izlaznog referentnog napona i referentne struje pomoću referentnog otpornika. Uz to, unutar naponsko–strujnog pretvarača moguće je dodatno namještati iznos referentne struje pomoću strujnog DA pretvornika, čime je omogućeno posredno podešavanje nominalne vrijednosti frekvencije takta oscilatora. Također, promjenjivi temperaturni koeficijent referentnog otpornika unutar naponsko–strujnog pretvarača izveden je pomoću upravljivih segmenata dvaju otpornika s različitim temperaturnim koeficijentima prvog reda, čime je omogućeno posredno ugađanje temperaturnog koeficijenta frekvencije. Najzad, strujno zrcalo replicira referentnu struju u tri različite struje koje su, uz referentni napon, potrebne za rad jezgre. Posljedično, frekvencija jezgre definirana je referentnim otporom unutar strujno–naponskog pretvornika i referentnim kapacitetom unutar jezgre ($f_{osc} = {}^{1}\!/_{2R_{REF}C_{REF}}$). Oscilator pri radu ne zahtijeva ulazne referentne napone i struje, već samo napajanje i digitalne ulazne kodove za podešavanje nominalne frekvencije i temperaturne karakteristike.

Slično kao i u prethodnim arhitekturama, jezgra s replicirajućim preklopnim komparatorom kompenzira kašnjenje komparatora mjerenjem utjecaja očitavajućeg komparatora koje se zasniva na usklađenosti s replicirajućim komparatorom, dok se napon pomaka kompenzira pomoću preklopnog sklopa. Nominalna je frekvencija prototipa jezgre oscilatora 2 MHz, površina je jednaka $0,021$ mm^2, a snaga pri naponu od $V_{DD} = 1,8$ V iznosi $116,8$ µW. Simulirana je preciznost frekvencije $\pm 0,21$ % uslijed promjena temperature od -40 °C do 125 °C te $\pm 0,33$ % uslijed promjena napona napajanja od $1,62$ V do $1,98$ V. Potiskivanje kašnjenja i napona pomaka komparatora veće je od deset puta te su parametri distorzije značajno bolji u odnosu na konvencionalnu jezgru ($HD_2 = -65,9$ dB i $HD_3 = -95,9$ dB pri $\Delta f_{osc} = 500$ kHz), uz nešto veće podrhtavanje takta ($\sigma_{Tosc} = 320$ ppm).

Nadalje, prototip oscilatora s mogućnošu namještanja temperaturnog koeficijenta frekvencije izrađen je u 180 nanometarskoj tehnologiji. Nominalna je frekvencija oscilatora 2 MHz, površina iznosi $0,075$ mm^2, dok je ukupna potrošnja 185 µW pri naponu napajanja od $1,8$ V. Pomak je frekvencije takta ± 0.77 % uz temperaturne promjene od -40 °C do 125 °C te $\pm 0,04$ % uslijed promjena napona napajanja od $1,62$ V do $1,98$ V, mjereno na osam uzoraka bez temperaturne kalibracije. Ukupno vrijeme pokretanja oscilatora iznosi $5,5$ µs, a podrhtavanje takta $\sigma_{Tosc} = 476$ ppm.

U sustavima koji zahtijevaju veću preciznost frekvencije poželjno je implementirati regulator napona kako bi se gotovo u potpunosti eliminirala ovisnost frekvencije takta o napajanju te provesti temperaturnu kalibraciju oscilatora kako bi se dodatno smanjila varijacija s temperaturnim promjenama. Pri tome, nakon izrade potrebno je izvršiti mjerenja sustava na nekoliko različitih temperatura kako bi se odredila temperaturna karakteristika frekvencije. Međutim, dodatna temperaturna mjerenja uvode značajne sporedne troškove u fazi testiranja, što se posebice odnosi na mjerenja temperatura nižih od sobne temperature ($T < 27$ °C). Sukladno tomu, predložena je metoda kalibracije relaksacijskih oscilatora koja se zasniva na mjerenju frekvencije na samo dvije proizvoljne temperature, čime se ograničava porast pripadajućih troškova proizvodnje.

Pošto se temperaturna ovisnost frekvencije kod relaksacijskih oscilatora u pravilu može aproksimirati polinomom drugog reda, za ispravnu karakterizaciju potrebna su minimalno tri mjerenja na različitim temperaturama. Međutim, na primjeru prototipa oscilatora demonstrirano je kako su dovoljne samo dvije točke za približan izračun optimalne vrijednosti podešavanja temperaturnog koeficijenta zbog relativno stabilne vrijednosti koeficijenta drugog reda temperaturne karakteristike. Premda u idealnom slučaju mjerenje pri manjim temperaturnim razlikama ($\Delta T < 30$ °C) rezultira boljom aproksimacijom, uslijed šuma i ostalih ograničenja mjernog sustava, potrebno je povećati temperaturni raspon mjerenja. Predložena metoda kalibracije temperaturne karakteristike oscilatora s dva temperaturna mjerenja (na $T = 35$ °C i $T = 85$ °C), predočena je na osam testnih uzoraka oscilatora, čime je postignuta oko tri puta veća stabilnost frekvencije (± 0.26 %) uslijed promjena temperature.

Ključne riječi: relaksacijski oscilator, napon pomaka, kašnjenje, temperaturna kalibracija, kalibracija procesnih parametara, potpuno integrirani sklopovi

Contents

Chapter 1

Introduction

1.1 Overview

Over the recent decade, the ever–increasing industry of mobile and wearable devices has developed essential requirements for fully integrated circuits. The targeted electronic products cover a broad application space, including but not limited to wearable devices, internet of things (IoT), wireless sensor networks (WSN), biomedical sensors, implantable biomedical devices, environmental monitoring systems, microcomputers, high–speed interfaces, and radio frequency identification (RFID) [1–30]. In most cases, such systems are intended to provide long battery life and small form–factor while simultaneously having a low manufacturing cost [13, 26, 31]. This became a vital consideration for the clock generation in SoCs (Systems–on–Chip), where precise crystal–based oscillators are no longer feasible since they feature a bulky external crystal resonator component [9–12, 24–28]. Moreover, the use of silicon–based high–performance time references, specifically LC [32, 33] and MEMS [34–36] resonators, remains limited due to their high power consumption, increased cost, and complexity of implementation [1, 9].

Accordingly, relaxation oscillators [1–24, 37–46] have become a favorable option for full on–chip devices, achieving an excellent trade–off between the physical area, implementation cost, power consumption, start–up time, and accuracy [14, 47]. They also offer considerable design flexibility, covering an extensive range of operating frequencies, specifically from Hz [37] to tens of MHz [4, 5], and also being scalable to low power and voltage levels [14, 39]. Furthermore, relaxation oscillators have an inherent advantage over ring oscillators [48, 49] in terms of frequency accuracy and start–up time [14, 47], although having a disadvantage in terms of phase noise [18–20, 50]. On the other hand, their accuracy is usually limited to the range of several percentage points by various process–related non–idealities [2, 4, 10]. First, the temperature dependency of the RC reference elements, namely the resistor and capacitor, directly affects the temperature drift of the output frequency. While most CMOS processes feature relatively stable Metal–Insulator–Metal (MIM) capacitors [16, 38], the standard polysilicon and diffusion resistors have significant first–order and second–order temperature coefficients. Here, the systematic influence of the resistor's first–order temperature coefficient can be mitigated using a composite resistor with opposing temperature coefficients [2–4, 10–13, 51], while the second–order temperature coefficient compensation requires advanced trimming techniques, such as demonstrated in [23, 27]. Nevertheless, a temperature coefficient of a composite resistor consisting of two different resistor types is susceptible to process variations [26], especially in high–volume production, which may be resolved using a non–standard precision resistor [8], usually available at an increased cost of processing. Furthermore, significant deterioration of the oscillator accuracy is caused by the propagation delay and offset voltage of the comparator stage [11, 12]. Here, the temperature dependency of the propagation delay is particularly significant since the offset voltage can be compensated by employing a chopped comparator

[8, 9], and the eventual supply dependency of the comparator can be minimized using a voltage regulator [8]. On the contrary, the propagation delay of the comparator is strongly temperature dependent [3, 8], where it is required to supply a disproportionate amount of current to the comparator to effectively minimize its influence on the timing [2, 4, 5]. Additionally, in terms of post–manufacturing sources of frequency shift, relaxation RC oscillators may suffer from package stress [27] and aging over lifetime [1–3, 52].

Accordingly, substantial research over the recent years has resulted in several different approaches to overcome the fundamental limitations of the relaxation oscillators. First, implementing the integrated error feedback loop that actively adapts the reference voltage considerably reduces the influence of the comparators at the price of an increased start–up time [1–5], where the accuracy of the output frequency becomes limited primarily by the drift of the reference resistor. Similar is presented in [6, 7], where a digital compensation improves the accuracy of the oscillator. On the other hand, employing a chopper in the comparator stage, as presented in [8, 9], eliminates the comparator's offset voltage and reduces the close–in phase noise, but standalone does not influence the propagation delay, similar to the self–clocked offset cancellation scheme published in [10]. Another approach is presented in [11, 12], where portions of the oscillator circuit are replicated to measure and cancel the undesirable influence of the comparators at the cost of increased area and power consumption. Furthermore, relaxation oscillators with current–mode comparators, published in [13–15], are capable of low voltage operation within the sub–microwatt region with relatively good accuracy. Also, [17] presents a relaxation oscillator capable of high–temperature operation, while works published in [18–22] present techniques for noise reduction in relaxation oscillators. Alternatively, in [24–28], post–manufacturing temperature calibration of RC oscillators significantly improves the performance but imposes significant cost overhead, requiring measurements at temperatures lower than the room temperature, together with complex circuitry that substantially increases circuit area.

This thesis further extends the research of the advanced relaxation oscillator cores, presenting several novel architectures [53–57] that minimize the influence of the comparator stage on the oscillation frequency. The proposed architectures compensate for the propagation delay by measuring the effective delay using replica circuitry, which, combined with chopper architecture, also cancels the offset voltage of the comparator. In order to enable a further enhancement of the oscillator's performance, a cost–efficient temperature calibration method of a self–referenced relaxation oscillator is proposed, compatible with high–volume production. Ultimately, combining the delay and offset–compensated relaxation oscillator architecture with a sample–to–sample process and temperature calibration eliminates the predominant sources of the frequency drift, eventually leading to clock accuracy significantly below the 1% range.

1.2 Contribution of This Work

The scientific contributions of the research presented within this thesis are:

- •Architecture of the relaxation oscillator with replica comparators that compensates the delay and systematic offset voltage of the comparators,
- •Architecture of the relaxation oscillator with chopped comparator pair that compensates the delay and offset voltage of the comparators, including the mismatch effects,
- •Architecture of the delay and offset voltage compensated relaxation oscillator with ultra low voltage capability,
- •Methodology for the post–manufacturing trim of the output frequency and its first order temperature coefficient.

1.3 Outline of the Dissertation

Chapter 2 presents a detailed analysis of the conventional relaxation oscillator architecture, including the influence of the comparator's non–idealities (propagation delay and offset voltage). Furthermore, an improved relaxation oscillator core architecture with replica comparators is proposed within this chapter, including the simulation and measurement results of the core prototype.

Chapter 3 proposes a further improved relaxation oscillator architecture with self–compensating chopped comparator pair, including the simulation and measurement results of the core prototype.

Chapter 4 presents the improved relaxation oscillator core architecture with replica integrator, suitable for low voltage operation in advanced technology nodes, together with the simulations of the proposed core prototype.

Chapter 5 presents a self–sustaining relaxation oscillator with replica chopped comparator core. Furthermore, a cost–efficient post–manufacturing process and temperature calibration procedure is presented, requiring two–point measurement at arbitrary temperatures. Eventually, the simulation and measurement results of the test–case relaxation oscillator are presented, demonstrating the proposed post–manufacturing process and temperature compensation method.

Chapter 6 presents the overview and comparison of relevant published RC oscillator designs, also including the outcomes of the Dissertation.

Chapter 2

Relaxation Oscillator Core with Replica Comparators

2.1 Motivation

Clock references based on RC relaxation oscillators have considerable advantages for wearable and battery–operated electronic applications, such as low power consumption [13–16], fast start–up [11, 14], linear tuning gain [10, 18, 19], and low cost due to compact size and compatibility with monolithic implementation [26]. Nevertheless, conventional relaxation oscillators are featured with several inherent weaknesses that limit their overall accuracy, typically to a range of a few percentage points. First, comparators' delay and offset voltage substantially contribute to the output frequency drift with temperature, supply voltage, and process variations [10, 14, 40]. Likewise, the oscillation frequency necessarily depends on the temperature drift of the reference elements, primarily the reference resistor [8]. Other timing error sources include the propagation delay of the logic blocks [4], switching non–idealities [26], mismatch between the devices [6, 15], aging [2], and packaging stress [27].

Accordingly, this chapter presents a detailed analysis of a conventional relaxation oscillator core, having an emphasis on the propagation delay and offset voltage of the comparator stage. Moreover, an advanced core architecture is proposed within this chapter [53] that compensates for the comparator's non–idealities. The core introduces two additional replica comparators that estimate the timing error and enable the delay and offset cancellation within the core integrator. Eventually, the core prototype is manufactured in 0.35–µm CMOS technology, oscillating with sub–1% accuracy and achieving a considerable performance improvement compared to the conventional core.

2.2 Conventional Relaxation Oscillator Core

The schematic of the conventional relaxation oscillator core is shown in Fig. 2.1 [3, 5, 41]. The oscillator core consists of two identical integrator blocks, two comparators, and an SR latch. Each integrator block includes a reference current source I_{REF}, two counter–phase operated switches controlled by the output signals of the SR latch ($C1$ and $C2$), and the capacitor having the capacitance value C_{REF}. The reference current (I_{REF}) and reference voltage (V_{REF}) are presumed to be generated within the reference generator, not shown in the schematic.

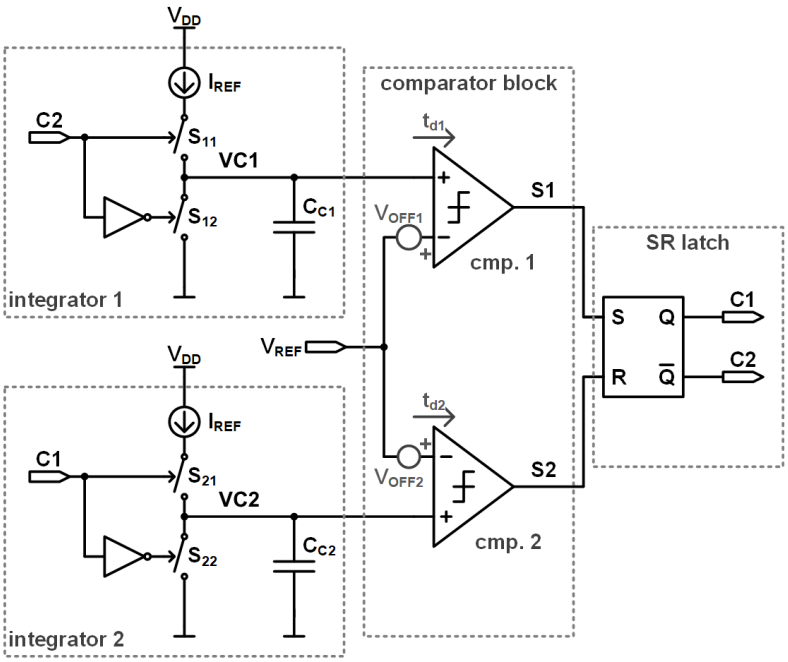


Figure 2.1: The schematic of the conventional relaxation oscillator core comprising two integrator blocks, two comparators, and an SR latch.

The operation of the conventional relaxation oscillator core in Fig. 2.1 is described with reference to the signal waveforms shown in Fig. 2.2. At an initial time ($t = t_0$) it is presumed that all the signals are set to the initial state by a start–up circuit (not shown in the schematic). Initially, the integration occurs within the second integrator in the time interval from t_0 to t_2. The integrating signal $VC2$ rises linearly, having the slope determined by the ratio of the charging current I_{REF} and the capacitor C_{C2}, specifically $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the first integrator block remains idle as the integration node $VC1$ is shorted to the ground reference node V_{SS} by the switch S_{12}. At a subsequent time, $t = t_1$, the integrating signal $VC2$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the second comparator $S2$ changes state to high at $t = t_2$ as a result of the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} (time required for charging the capacitances on the internal nodes of the comparator up to the digital threshold voltage V_{THR}) and the offset voltage V_{OFF2} (effectively superimposed on the reference voltage V_{REF}). Following the positive pulse of the

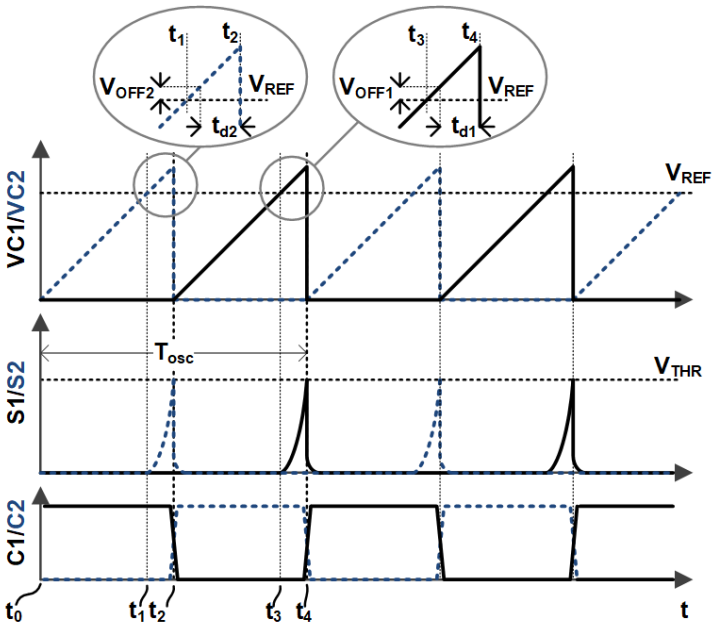


Figure 2.2: The signal waveforms of the conventional relaxation oscillator core.

second comparator output $S2$ and change of the control signals $C1$ and $C2$, after $t = t_2$, the integration starts within the first integrator. The integrating signal $VC1$ rises linearly, having the slope determined by the ratio of the charging current I_{REF} and the capacitor C_{C1}, specifically $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the second integrator block is idle as the integration node $VC2$ is shorted to the ground reference node V_{SS} by the switch S_{22}. At a subsequent time, $t = t_3$, the integrating signal $VC1$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the first comparator $S1$ changes state to high at $t = t_4$ as a result of the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}.

With this, a complete oscillation cycle is described from t_0 to t_4, where the expression for the oscillation period T_{osc} is determined by the reference voltage V_{REF}, comparator offset voltages, V_{OFF1} and V_{OFF2}, slope of the integrating signals, $\Delta VC/\Delta t = I_{REF}/C_{REF}$, and propagation delay of the comparators, t_{d1} and t_{d2} [10, 15]:

$$T_{osc} = \frac{2\big(V_{REF} + ½(V_{OFF1} + V_{OFF2})\big)C_{REF}}{I_{REF}} + t_{d1} + t_{d2}. \tag{2.1}$$

Consequently, together with the inherent drift of the references (V_{REF} and I_{REF}), the primary sources of the frequency instability are the propagation delay and offset voltage of the comparators [40], along with other minor effects neglected within the analysis (e.g., delay of the logic gates, switching non–idealities, parasitics, and mismatch between integrator blocks). Here, the comparator propagation delay is a parameter strongly dependent on the temperature and supply voltage [11, 13], and also compromises the frequency tuning linearity of the oscillator [18].

The offset voltage, on the other hand, in addition to the drift versus temperature and supply voltage, can also suffer from aging effects [1–3, 52] and deteriorate the clock accuracy over the lifetime. The straightforward reduction of the offset voltage can be achieved by increasing the device area, whereas reducing the propagation delay demands a large amount of additional power [2, 4], as will be discussed in the continuation of this chapter. Accordingly, a more convenient architecture must be considered to maintain a reasonable level of power and area while improving the frequency stability and tuning linearity.

2.3 Analysis of Comparator Non–Idealities

Following the expression for the oscillation period of the conventional relaxation oscillator core (2.1), the dominant influence on the frequency accuracy originates from the non–idealities of two sensing comparators [8], namely the propagation delay t_d and offset voltage V_{OFF}. Fig. 2.3 presents two common comparator architectures comprising a symmetrical operational transconductance amplifier – OTA (M_{N1-4} and M_{P1-4}), and the output inverter (M_{N5} and M_{P5}). Using the comparators with a symmetrical load of input transistors, such as the symmetrical OTA, is preferred over simpler comparator topologies since it ensures a smaller systematic offset voltage. The pMOS input pair variant (Fig. 2.3b) is assumed for the simulation of the propagation delay and offset voltage; nevertheless, all derived conclusions are also applicable to the variant with the nMOS input pair. The design parameters for the benchmark comparator designed in 0.35–µm technology are shown in Table 2.1.

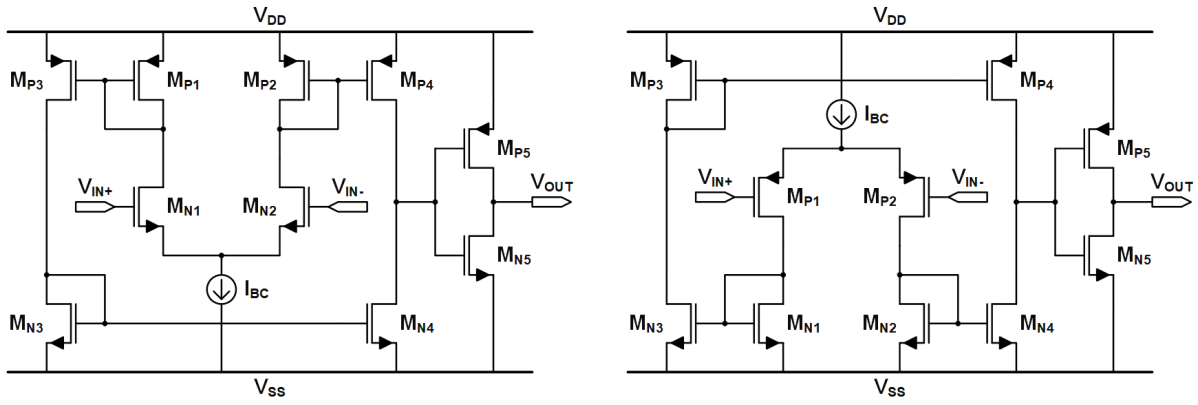


Figure 2.3: The schematic of the comparator (a) with nMOS input pair (b) with pMOS input pair. The comparators comprise a symmetrical OTA and an inverter stage.

Table 2.1: The design parameters of the benchmark comparator with pMOS input pair.

Transistor	W [µm]	L [µm]	Device
M_{N1-4}[1:4]	0.75	3	nmos3v
M_{P1-2}[1:4]	1.5	3	pmos3v
M_{P3-4}[1:4]	1.5	3	pmos3v
M_{N5}	1	0.35	nmos3v
M_{P5}	1.6	0.35	pmos3v

W and L are single finger dimensions.

2.3.1 Offset Voltage

The offset voltage of a comparator is usually divided into the systematic offset voltage V_{OFFsys} and random offset voltage V_{OFFrnd}, specifically

$$V_{OFF} = V_{OFFsys} + V_{OFFrnd}. \tag{2.2}$$

The systematic offset voltage depends exclusively on the variation of the PVT (process, voltage, temperature) parameters rather than the device mismatch [59]. Therefore, all identically designed comparators subjected to the same process and environment conditions would have an equal systematic offset voltage. For the comparator with the nMOS input pair (Fig. 2.3a), the expression for the systematic offset voltage V_{OFFsys}, derived in Appendix A.1.1, is

$$V_{OFFsys} = \frac{V_{GS,N3} - ½V_{DD}}{g_{m,dp}(r_{ds,N4}||r_{ds,P4})}. \tag{2.3}$$

Here, $V_{GS,N3}$ is the gate–source voltage of the nMOS mirror transistor M_{N3}, $g_{m,dp}$ is the transconductance of the differential pair transistors (M_{N1-2}), while $r_{ds,N4}$ and $r_{ds,P4}$ are the dynamic resistances of the output transistors M_{N4} and M_{P4}, respectively. Similarly, for the comparator with the pMOS input pair (Fig. 2.3b), the expression for the systematic offset voltage V_{OFFsys} is

$$V_{OFFsys} = \frac{V_{GS,P3} + ½V_{DD}}{g_{m,dp}(r_{ds,N4}||r_{ds,P4})}. \tag{2.4}$$

Here, $V_{GS,P3}$ is the gate–source voltage of the transistor M_{P3}, $g_{m,dp}$ is the transconductance of the differential pair transistors (M_{P1-2}), while $r_{ds,N4}$ and $r_{ds,P4}$ are the dynamic resistances of the output transistors M_{N4} and M_{P4}, respectively. According to (2.3) and (2.4), the root cause of the systematic offset voltage is the imbalance in the bias voltages of the internal nodes in combination with the channel length modulation effect of the output transistors. Note that the denominators in (2.3) and (2.4) are equal to the gain of the OTA stage, indicating that a higher gain reduces the systematic offset voltage.

On the other hand, the random offset voltage of a comparator is primarily related to the device mismatch [58, 60]. As derived in Appendix A.1.2, the variance of the overall random offset voltage V_{OFFrnd} can be calculated as follows:

$$\sigma^2(V_{OFFrnd}) = \frac{\sum \sigma^2(\Delta I_D)}{g_{m,dp}^2}, \tag{2.5}$$

where the sum of the particular contributions $\sigma^2(\Delta I_D)$ of the OTA transistors to the overall output current imbalance is evaluated and divided with the transconductance of the differential pair $g_{m,dp}$. Specifically, the particular contribution $\sigma^2(\Delta I_D)$ for each transistor in strong inversion

region can be expressed as

$$\sigma^2(\Delta I_D) = I_D^2 \frac{A_{KT}^2}{WL} + g_m^2 \frac{A_{Vth}^2}{WL} \tag{2.6}$$

and for the transistor in weak inversion as

$$\sigma^2(\Delta I_D) = g_m^2 \frac{A_{Vth}^2}{WL}. \tag{2.7}$$

Here, A_{KT} and A_{Vth} are the mismatch proportionality parameters for the current factor and threshold voltage, having a constant value at a given process, W and L are the width and length of a transistor, and g_m is the transconductance. Equations (2.5)–(2.7) indicate that larger device area (WL) leads to smaller random offset voltage values. Similarly, a higher transconductance of a differential pair at a given current also reduces the offset voltage, specifically achievable in weak inversion.

Finally, the systematic and random offset voltage of the benchmark comparator from Fig. 2.3b are simulated assuming the test bench from Fig. 2.4 and the design parameters from Table 2.1. The simulations are performed on 250 Monte Carlo points under the nominal conditions ($T = 35°C$ and $V_{DD} = 3.3$ V). Here, the Monte Carlo simulations include only pro-

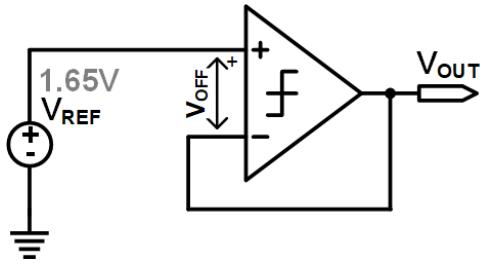
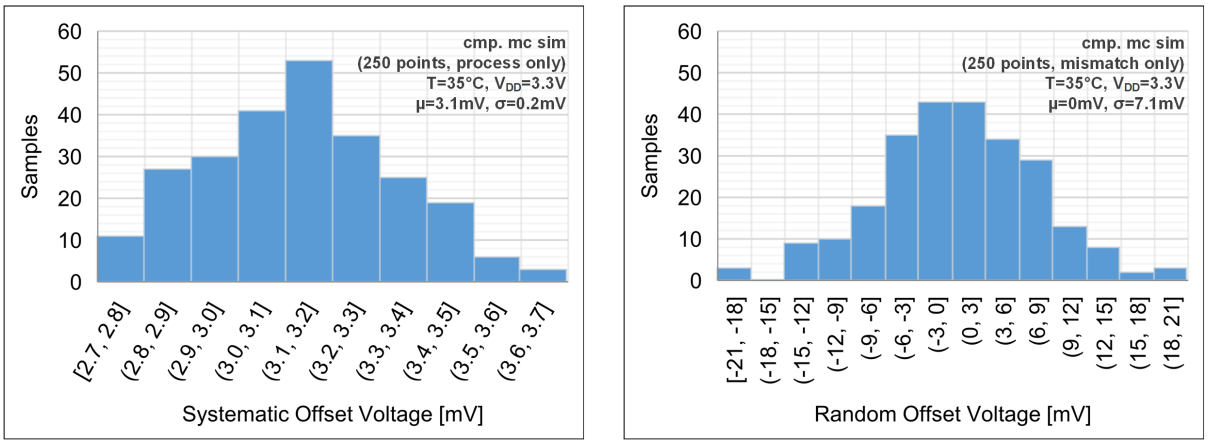


Figure 2.4: The test bench for the simulation of the offset voltage of the comparator.



(a) (b)

Figure 2.5: The simulated offset voltage of the comparator (a) systematic offset voltage (V_{OFFsys}) (b) random offset voltage (V_{OFFrnd}). The simulations are performed on 250 Monte Carlo points and the nominal environment conditions ($T = 35°C$, $V_{DD} = 3.3$ V).

cess variation (device mismatch excluded) for the systematic offset voltage simulation and mismatch (process variations excluded) for the random offset voltage simulation. The simulation results are shown in Fig. 2.5. For the systematic offset voltage, the mean value is $\mu(V_{OFFsys}) = 3.1$ mV with $\sigma(V_{OFFsys}) = 0.2$ mV, while for the random offset voltage, the mean value is $\mu(V_{OFFrnd}) = 0$ mV (since the systematic offset is subtracted from the results) and $\sigma(V_{OFFrnd}) = 7.1$ mV. Also, the systematic and random offset voltage of a comparator may have a dependency on temperature and supply voltage that needs to be considered during the design phase.

2.3.2 Propagation Delay

The expression for the propagation delay (t_d) of the comparators from Fig. 2.3, assuming the setup from Fig. 2.6, can be approximated with

$$t_d = \sqrt{\frac{V_{DD}C_{out}}{\Delta VC/\Delta t \cdot \sqrt{2K_T I_{BC}}}} \tag{2.8}$$

for the input pair in strong inversion (derived in Appendix A.2.1) and

$$t_d = \sqrt{\frac{2nV_T V_{DD}C_{out}}{\Delta VC/\Delta t \cdot I_{BC}}} + \frac{\sqrt{2}}{3}\sqrt{\left(\frac{V_{DD}C_{out}}{4I_{BC}}\right)^3 \cdot \frac{\Delta VC/\Delta t}{nV_T}} \tag{2.9}$$

for the input pair in weak inversion (derived in Appendix A.2.2). Here, V_{DD} is the supply voltage, C_{out} is the effective capacitance of the output node of the OTA (input node of the inverter), I_{BC} is the comparator bias current, $\Delta VC/\Delta t$ is the slope of the integrating voltage ($\Delta VC/\Delta t = I_{REF}/C_{REF}$), K_T is the current factor ($K_T = ½\mu_c C_{ox} W/L$) of the input transistors, n is the subthreshold slope factor ($n \approx 1.4 \sim 1.5$) [61], and V_T is the thermal voltage ($V_T = kT/q$). It is also feasible to derive the expression for an input pair in a velocity saturation region, applicable for higher overdrive voltages of the input transistors [59]; nevertheless, since this region leads to very low power efficiency, it is rarely used and thus omitted from this analysis.

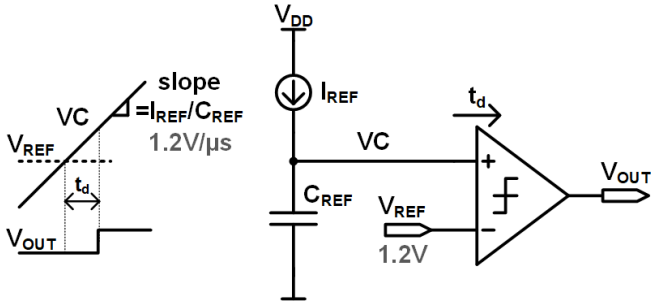
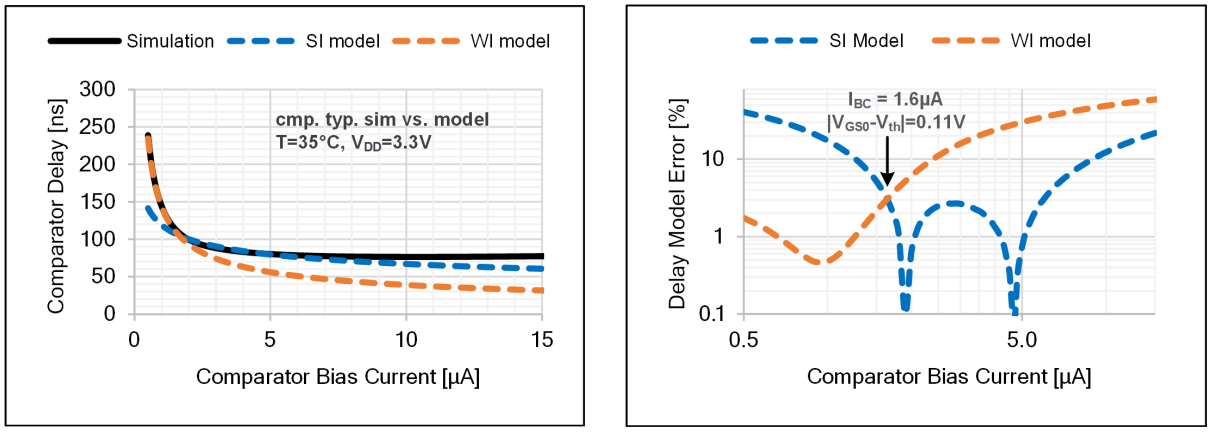


Figure 2.6: The test bench for the simulation of the comparator propagation delay.

When operating in the strong inversion (SI) region, as seen in (2.8), the delay is inversely proportional to the fourth root of the bias current I_{BC} ($t_d \propto I_{BC}^{-1/4}$), meaning that a disproportionate amount of power must be provided to reduce the propagation delay. On the other hand, the weak inversion (WI) operation is much more appropriate regarding the power efficiency. As seen in (2.9), the expression consists of two terms: the first is inversely proportional to the square root of the bias current I_{BC} ($\propto I_{BC}^{-1/2}$) and more prominent in a moderate inversion, whereas the second ($\propto I_{BC}^{-3/2}$) term becomes dominant for smaller currents. Also, (2.8) and (2.9) reveal the dependency of the propagation delay t_d on the temperature and the supply voltage: voltage dependency is reflected by the presence of the V_{DD} factor in both equations, while the dominant contributors to the temperature drift are K_T for the first equation (due to the temperature dependency of the carrier mobility [62]) and thermal voltage V_T for the second equation.

The two presented analytical models for the calculation of the comparator's propagation delay are compared with simulations using the test bench shown in Fig. 2.6, assuming the comparator with the pMOS input pair (Fig. 2.3b) and the design parameters from Table 2.1. The voltage ramp V_C is applied to the non–inverting input terminal, having the slope $\Delta VC/\Delta t = 1.2$ V/µs, while the inverting input terminal is connected to the reference voltage $V_{REF} = 1.2$ V. The fitted parameters K_T, C_{out}, and n used in the model are obtained with the optimization of the process model data and parasitic extraction values.

The comparator delay t_d is plotted versus the bias current I_{BC} in Fig. 2.7, simulated for the typical corner under the nominal environment conditions ($T = 35°$C, $V_{DD} = 3.3$ V). From the figure, it is evident that a good correspondence between the simulation and the analytical models from (2.8) and (2.9) is achieved, specifically for the weak inversion model in the bias current range up to $I_{BC} = 1.6$ µA (∼110 mV overdrive voltage), and for the strong inversion model in

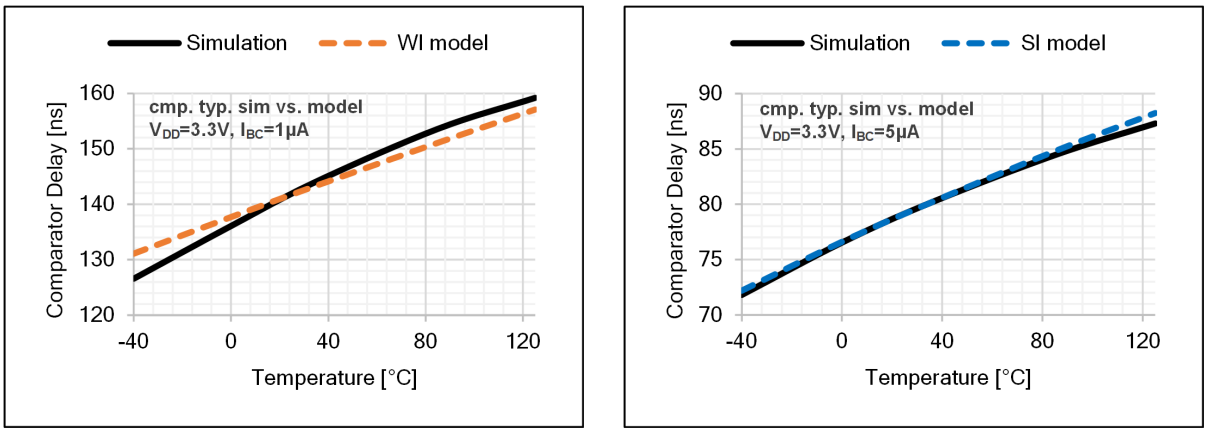


(a) (b)

Figure 2.7: (a) The comparison of the simulated comparator delay t_d with strong inversion (SI) model and weak inversion (WI) model, plotted vs. comparator bias current I_{BC}. (b) The error of the analytical model relative to the simulated propagation delay. The simulations are performed at the nominal environment conditions ($T = 35°$C, $V_{DD} = 3.3$ V) and typical process corner.

the bias current range 1.6 µA $< I_{BC} <$ 10 µA. Note that for larger comparator bias currents, specifically $I_{BC} >$ 10 µA (overdrive voltages larger than around 0.3 V), the strong inversion model eventually falls off as the input transistors enter the velocity saturation region. The best power versus delay tradeoff is achieved for the comparator bias currents around $I_{BC} = 2$ µA. Here, lower bias currents would result in a substantial delay increase, whereas increasing the power over the recommended levels would provide an insignificant reduction of the propagation delay, especially when going towards the velocity saturation region.

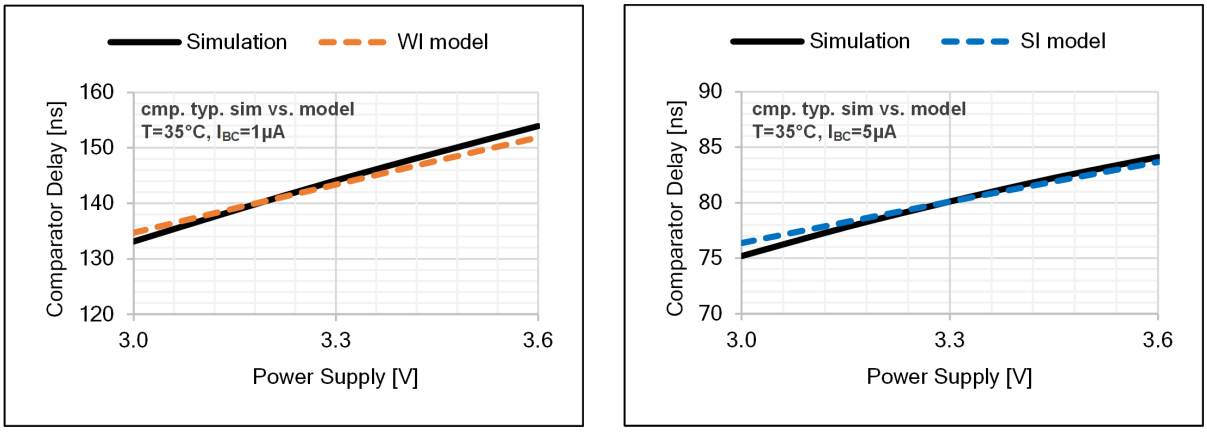
Next, the temperature dependency of the comparator's propagation delay t_d is simulated both for weak inversion and strong inversion using the bias current of $I_{BC} = 1$ µA and $I_{BC} =$ 5 µA, respectively. The temperature range is from -40°C to 125°C, and the supply voltage is $V_{DD} = 3.3$ V. The simulation results are shown in Fig. 2.8 and compared with the corresponding weak inversion (2.9) and strong inversion (2.8) model. Also, for the strong inversion model, it is assumed that the temperature dependency of the parameter K_T due to the carrier mobility (μ_c) temperature drift is $K_T \propto T^{-1.5}$ [9, 17]. As seen from the figures, the strong inversion model achieves a nearly perfect fit to the simulation data. On the other hand, the weak inversion model shows a slight discrepancy, originating from the fact that the subthreshold slope factor n is considered constant over the entire temperature range, while in fact, it has a slight positive first–order temperature coefficient [61].



(a) (b)

Figure 2.8: The comparison of the simulated comparator delay t_d with the analytical model (a) for weak inversion (WI) at $I_{BC} = 1$ µA (b) for strong inversion (SI) at $I_{BC} = 5$ µA; plotted vs. temperature. The simulations are performed at the typical process corner and nominal supply voltage ($V_{DD} = 3.3$ V).

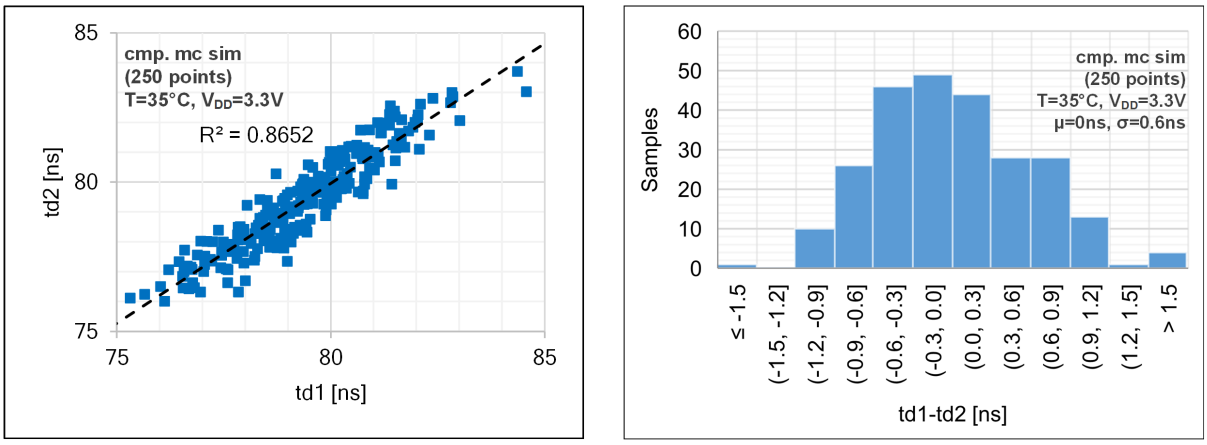
Similarly, the variation of the simulated propagation delay versus supply voltage is plotted in Fig. 2.9 and compared with the corresponding weak inversion (2.9) and strong inversion (2.8) model. The supply voltage range is from 3.0 V to 3.6 V, and the temperature is $T = 35$°C. As seen from the figures, a considerably good match between the models and the simulation is achieved in both cases.



(a) (b)

Figure 2.9: The comparison of the simulated comparator delay t_d with the analytical model (a) for weak inversion (WI) at $I_{BC} = 1$ µA (b) for strong inversion (SI) at $I_{BC} = 5$ µA; plotted vs. supply voltage. The simulations are performed at the typical process corner and nominal temperature ($T = 35°C$).

In the end, the simulation of the two comparators subjected to the same process variation and independent mismatch conditions is performed on 250 Monte Carlo points. The simulation results are presented in Fig. 2.10, where a substantial correlation between the propagation delays t_{d1} and t_{d2} of the two independent comparators is detected. This implies that the propagation delay of a comparator is primarily related to the process parameters rather than the mismatch. Therefore, it is expected for two identically designed comparators within the oscillator core to have an almost identical propagation delay, specifically $t_{d1} \approx t_{d2}$. This fact will be exploited in the continuation of this research, where replica comparators are implemented to cancel the propagation delay's influence on the oscillator timing.



(a) (b)

Figure 2.10: The simulated propagation delay of two independent comparators subjected to identical process variation (a) t_{d1} vs. t_{d2} scatter plot (b) histogram showing the propagation delay difference ($t_{d1} - t_{d2}$). The simulations are performed on 250 Monte Carlo points and the nominal environment conditions ($T = 35°C$, $V_{DD} = 3.3$ V).

2.4 Relaxation Oscillator Core with Replica Comparators

2.4.1 Core Architecture

The schematic of the relaxation oscillator core with replica comparators [53] is presented in Fig. 2.11. The oscillator core consists of two integrator blocks, a comparator block, and a logic block. Each integrator block includes three current sources (the first and third having the reference current I_{REF} and the second one having half the reference current $½I_{REF}$), four switches controlled by the output signals of the logic block, and the capacitor having the capacitance value C_{REF}. The comparator block consists of four identically designed comparators: two sensing comparators and two operating as replica comparators. The logic block processes the comparator outputs into the control signals, feeding them back to the integrator blocks, maintaining the oscillation in this way. Compared to the conventional relaxation oscillator topology from Fig. 2.1, the circuitry for the measurement and cancellation of the timing influence of the comparator stage is added, consisting of two counter–phase comparator replicas and two additional switched current sources inside the integrator blocks.

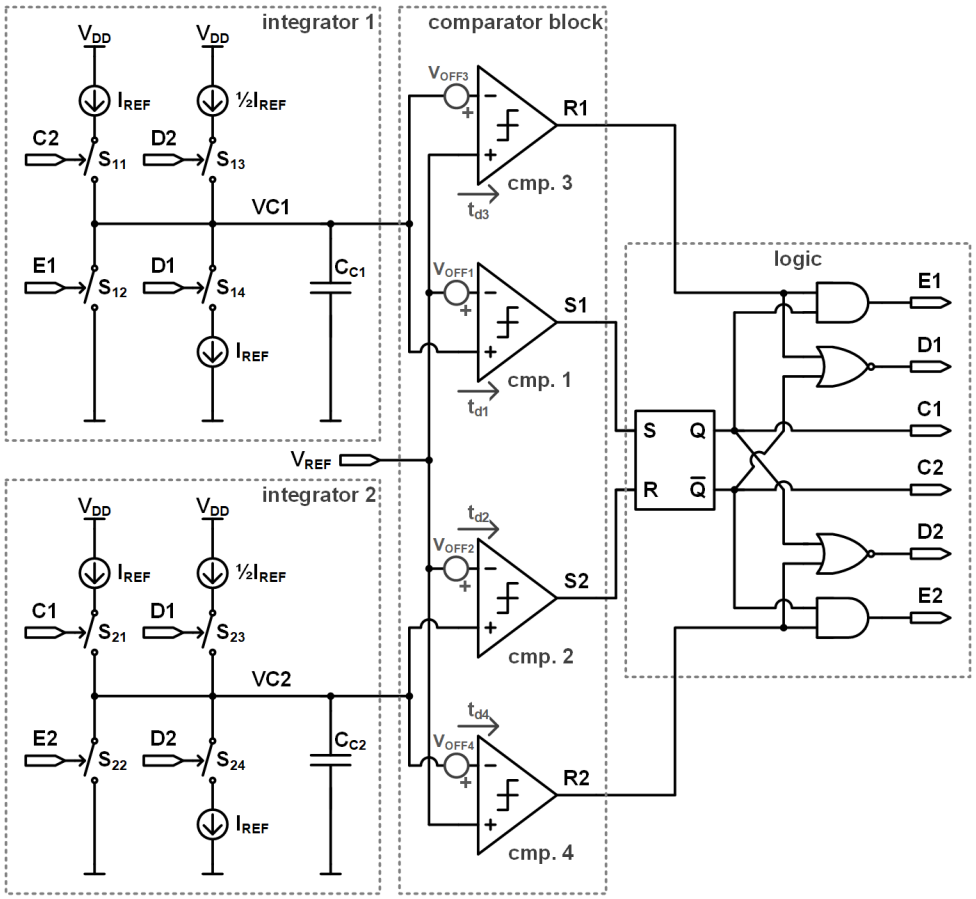


Figure 2.11: The schematic of the relaxation oscillator core with replica comparators, comprising two identical integrator blocks, a comparator block with two sensing and two replica comparators, and a logic block.

The operation of the relaxation oscillator core with replica comparators is described with reference to the corresponding signal waveforms in Fig. 2.12. At an initial time ($t = t_0$), it is presumed that all the signals are set to the initial state by a start–up circuit (not shown in the schematic). Initially, the integration occurs within the second integrator in the time interval from t_0 to t_2. The integrating voltage $VC2$ rises linearly, having the nominal slope $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the first integrator block remains idle as the integration node $VC1$ is shorted to the ground reference node V_{SS} by the switch S_{12}. At a subsequent time, $t = t_1$, the integrating signal $VC2$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the second comparator $S2$ changes state to high at $t = t_2$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. The timing can be expressed as follows:

$$t_2 = \frac{(V_{REF} + V_{OFF2})C_{REF}}{I_{REF}} + t_{d2}. \tag{2.10}$$

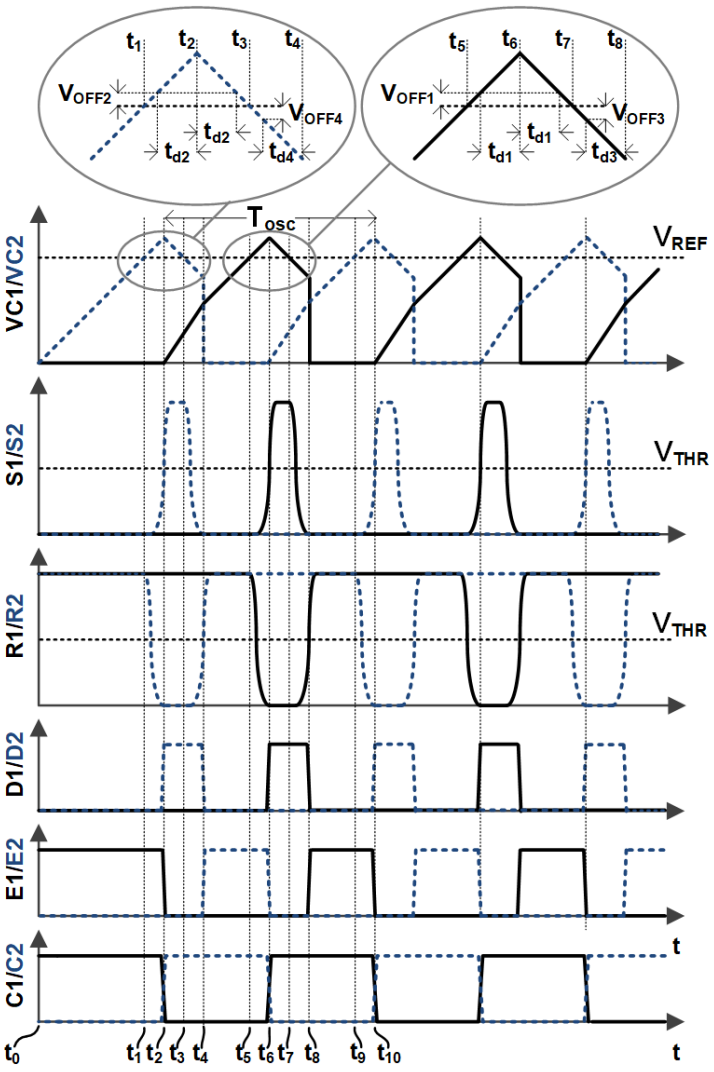


Figure 2.12: The signal waveforms of the relaxation oscillator core with replica comparators.

Following the change of the second comparator output $S2$, the logic block output signals $C1$, $C2$, and $D2$ also change to low, high, and high, respectively. Consequently, the integration starts within the first integrator block such that the integrating signal $VC1$ rises linearly, having the slope $\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC2$ starts to decrease, now having the opposite slope $\Delta VC2/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the counter–phase arrangement of the second and fourth comparator and the opposite slopes of the integrating voltage $VC2$ around the crossover points with the reference voltage V_{REF} ($t = t_1$ and $t = t_3$), the operation of the second (sensing) comparator in the time interval from t_1 to t_2 is replicated by the fourth (replica) comparator in the time interval from t_3 to t_4. Specifically, at $t = t_3$, the integrating signal $VC2$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the fourth comparator $R2$ changes to high at $t = t_4$ due to the non–ideal characteristics of the fourth comparator, namely the propagation delay t_{d4} and the offset voltage V_{OFF4}. In this way, as a function of the comparator outputs $S2$ and $R2$, the logic block generates a positive pulse on the measurement signal $D2$ in the time interval from t_2 to t_4, having the duration

$$t_{D2} = t_4 - t_2 = t_{d2} + t_{d4} + \frac{(V_{OFF2} + V_{OFF4})C_{REF}}{I_{REF}}. \tag{2.11}$$

The influence of the second comparator prior to $t = t_2$ is compensated with a 50% increase in the slope of the integrating signal $VC1$ compared to the nominal ($\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D2}. The voltage of the integration node $VC1$ at the time $t = t_4$, hereafter denoted $VC1(t_4)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D2}, and can be represented as follows:

$$VC1(t_4) = \Delta VC1/\Delta t \cdot t_{D2} = \frac{3I_{REF}}{2C_{REF}}(t_{d2} + t_{d4}) + \frac{3}{2}(V_{OFF2} + V_{OFF4}). \tag{2.12}$$

After $t = t_4$, the integrating signal $VC1$ continues to rise linearly, having the nominal slope $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the second integrator block is idle as the integration node $VC2$ is shorted to the ground reference node V_{SS} by the switch S_{22}. At a subsequent time, $t = t_5$, the integrating signal $VC1$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the first comparator $S1$ changes state to high at $t = t_6$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. The timing can be expressed as follows:

$$t_6 - t_4 = \frac{(V_{REF} + V_{OFF1} - VC1(t_4))C_{REF}}{I_{REF}} + t_{d1}. \tag{2.13}$$

Following the change of the first comparator output $S1$, the logic block output signals $C1$, $C2$, and $D1$ also change to high, low, and high, respectively. Consequently, the integration starts

within the second integrator block such that the integrating signal $VC2$ rises linearly, having the slope $\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC1$ starts to decrease, now having the opposite slope $\Delta VC1/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the counter–phase arrangement of the first and third comparator and the opposite slopes of the integrating voltage $VC1$ around the crossover points with the reference voltage V_{REF} ($t = t_5$ and $t = t_7$), the operation of the first (sensing) comparator in the time interval from t_5 to t_6 is replicated by the third (replica) comparator in the time interval from t_7 to t_8. Specifically, at $t = t_7$, the integrating signal $VC1$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the third comparator $R1$ changes to high at $t = t_8$ due to the non–ideal characteristics of the third comparator, namely the propagation delay t_{d3} and the offset voltage V_{OFF3}. In this way, as a function of the comparator outputs $S1$ and $R1$, the logic block generates a positive pulse on the measurement signal $D1$ in the time interval from t_6 to t_8, having the duration

$$t_{D1} = t_8 - t_6 = t_{d1} + t_{d3} + \frac{(V_{OFF1} + V_{OFF3})C_{REF}}{I_{REF}}. \tag{2.14}$$

The influence of the first comparator prior to $t = t_6$ is compensated with a 50% increase in the slope of the integrating signal $VC2$ compared to the nominal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D1}. The voltage of the integration node $VC2$ at the time $t = t_8$, hereafter denoted $VC2(t_8)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D1}, and can be represented as follows:

$$VC2(t_8) = \Delta VC2/\Delta t \cdot t_{D1} = \frac{3I_{REF}}{2C_{REF}}(t_{d1} + t_{d3}) + \frac{3}{2}(V_{OFF1} + V_{OFF3}). \tag{2.15}$$

After $t = t_8$, the integrating signal $VC2$ continues to rise linearly, having the nominal slope $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the first integrator block is idle as the integration node $VC1$ is shorted to the ground reference node V_{SS} by the switch S_{12}. At a subsequent time, $t = t_9$, the integrating signal $VC2$ becomes equal to the reference voltage V_{REF}. Nevertheless, the output of the second comparator $S2$ changes state to high at $t = t_{10}$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. The timing can be expressed as follows:

$$t_{10} - t_8 = \frac{(V_{REF} + V_{OFF2} - VC2(t_8))C_{REF}}{I_{REF}} + t_{d2}. \tag{2.16}$$

With this, a complete oscillation cycle is described from t_2 to t_{10}. The duration of one oscillation period can be calculated by adding the time segments as follows:

$$T_{osc} = (t_4 - t_2) + (t_6 - t_4) + (t_8 - t_6) + (t_{10} - t_8), \tag{2.17}$$

resulting in

$$T_{osc} = \frac{2(V_{REF} + ½\delta V_{OFF})C_{REF}}{I_{REF}} + \delta t_d, \tag{2.18}$$

where

$$\delta V_{OFF} = \frac{1}{2}(V_{OFF1} + V_{OFF2} - V_{OFF3} - V_{OFF4}) \tag{2.19}$$

and

$$\delta t_d = \frac{1}{2}(t_{d1} + t_{d2} - t_{d3} - t_{d4}). \tag{2.20}$$

As concluded from (2.18)–(2.20), the oscillation period of the proposed core is primarily determined by the values of the references (V_{REF}, I_{REF}, C_{REF}) since a non–zero value of the residual offset voltage δV_{OFF} and propagation delay δt_d is induced by the relative mismatch of the four comparators. This further implies that the influence of the systematic offset voltage of the comparators is fully compensated, whereas the random offset voltage is not addressed and can potentially compromise the performance. Moreover, in Section 2.3.2, it was demonstrated that the propagation delay variation is mainly related to the process parameters rather than mismatch, meaning that the residual delay δt_d is expected to be negligible. Other minor effects influencing the timing, such as the delay of the logic gates, switching non–idealities, parasitics, and mismatch between the integrator blocks, are neglected within this analysis.

2.4.2 Core Prototype

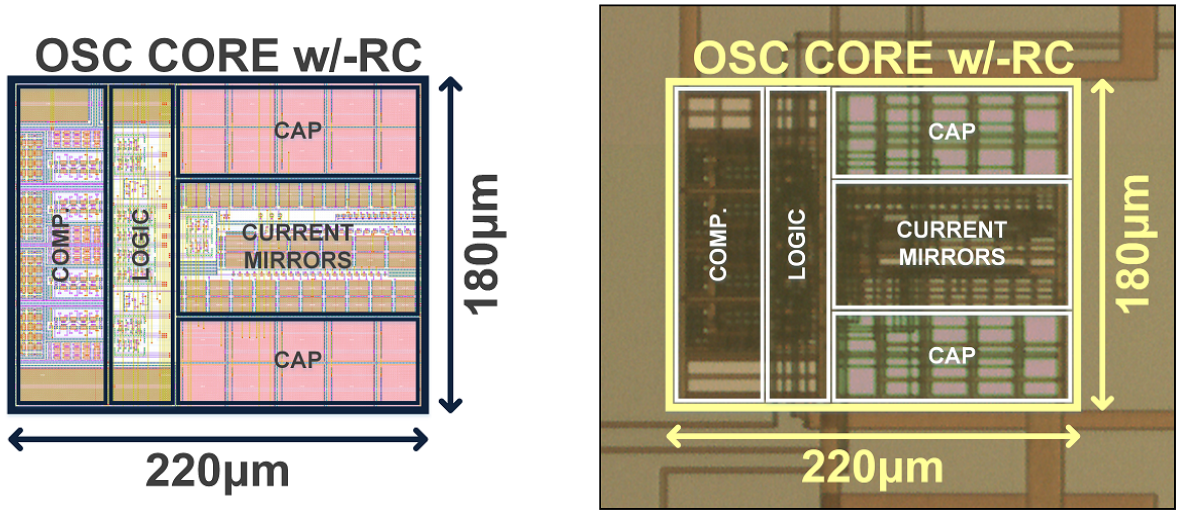
The 1–MHz prototype of the relaxation oscillator core with replica comparators from Fig. 2.11 is designed and manufactured in 0.35–µm technology. The prototype layout and the corresponding micro–photography of a manufactured sample are shown in Fig. 2.13, having a total area of 220 µm $\times$ 180 µm (0.04 mm^2).

The design parameters of the core prototype are shown in Table 2.2. The switches within the two integrator blocks (S_{11-14}, S_{21-24}), denoted as S_{int}, are identical and implemented with a single nMOS transistor. The two reference capacitors C_{C1-2} are polysilicon–insulator–polysilicon type (PIP). The schematic of four comparators used in the core is shown in Fig. 2.3b, comprising a symmetrical OTA (M_{P1-4} and M_{N1-4}) and an inverter buffer (M_{N5} and M_{P5}). The design parameters of the comparators are shown in Table 2.1.

Additionally, to compare the proposed core's performance to the conventional architecture, the core prototype includes the control circuitry which disables the operation of replica comparators. In this case, the oscillator architecture is reduced to the conventional relaxation oscillator (Fig. 2.1), having a nominal frequency of 0.85 MHz.

2.4.3 Reference Circuitry

A typical implementation of the relaxation oscillator core with replica comparators (Fig. 2.11) within a self–sustaining clock generator is shown in Fig. 2.14. The core requires a reference voltage V_{REF}, typically generated within a reference generator (VREF GEN). Furthermore, three required currents (shared between the two integrators) may be generated within a voltage to current converter block (V2I), having the value determined by the ratio of the reference



(a) (b)

Figure 2.13: The oscillator core with replica comparators prototype (a) layout (b) micro–photography. The core occupies an area of 0.04 mm^2.

Table 2.2: The design parameters of the relaxation oscillator core prototype with replica comparators.

Switch	W [µm]	L [µm]		Device
S_{int}	0.5	0.35		nmos3v
Capacitor	W [µm]	L [µm]	Cap [pF]	Device
C_{C1-2}[1:10]	21.4	22.2	4.16	cpip

W and L are single finger dimensions.
Cap is overall capacitance.

voltage V_{REF} and a reference resistance R_{REF}, further replicated within a current mirror block (CMIR). The current mirror block also provides the bias currents for the comparators (not shown in the schematic).

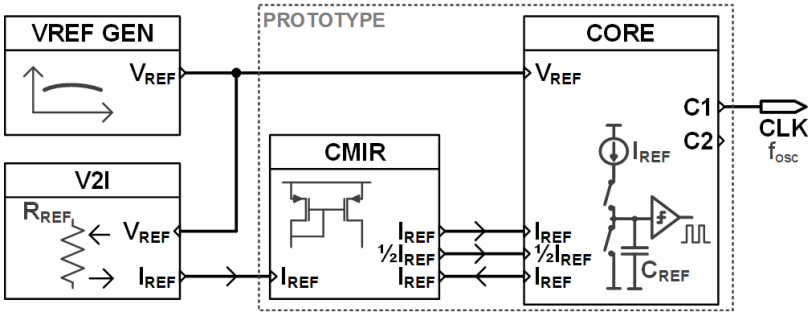


Figure 2.14: The diagram of the reference generation scheme, comprising the reference blocks (reference generator and voltage to current converter) and the current mirror block.

In this example, as seen in Fig. 2.14, the current mirror block (Fig. 2.15) is included within the prototype design, having the design parameters listed in Table 2.3. In order to limit its influence on the core performance, the current mirror is designed to provide an adequate matching between the three currents by using cascoded mirrors with a relatively large area of the devices. Furthermore, considering the following:

$$I_{REF} = V_{REF}/R_{REF}, \tag{2.21}$$

the expression for the oscillation period of the proposed core with replica comparators (2.18) becomes approximately equal to

$$T_{osc} \approx 2R_{REF}C_{REF}. \tag{2.22}$$

The test bench from Fig. 2.16 is assumed for the oscillator core transient simulations presented within the following section. The default value of the supply voltage is $V_{DD} = 3.3$ V, while the values of the externally sourced references are $V_{REF} = 1.2$ V for the reference voltage and $I_{REF} = 10$ µA for the reference current. Also, to offset the systematic first–order temperature coefficient of the reference PIP capacitor, the temperature dependency of the current I_{REF} is set to -40 ppm/°C.

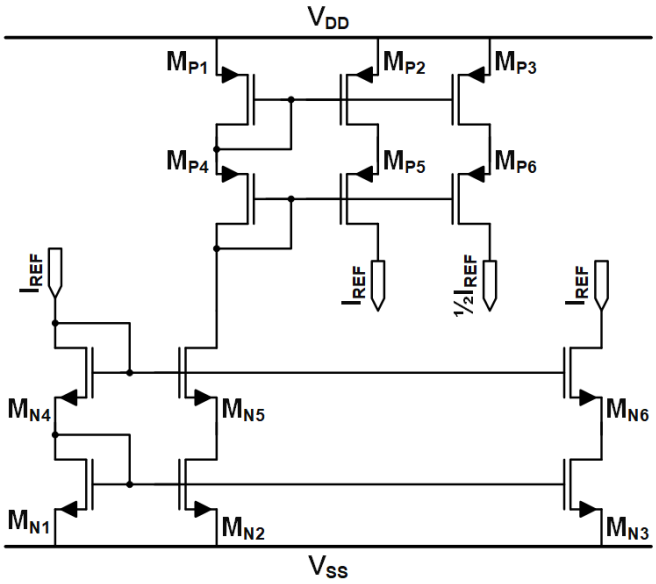


Figure 2.15: The schematic of the current mirror.

Table 2.3: The design parameters of the current mirror.

Transistor	W [µm]	L [µm]	Device
M_{N1-3}[1:4]	7.5	15	nmos3v
M_{N4-6}[1:4]	1	2	nmos3v
M_{P1-2}[1:4]	12.5	10	pmos3v
M_{P3}[1:2]	12.5	10	pmos3v
M_{P4-5}[1:4]	1.5	1	pmos3v
M_{P6}[1:2]	1.5	1	pmos3v

W and L are single finger dimensions.

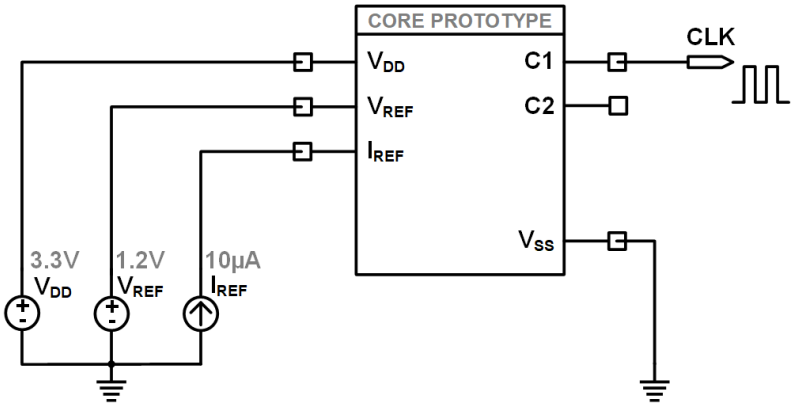


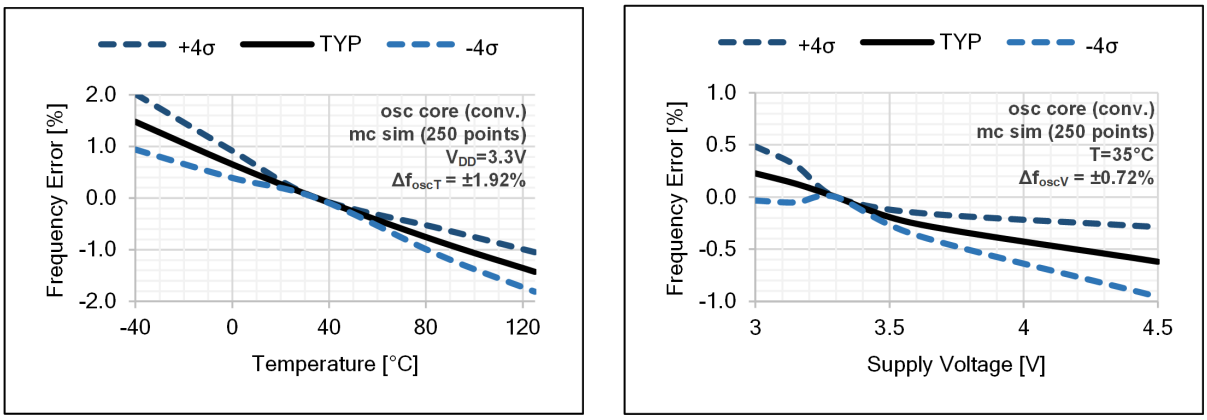
Figure 2.16: The test bench for the transient simulations of the oscillator core with replica comparators and the conventional oscillator core.

2.5 Simulation Results

The designed prototypes of the conventional oscillator core (conv.) and oscillator core with replica comparators (w/–RC) are simulated assuming the test setup described in Section 2.4.3. The oscillators consume around $P = 150$ µW ($I_{DD} \approx 45$ µA) and $P = 210$ µW ($I_{DD} \approx 64$ µA) at the nominal conditions ($T = 35$°C and $V_{DD} = 3.3$ V), having the average nominal frequency f_{osc0} of 0.85 MHz and 1 MHz, respectively. The cores start with a half–cycle delay (0.6 µs and 0.5 µs) after the settling of the references.

2.5.1 Temperature and Supply Variation

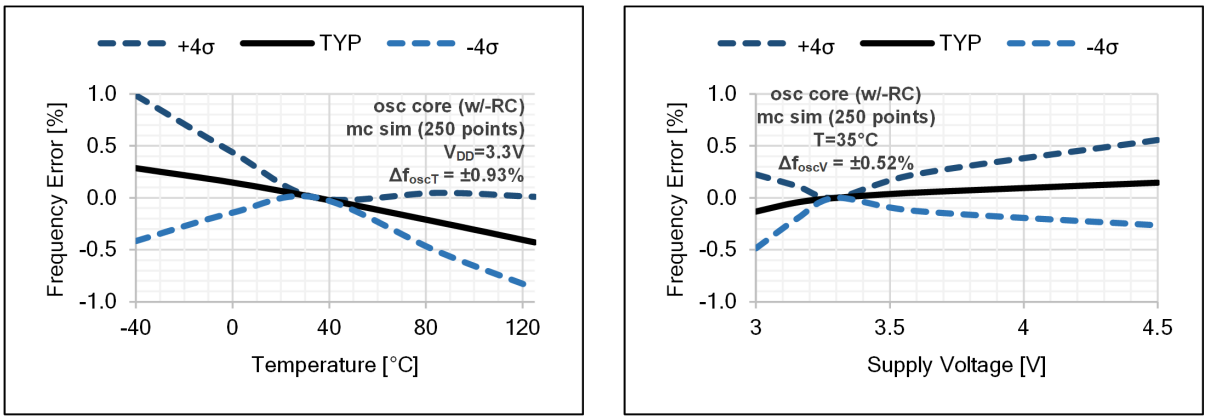
The simulated frequency variation of the conventional relaxation oscillator core versus temperature and supply voltage is shown in Fig. 2.17. The simulations are performed on 250 Monte Carlo points. The simulated frequency drift Δf_{oscT} versus temperature is from -1.81% to $+2.02\%$ in the temperature range from -40°C to 125°C. The simulated frequency drift Δf_{oscV} versus supply voltage is from -0.95% to $+0.49\%$ in the supply range from 3.0 V to 4.5 V.



(a) (b)

Figure 2.17: The simulated frequency error of the conventional relaxation oscillator core prototype vs. (a) temperature (at $V_{DD} = 3.3$ V) (b) supply voltage (at $T = 35$°C). The simulations are performed on 250 Monte Carlo points.

The simulated frequency variation of the proposed oscillator core with replica comparators versus temperature and supply voltage is shown in Fig. 2.18. The simulations are performed on 250 Monte Carlo points. The simulated frequency drift Δf_{oscT} versus temperature is from -0.87% to $+0.99\%$ in the temperature range from -40°C to 125°C. The simulated frequency drift Δf_{oscV} versus supply voltage is from -0.47% to $+0.56\%$ in the supply range from 3.0 V to 4.5 V.

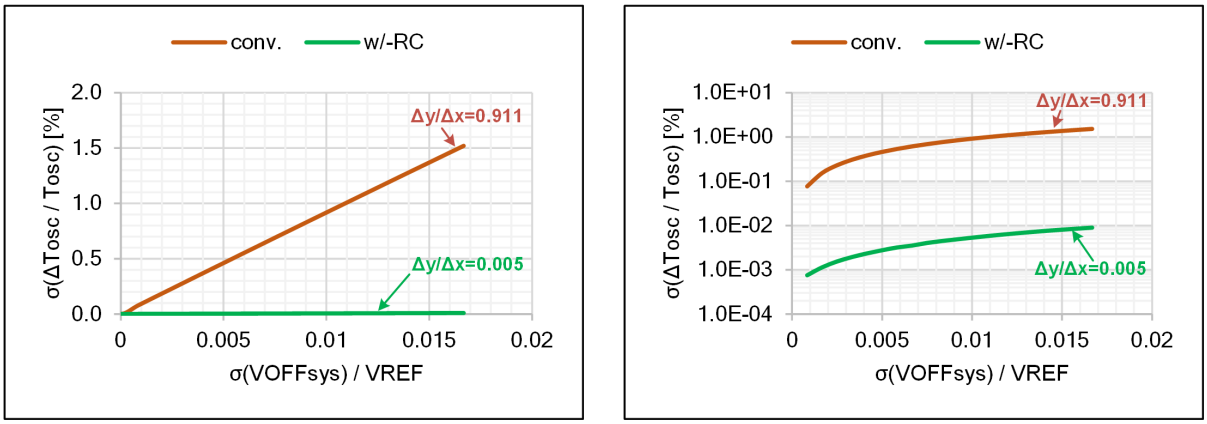


(a) (b)

Figure 2.18: The simulated frequency error of the proposed relaxation oscillator core prototype with replica comparators vs. (a) temperature (at $V_{DD} = 3.3$ V) (b) supply voltage (at $T = 35°C$). The simulations are performed on 250 Monte Carlo points.

2.5.2 Sensitivity to Offset Voltage

Fig. 2.19 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the systematic offset voltage (V_{OFFsys}) for the conventional core (conv.) and core with replica comparators (w/–RC). Here, the identical offset voltage is applied to all comparators in both cases, with the standard deviation $\sigma(V_{OFFsys})$ ranging from 0 mV to 20 mV. In both cases, the spread of the relative period error $\sigma(\Delta T_{osc}/T_{osc})$ is directly proportional to the systematic offset voltage relative spread $\sigma(V_{OFFsys})/V_{REF}$. For the conventional core, the simulated sensitivity of the oscillation period to the systematic offset voltage is $S_{VOFFsys} = 0.911$, while for the proposed core (w/–RC), the sensitivity is more than two orders of magnitude smaller, specifically $S_{VOFFsys} = 0.005$. In both cases, the results are in good accordance with the analytically predicted values from

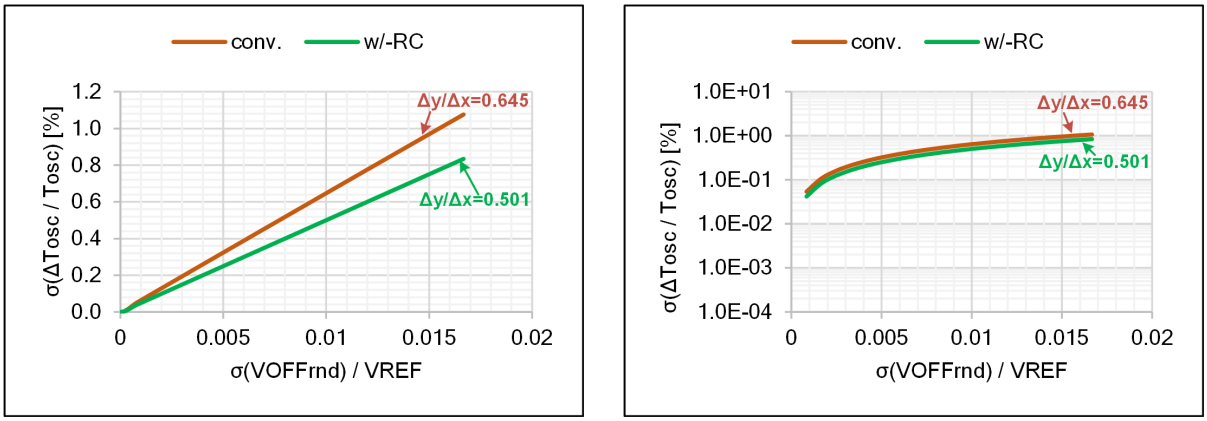


(a) (b)

Figure 2.19: The simulated sensitivity of the oscillation period to the systematic offset voltage, shown for the conventional (conv.) and proposed relaxation oscillator core with replica comparators (w/–RC) (a) plotted in linear scale (b) plotted in logarithmic scale.

Appendix B.1, particularly $S_{VOFFsys} = 1$ for the conventional core and $S_{VOFFsys} = 0$ for the proposed core (shown in (B.11) and (B.29), respectively).

Fig. 2.20 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the random offset voltage (V_{OFFrnd}) for the conventional core (conv.) and core with replica comparators (w/–RC). Here, the offset voltage of the comparators is assumed independent, with the standard deviation $\sigma(V_{OFFrnd})$ ranging from 0 mV to 20 mV. Again, the spread of the relative period error $\sigma(\Delta T_{osc}/T_{osc})$ rises proportionally with the random offset voltage relative spread $\sigma(V_{OFFrnd})/V_{REF}$. In this case, the simulated sensitivity is $S_{VOFFrnd} = 0.645$ for the conventional core and $S_{VOFFrnd} = 0.501$ for the proposed core (w/–RC). In both cases, the results are in good accordance with the analytically predicted values from Appendix B.1, specifically $S_{VOFFrnd} = 1/\sqrt{2}$ for the conventional core and $S_{VOFFrnd} = 0.5$ for the proposed core (shown in (B.16) and (B.39), respectively).



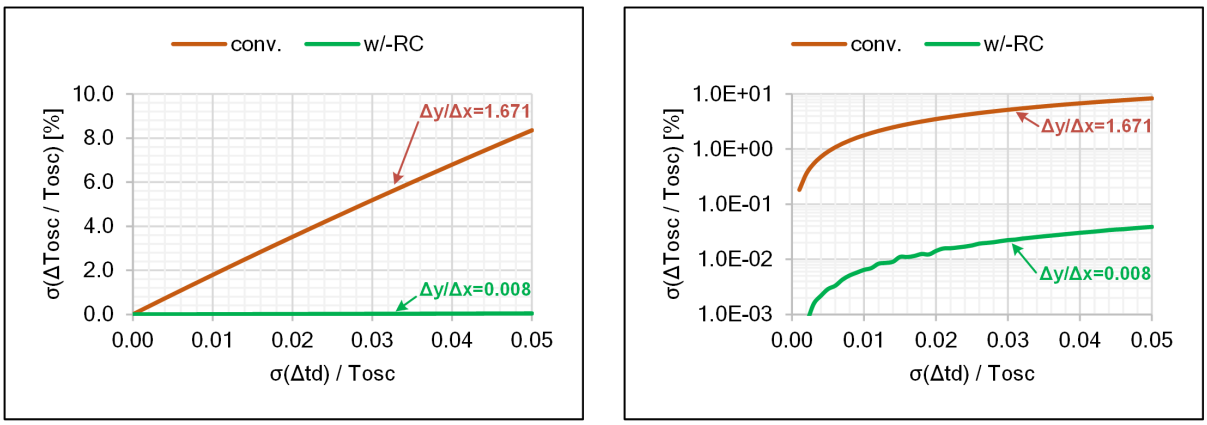
(a) (b)

Figure 2.20: The simulated sensitivity of the oscillation period to the random offset voltage, shown for the conventional (conv.) and proposed relaxation oscillator core with replica comparators (w/–RC) (a) plotted in linear scale (b) plotted in logarithmic scale.

2.5.3 Sensitivity to Propagation Delay

Fig. 2.21 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the propagation delay of the comparator (t_d) for the conventional core (conv.) and core with replica comparators (w/–RC). Here, all comparators are subjected to the same delay variation in both cases, with a standard deviation $\sigma(\Delta t_d)$ ranging from 0 ns to 50 ns. Similar to before, the spread of the relative period error $\sigma(\Delta T_{osc}/T_{osc})$ is directly proportional to the relative variation of the propagation delay $\sigma(\Delta t_d)/T_{osc}$. For the conventional core, the simulated sensitivity is $S_{td} = 1.671$, while for the proposed oscillator core with replica comparators (w/–RC), the sensitivity is more than two orders of magnitude lower, specifically $S_{td} = 0.008$. In both cases, the results are in good accordance with the analytically predicted values from Appendix B.2, specifically $S_{td} = 2$

for the conventional core and $S_{td} = 0$ for the proposed core (shown in (B.50) and (B.63), respectively).



(a) (b)

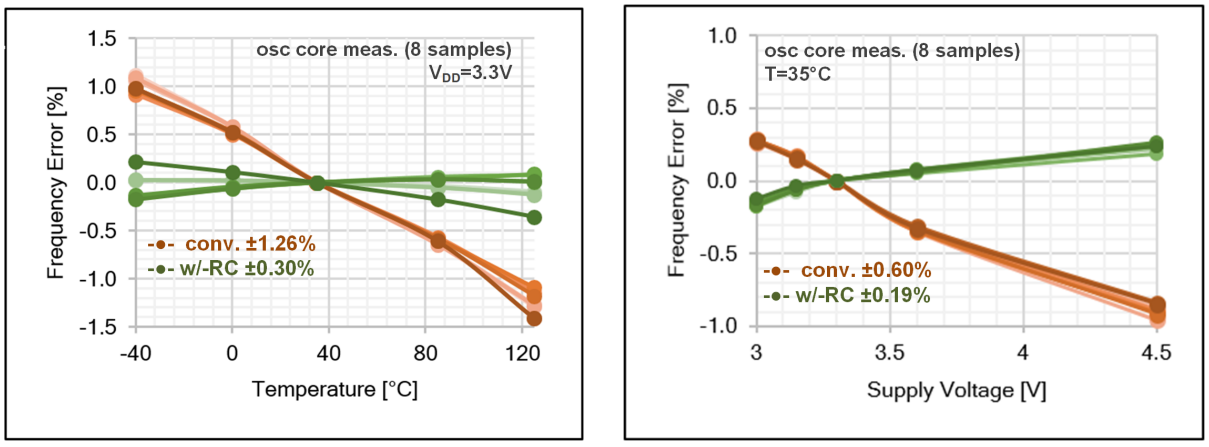
Figure 2.21: The simulated sensitivity of the oscillation period to the comparator delay, shown for the conventional (conv.) and proposed relaxation oscillator core with replica comparators (w/–RC) (a) plotted in linear scale (b) plotted in logarithmic scale.

2.6 Measurement Results

The relaxation oscillator prototype with replica comparators (w/–RC), shown in Fig. 2.13, is manufactured in 0.35–µm CMOS technology with eight samples packaged for measurement. The reference voltage and current (V_{REF} and I_{REF}) are sourced externally, according to Fig. 2.16. The nominal frequency f_{osc0} of the measured samples is around 1 MHz, consuming around $P = 210$ µW ($I_{DD} \approx 64$ µA) under the typical conditions ($T = 35°$C and $V_{DD} = 3.3$ V). The measured process sensitivity of the pre–calibrated frequency is $\sigma(f_{osc0})/\mu(f_{osc0}) = 1.1\%$. Furthermore, the samples are also measured with disabled measurement and compensation circuitry (implying the conventional topology from Fig. 2.1). In this case, the conventional core prototype typically consumes around $P = 150$ µW ($I_{DD} \approx 45$ µA) and has a nominal frequency f_{osc0} of around 850 kHz.

2.6.1 Temperature and Supply Variation

The measured frequency variation versus temperature is plotted in Fig. 2.22a for the conventional core (conv.) and the proposed core with replica comparators (w/–RC). The measured frequency drift Δf_{oscT} versus temperature is from -1.42% to $+1.09\%$ for the conventional core (conv.) and from -0.36% to $+0.23\%$ for the proposed core (w/–RC), both measured in the temperature range from $-40°$C to $125°$C. Therefore, the proposed core with replica comparators (w/–RC) exhibits an improvement of around four times compared to the conventional core ($\pm 0.3\%$ vs. $\pm 1.26\%$). At this point, the temperature variation of the current sources becomes the main contributor to the residual frequency drift. The delay of the logic gates, however, is relatively negligible at the frequency of 1 MHz. Once the internal references are included, the



(a) (b)

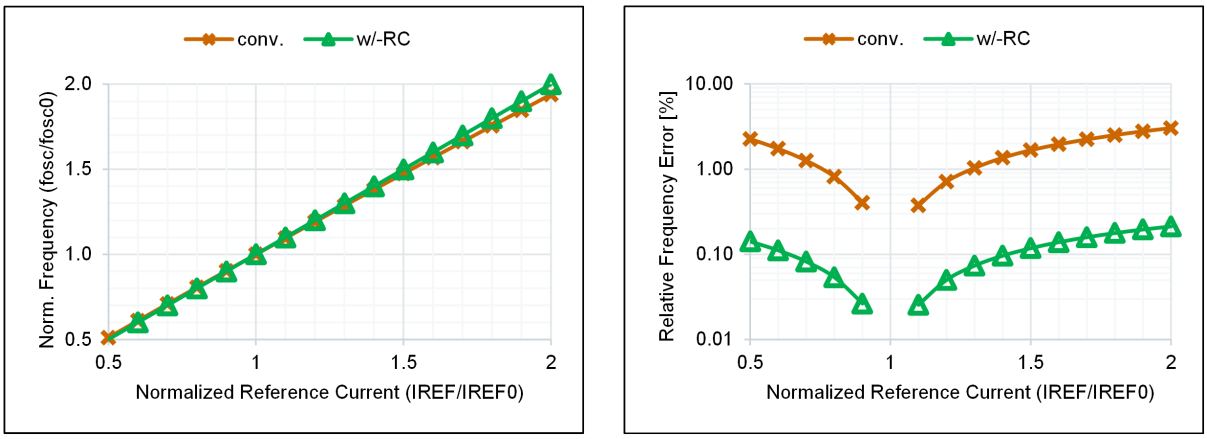
Figure 2.22: The measured frequency error of the conventional (conv.) and proposed (w/–RC) relaxation oscillator core vs. (a) temperature (at $V_{DD} = 3.3$ V) (b) supply voltage (at $T = 35°$C). The measurements are performed on eight test chip samples.

overall temperature sensitivity is expected to be dominated by the second–order temperature coefficient of the on–chip composite resistor [13], usually contributing with more than $\pm 0.5\%$.

The measured frequency variation versus supply voltage is shown in Fig. 2.22b for the conventional (conv.) and the proposed core with replica comparators (w/–RC). The frequency drift Δf_{oscV} versus supply voltage is from -0.92% to $+0.28\%$ for the conventional core (conv.) and from -0.13% to $+0.24\%$ for the proposed core (w/–RC), both measured in the supply range from 3.0 V to 4.5 V. Therefore, the proposed core with replica comparators (w/–RC) exhibits an improvement of more than three times compared to the conventional core ($\pm 0.19\%$ vs. $\pm 0.6\%$). Considering the typically low voltage sensitivity of the bandgap references, on–chip resistors, and voltage–to–current converters, the line sensitivity is expected to remain limited after implementing the internal reference block.

2.6.2 Control Linearity

The response of the normalized output frequency f_{osc}/f_{osc0} to the normalized control current I_{REF}/I_{REF0} is measured for the conventional (conv.) and proposed (w/–RC) relaxation oscillator core. The measurements are performed on eight samples for each core under the nominal conditions ($T = 35°\text{C}$ and $V_{DD} = 3.3$ V). The results of typical samples are plotted in Fig. 2.23.



(a) (b)

Figure 2.23: (a) The typical normalized frequency response vs. the normalized reference current, shown for the conventional (conv.) and proposed (w/–RC) relaxation oscillator core. (b) The relative error of the normalized frequency (compared to the ideal case $y = x$) vs. the normalized reference current.

Following the third–order polynomial fitting of the measured data, specifically

$$y = c_3 x^3 + c_2 x^2 + c_1 x + c_0, \tag{2.23}$$

the second and third harmonic distortion figures (HD_2 and HD_3) are calculated using [63]

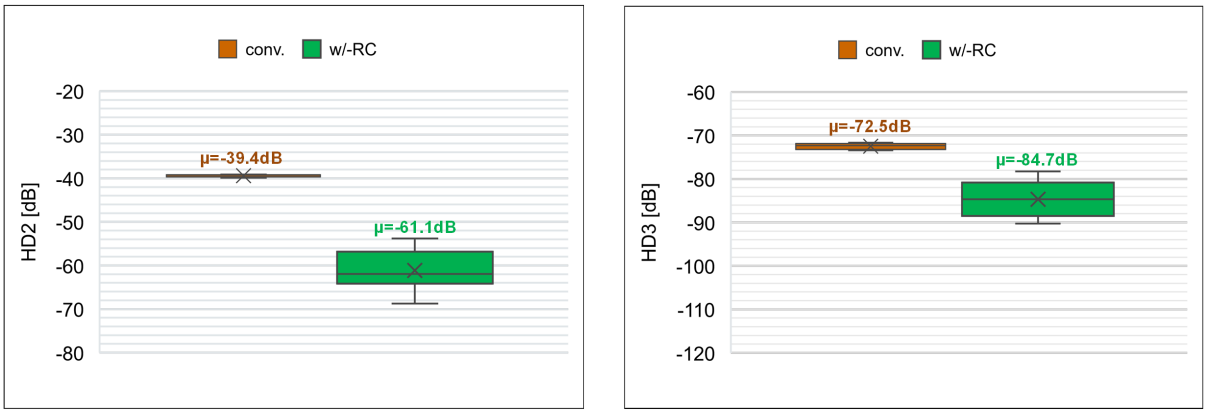
$$HD_2[dB] = 20log\left(\frac{1}{2}A_c\left|\frac{c_2}{c_1}\right|\right) \tag{2.24}$$

and

$$HD_3[dB] = 20log\left(\frac{1}{4}A_c^2\left|\frac{c_3}{c_1}\right|\right), \tag{2.25}$$

where c_1, c_2, and c_3 are the polynomial coefficients from (2.23), and A_c is the amplitude of the control signal, specifically the normalized control current I_{REF}/I_{REF0}.

The mean values of the distortion parameters are equal to $HD_2 = -39.4$ dB and $HD_3 = -72.5$ dB for the conventional core (conv.) and $HD_2 = -61.1$ dB and $HD_3 = -84.7$ dB for the proposed core (w/–RC), both calculated with $\Delta f_{osc} = 500$ kHz ($\Delta I_{REF}/I_{REF0} = 0.5$). The results of the measured samples are presented in Fig. 2.24. As concluded from the presented results, the elimination of the delay of the comparators results in a significant improvement in control linearity.

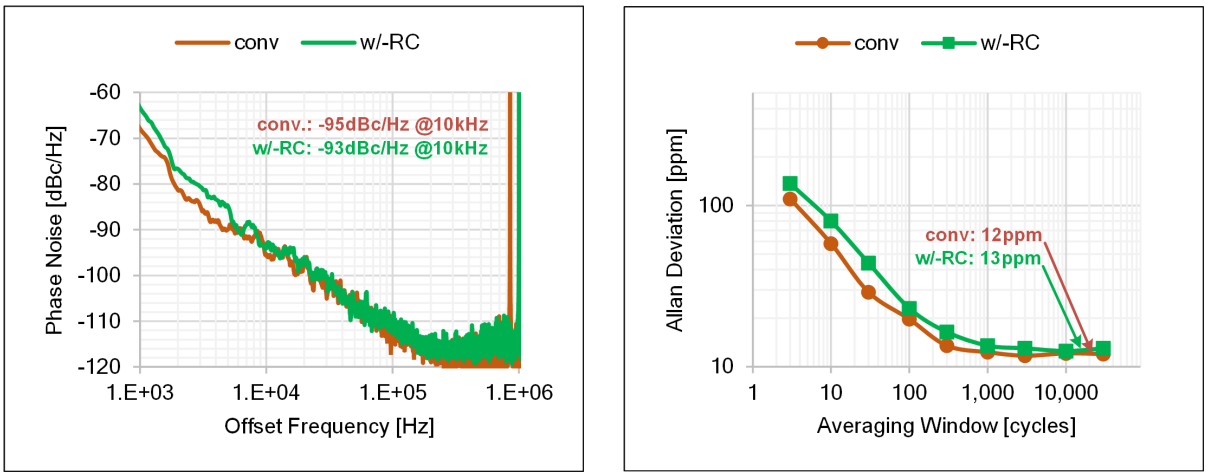


(a) (b)

Figure 2.24: The distortion parameters of the control characteristic, shown for the conventional (conv.) and proposed (w/–RC) relaxation oscillator core. (a) HD_2 (b) HD_3. The distortion parameters are calculated for $\Delta f_{osc} = 500$ kHz.

2.6.3 Noise Performance

The noise performance of the conventional (conv.) and proposed (w/–RC) relaxation oscillator core is evaluated using the phase noise and Allan deviation measurements, shown in Fig. 2.25. The measurements are performed under the nominal conditions ($T = 35°$C and $V_{DD} = 3.3$ V). The period jitter is $\sigma_{Tosc} = 195$ ppm for the conventional (conv.) and $\sigma_{Tosc} = 230$ ppm for the proposed (w/–RC) relaxation oscillator core, while the phase noise at 10 kHz and Allan deviation floor are -95 dBc/Hz and -93 dBc/Hz, and $\sigma_y = 12$ ppm and $\sigma_y = 13$ ppm, respectively.



(a) (b)

Figure 2.25: (a) The phase noise measurement of the conventional (conv.) and proposed (w/–RC) relaxation oscillator core. (b) The Allan deviation vs. averaging window length for the conventional (conv.) and proposed (w/–RC) relaxation oscillator core.

2.7 Summary

In this chapter, the conventional relaxation oscillator topology was presented and discussed in detail. Furthermore, the influence of the comparator–related effects on the timing was analytically evaluated. Next, the improved relaxation oscillator design with replica comparators was introduced, compensating for the propagation delay and systematic offset voltage of the comparator stage. The performance improvements of the proposed core were demonstrated with the sensitivity analysis, simulations, and, eventually, the measurements of the manufactured core prototype. The prototype designed in 0.35–µm CMOS technology has an area of 0.04 mm^2, typically operates at 1 MHz, and consumes around $I_{DD} = 64$ µA. The measured frequency drift is $\pm 0.3\%$ in the temperature range from -40°C to 125°C and $\pm 0.19\%$ in the supply range from 3.0 V to 4.5 V. The design and performance overview for the proposed core prototype is shown in Table 2.4. In conclusion, the performance of the proposed core is improved significantly compared to the conventional core, showing a substantial improvement in frequency drift versus temperature and supply voltage, control linearity, and sensitivity to comparator offset voltage and propagation delay.

Table 2.4: The design and performance summary of the relaxation oscillator core with replica comparators (w/–RC).

Parameter	Description	Value	Unit	Conditions
	Technology	350	nm	
A	Area	0.04	mm^2	
f_{osc0}	Nominal Frequency	1	MHz	nominal
P	Power	210	µW	nominal
V_{DD}	Supply Voltage	3.3	V	
Δf_{oscT}	[a]Drift vs. Temperature	± 0.93	%	$T = -40 \sim 125$°C
Δf_{oscV}	[a]Drift vs. Supply	± 0.52	%	$V_{DD} = 3.0 \sim 4.5$ V
$t_{startup}$	[a]Start–Up Time	0.5	µs	nominal
σ_{Tosc}	[b]Period Jitter	230	ppm	nominal
HD_2/HD_3	[b]Distortion Parameters	–61.1/–84.7	dB	$\Delta f_{osc} = 500$ kHz
$\mathscr{L}(f)$	[b]Phase Noise	–93	dBc/Hz	$f_m = 10$ kHz
$\sigma_y(\tau)$	[b]Allan Deviation Floor	13	ppm	$\tau = 30$k cycles
$S_{VOFFsys}$	[a]Sensitivity to Syst. Offset Volt.	0.005	$1/V_{REF}$	nominal
$S_{VOFFrnd}$	[a]Sensitivity to Random Offset Volt.	0.501	$1/V_{REF}$	nominal
S_{td}	[a]Sensitivity to Propagation Delay	0.008	$1/T_{osc}$	nominal

[a]Simulated. [b]Measured.

Chapter 3

Relaxation Oscillator Core with Self–Compensating Chopped Comparator

3.1 Motivation

The relaxation oscillator core architecture with replica comparators was introduced in the previous chapter, having a potential for significant performance enhancement by compensating for the effects of the comparator stage. Nevertheless, the presented offset and delay cancellation method based on replica comparators accounts only for the systematic timing contributions and becomes less effective with a more significant mismatch between the comparators. This limitation is particularly noticeable when the design scales to a smaller size and low power, where random effects are more pronounced [58]. These random effects may be partially resolved with a chopper architecture, as demonstrated in [8, 9], where chopping a single comparator entirely cancels the offset voltage (including the random effects) but does not influence the propagation delay. Likewise, the two comparator pairs within the relaxation oscillator core with replica comparators (Fig. 2.11) can be replaced with a single chopped comparator and replica pair since only one pair is active at a time. Furthermore, the adaptation of the switching scheme of the chopper such that the sensing and replica comparators are alternated with each half–cycle enables the cancellation of both the random and systematic non–idealities of the comparator stage.

In this sense, a further improved core architecture [54] is proposed within this chapter, comprising a self–compensating chopped comparator that entirely cancels the propagation delay and offset voltage of the comparators. The core prototype is manufactured in 0.35–µm CMOS technology, exhibiting an additional performance improvement. Also, reducing the number of comparators from four to two decreases the chip area and power consumption.

3.2 Relaxation Oscillator Core with Self–Compensating Chopped Comparator

3.2.1 Core Architecture

The schematic of the relaxation oscillator core employing a self–compensating chopped comparator [54] is presented in Fig. 3.1. The oscillator core consists of two integrator blocks, a chopped comparator block, a masking block, and a logic block. Each integrator block includes three current sources (the first and third having the reference current I_{REF} and the second one having half the reference current $½I_{REF}$), four switches controlled by the output signals of the logic block, and the capacitor having the capacitance value C_{REF}. The chopped comparator block consists of two switching blocks and two identically designed comparators in counter–phase arrangement. The operation of the switching blocks is described by the signal mappings shown in Fig. 3.1, defining the two states of the chopper depending on the corresponding control signals. Furthermore, the masking block regulates the propagation of the chopper output signals to the logic block, preserving the signal integrity. Finally, the logic block processes the chopper outputs into the control signals, feeding them back to the integrator block, chopped comparator block, and masking block, maintaining the oscillation in this way. Compared to the oscillator core with replica comparators from Section 2.4, the comparator stage is implemented as a chopped comparator pair instead of four comparators.

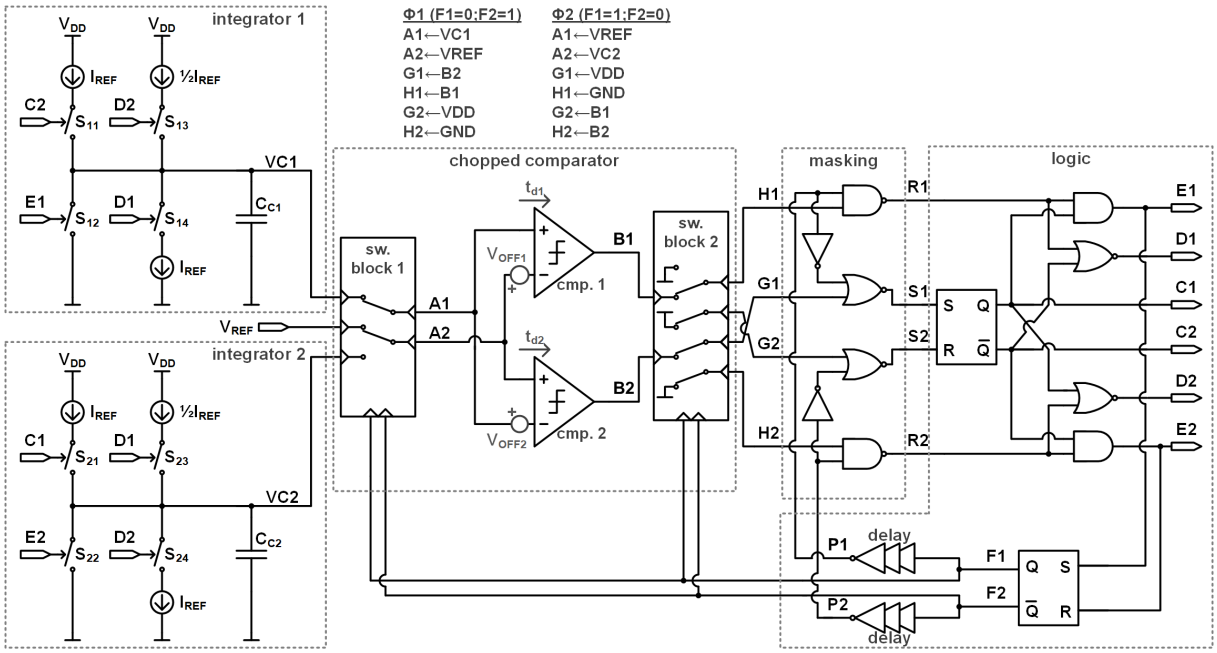


Figure 3.1: The schematic of the relaxation oscillator core with self–compensating chopped comparator, comprising two identical integrator blocks, a chopped comparator block, a masking block, and a logic block.

The operation of the relaxation oscillator core in Fig. 3.1 is described with reference to the corresponding signal waveforms shown in Fig. 3.2. At an initial time ($t = t_0$), it is presumed that all the signals are set to the initial state by a start–up circuit (not shown in the schematic). Initially, the chopper state is set to ϕ_2, and the integration occurs within the second integrator in the time interval from t_0 to t_2. The integrating voltage $VC2$ rises linearly, having the nominal slope $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. Due to the initial configuration of the chopper, while $F1$ is high and $F2$ is low, the integrating signal $VC2$ is present at the switch output $A2$ ($VC2 \mapsto A2$). Meanwhile, the first integrator block remains idle as the integration node $VC1$ is shorted to the ground reference node V_{SS} by the switch S_{12}. At a subsequent time, $t = t_1$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), becomes equal to the reference voltage V_{REF} also present at the switch output $A1$ ($V_{REF} \mapsto A1$). Nevertheless, the output of the first comparator $B1$, also present at the chopper output $G2$ ($B1 \mapsto G2$), changes state to low at $t = t_2$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. Simultaneously, the latch reset signal $S2$ changes state to high. The timing can be expressed as follows:

$$t_2 = \frac{(V_{REF} + V_{OFF1})C_{REF}}{I_{REF}} + t_{d1}. \tag{3.1}$$

Following the change of the latch reset signal $S2$, the logic block output signals $C1$, $C2$, $D2$, and $E1$ also change to low, high, high, and low, respectively. Consequently, the integration starts within the first integrator block such that the integrating signal $VC1$ rises linearly, having the slope $\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC2$, also present at the switch output $A2$ ($VC2 \mapsto A2$), starts to decrease, now having the opposite slope $\Delta VC2/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the counter–phase arrangement of the first and second comparator and the opposite slopes of the integrating voltage $VC2$ around the crossover points with the reference voltage V_{REF} ($t = t_1$ and $t = t_3$), the operation of the first (sensing) comparator in the time interval from t_1 to t_2 is replicated by the second (replica) comparator in the time interval from t_3 to t_4. Specifically, at $t = t_3$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), becomes equal to the reference voltage V_{REF} also present at the switch output $A1$ ($V_{REF} \mapsto A1$). Nevertheless, the second comparator reaches the switching point at $t = t_4$ due to the propagation delay t_{d2} and the offset voltage V_{OFF2}. In this way, as a function of the comparator outputs $B1$ and $B2$, present at the chopper outputs $G2$ ($B1 \mapsto G2$) and $H2$ ($B2 \mapsto H2$), the logic block generates a positive pulse on the measurement signal $D2$ in the time interval from t_2 to t_4, having the duration

$$t_{D2} = t_4 - t_2 = t_{d1} + t_{d2} + \frac{(V_{OFF1} + V_{OFF2})C_{REF}}{I_{REF}}. \tag{3.2}$$

The influence of the first comparator prior to $t = t_2$ is compensated with a 50% increase in the

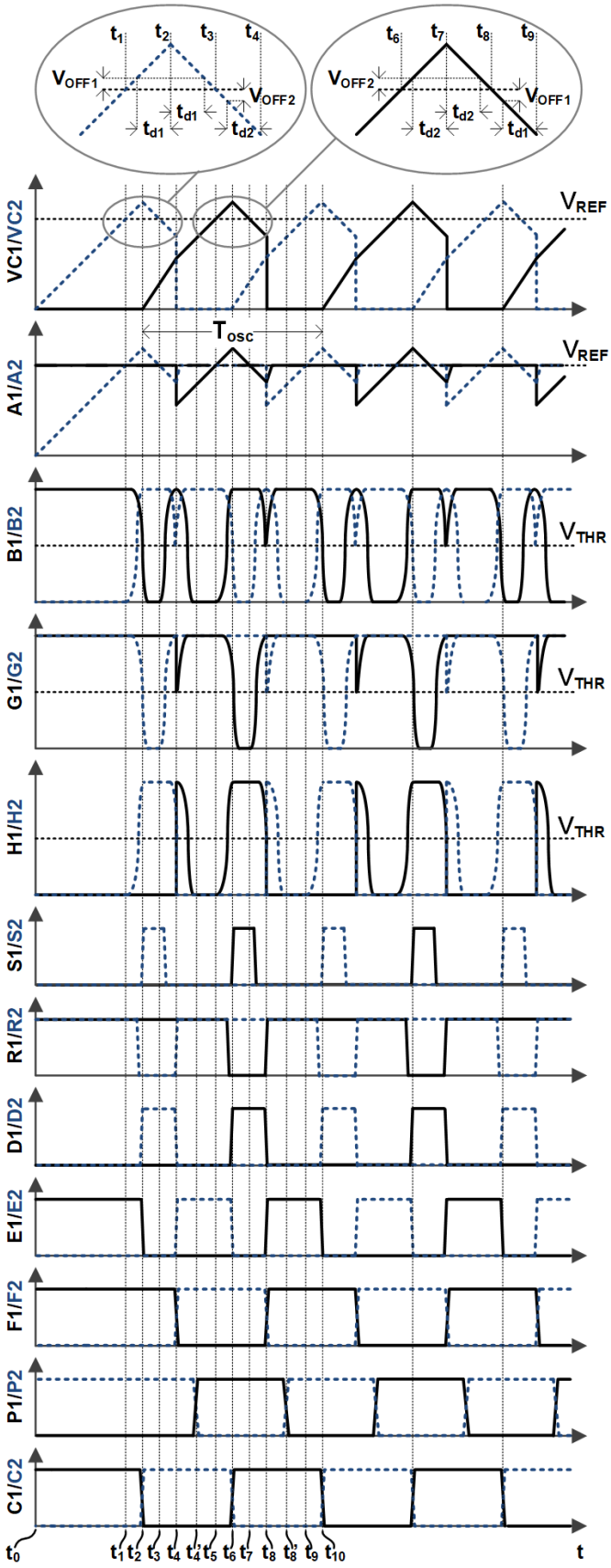


Figure 3.2: The signal waveforms of the relaxation oscillator core with self–compensating chopped comparator.

slope of the integrating signal $VC1$ compared to the nominal ($\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D2}. The voltage of the integration node $VC1$ at the time $t = t_4$, hereafter denoted $VC1(t_4)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC1/\Delta t = 1.5I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D2}, and can be represented as follows:

$$VC1(t_4) = \Delta VC1/\Delta t \cdot t_{D2} = \frac{3I_{REF}}{2C_{REF}}(t_{d1} + t_{d2}) + \frac{3}{2}(V_{OFF1} + V_{OFF2}). \tag{3.3}$$

Following the rising edge of the signal $R2$ at $t = t_4$, the logic block output signals $E2$, $F1$, and $F2$ change to high, low, and high, respectively. Consequently, the chopper state is set to ϕ_1. After $t = t_4$, the integrating signal $VC1$, now present at the switch output $A1$ ($VC1 \mapsto A1$), continues to rise linearly, having the nominal slope $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the second integrator block is idle as the integration node $VC2$ is shorted to the ground reference node V_{SS} by the switch S_{22}. The masking block input signals $P1$ and $P2$ change to high and low, respectively, at a slightly delayed time, namely $t = t_4'$, to prevent the propagation of the glitches caused by chopper operation to the logic block. At a subsequent time, $t = t_5$, the integrating signal $VC1$, which is present at the switch output $A1$ ($VC1 \mapsto A1$), becomes equal to the reference voltage V_{REF} also present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the output of the second comparator $B2$, also present at the chopper output $G1$ ($B2 \mapsto G1$), changes state to low at $t = t_6$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. Simultaneously, the latch set signal $S1$ changes state to high. The timing can be expressed as follows:

$$t_6 - t_4 = \frac{(V_{REF} + V_{OFF2} - VC1(t_4))C_{REF}}{I_{REF}} + t_{d2}. \tag{3.4}$$

Following the change of the latch set signal $S1$, the logic block output signals $C1$, $C2$, $D1$, and $E2$ also change to high, low, high, and low, respectively. Consequently, the integration starts within the second integrator block such that the integrating signal $VC2$ rises linearly, having the slope $\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC1$, also present at the switch output $A1$ ($VC1 \mapsto A1$), starts to decrease, now having the opposite slope $\Delta VC1/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the counter–phase arrangement of the first and second comparator and the opposite slopes of the integrating voltage $VC1$ around the crossover points with the reference voltage V_{REF} ($t = t_5$ and $t = t_7$), the operation of the second (sensing) comparator in the time interval from t_5 to t_6 is replicated by the first (replica) comparator in the time interval from t_7 to t_8. Specifically, at $t = t_7$, the integrating signal $VC1$, which is present at the switch output $A1$ ($VC1 \mapsto A1$), becomes equal to the reference voltage V_{REF} also present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the first comparator reaches the switching point at $t = t_8$ due to the propagation delay t_{d1} and the offset voltage V_{OFF1}. In this way, as a

function of the comparator outputs $B1$ and $B2$, present at the chopper outputs $H1$ ($B1 \mapsto H1$) and $G1$ ($B2 \mapsto G1$), the logic block generates a positive pulse on the measurement signal $D1$ in the time interval from t_6 to t_8, having the duration

$$t_{D1} = t_8 - t_6 = t_{d1} + t_{d2} + \frac{(V_{OFF1} + V_{OFF2})C_{REF}}{I_{REF}}. \tag{3.5}$$

The influence of the second comparator prior to $t = t_6$ is compensated with a 50% increase in the slope of the integrating signal $VC2$ compared to the nominal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D1}. The voltage of the integration node $VC2$ at the time $t = t_8$, hereafter denoted $VC2(t_8)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D1}, and can be represented as follows:

$$VC2(t_8) = \Delta VC2/\Delta t \cdot t_{D1} = \frac{3I_{REF}}{2C_{REF}}(t_{d1} + t_{d2}) + \frac{3}{2}(V_{OFF1} + V_{OFF2}). \tag{3.6}$$

Following the rising edge of the signal $R1$ at $t = t_8$, the logic block output signals $E1$, $F1$, and $F2$ change to high, high, and low, respectively. After $t = t_8$, the integrating signal $VC2$, now present at the switch output $A2$ ($VC2 \mapsto A2$), continues to rise linearly, having the nominal slope $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. Meanwhile, the first integrator block is idle as the integration node $VC1$ is shorted to the ground reference node V_{SS} by the switch S_{12}. The masking block input signals $P1$ and $P2$ change to low and high, respectively, at a slightly delayed time, namely $t = t_8'$, to prevent the propagation of the glitches caused by chopper operation to the logic block. At a subsequent time, $t = t_9$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), becomes equal to the reference voltage V_{REF} also present at the switch output $A1$ ($V_{REF} \mapsto A1$). Nevertheless, the output of the first comparator $B1$, also present at the chopper output $G2$ ($B1 \mapsto G2$), changes state to low at $t = t_{10}$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. Simultaneously, the latch reset signal $S2$ changes state to high. The timing can be expressed as follows:

$$t_{10} - t_8 = \frac{(V_{REF} + V_{OFF1} - VC2(t_8))C_{REF}}{I_{REF}} + t_{d1}. \tag{3.7}$$

With this, a complete oscillation cycle is described from t_2 to t_{10}. The duration of one oscillation period can be calculated by adding the time segments as follows:

$$T_{osc} = (t_4 - t_2) + (t_6 - t_4) + (t_8 - t_6) + (t_{10} - t_8), \tag{3.8}$$

resulting in

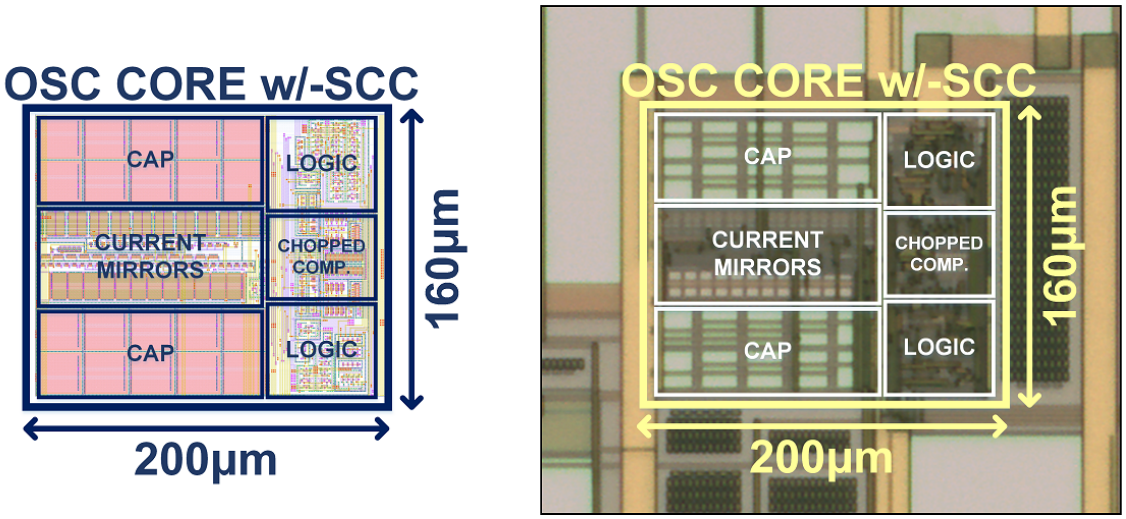
$$T_{osc} = \frac{2V_{REF}C_{REF}}{I_{REF}}. \tag{3.9}$$

Conclusively, the proposed architecture entirely compensates for the influence of the comparator stage, where the self–compensating chopped comparator pair enables the measurement of the propagation delay and offset voltage of the comparators and compensation by boosting the integration cycle by the same amount. Accordingly, the period becomes primarily determined by the values of the references (V_{REF}, I_{REF}, C_{REF}), along with other minor effects neglected within the analysis (e.g., delay of the logic gates, switching non–idealities, parasitics, and mismatch between the integrator blocks).

3.2.2 Core Prototype

The 1–MHz prototype of the relaxation oscillator core with self–compensating chopped comparator from Fig. 3.1 is designed and manufactured in 0.35–µm technology. The prototype layout and the corresponding micro–photography of a manufactured sample are shown in Fig. 3.3, having a total area of 200 µm × 160 µm (0.032 mm^2).

The design parameters of the core prototype are shown in Table 3.1. The switches within the two integrator blocks (S_{11-14}, S_{21-24}), denoted as S_{int}, are identical and implemented with a single nMOS transistor. On the other hand, the switches within the two switching blocks, denoted as S_{chop}, are implemented as CMOS analog switches with identically sized nMOS and pMOS transistors. The two reference capacitors C_{C1-2} are polysilicon–insulator–polysilicon type (PIP). The schematic of the two chopped comparators used in the core is shown in Fig. 3.4, consisting of an OTA (M_{N1-2} and M_{P1-2}) and an inverter buffer (M_{N3} and M_{P3}). The design parameters of the comparators are shown in Table 3.2. In contrast to the oscillator core



(a) (b)

Figure 3.3: The oscillator core with self–compensating chopped comparator prototype (a) layout (b) micro–photography. The core occupies an area of 0.032 mm^2.

Table 3.1: The design parameters of the relaxation oscillator core prototype with self–compensating chopped comparator.

Switch	W [µm]	L [µm]		Device
S_{int}	0.5	0.35		nmos3v
S_{chop}	0.5	0.35		nmos3v+pmos3v
Capacitor	**W [µm]**	**L [µm]**	**Cap [pF]**	**Device**
C_{C1-2}[1:10]	21.4	22.2	4.16	cpip

W and L are single finger dimensions.
Cap is overall capacitance.

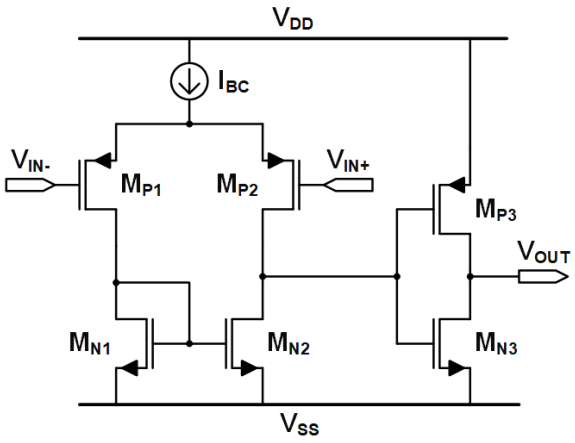


Figure 3.4: The schematic of the comparator.

Table 3.2: The design parameters of the comparator.

Transistor	W [µm]	L [µm]	Device
M_{N1-2}[1:4]	0.5	2.5	nmos3v
M_{P1-2}[1:4]	1	4	pmos3v
M_{N3}	0.4	0.35	nmos3v
M_{P3}	0.4	0.35	pmos3v

W and L are single finger dimensions.

with replica comparators from the previous chapter, the self–compensating chopped comparator architecture allows a simpler comparator topology since it is less sensitive to the offset and delay of the comparators, thus leading to both reduced power and area.

3.2.3 Reference Circuitry

A typical implementation of the relaxation oscillator core with self–compensating chopped comparator (Fig. 3.1) within a self–sustaining clock generator is shown in Fig. 3.5. The core requires a reference voltage V_{REF}, typically generated within a reference generator (VREF GEN). Furthermore, three required currents (shared between the two integrators) may be generated within a voltage to current converter block (V2I), having the value determined by the ratio of the reference voltage V_{REF} and a reference resistance R_{REF}, further replicated within a current mirror block (CMIR). The current mirror block also provides the bias currents for the comparators (not shown in the schematic). In this example, as seen in Fig. 3.5, the current mirror block (Fig. 3.6) is included within the prototype design, having the design parameters listed in Table 3.3. In order to limit its influence on the core performance, the current mirror is designed to provide an adequate matching between the three currents by using cascoded mirrors with a relatively large area of the devices.

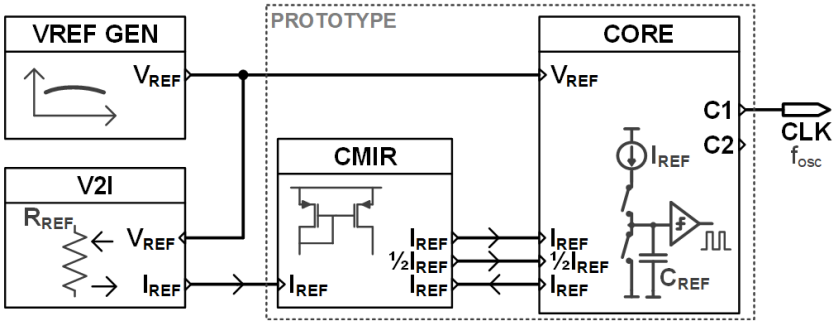


Figure 3.5: The diagram of the reference generation scheme, comprising the reference blocks (reference generator and voltage to current converter) and the current mirror block.

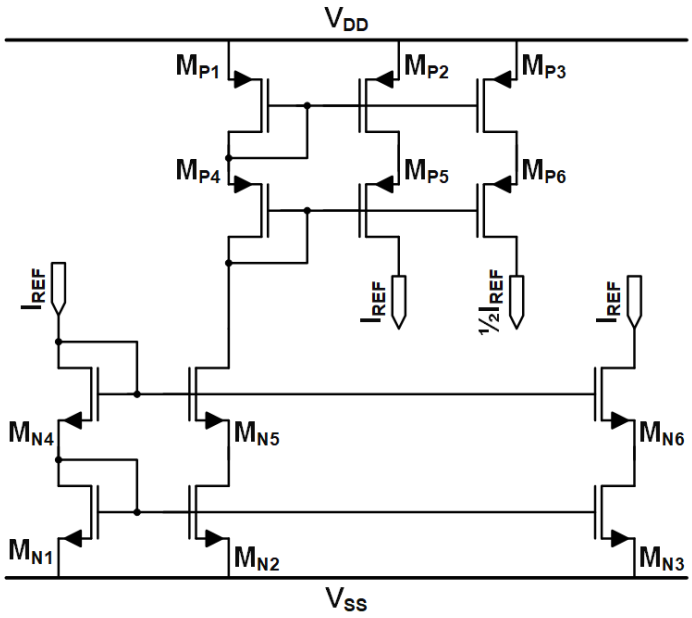


Figure 3.6: The schematic of the current mirror.

Table 3.3: The design parameters of the current mirror.

Transistor	W [µm]	L [µm]	Device
M_{N1-3}[1:4]	7.5	15	nmos3v
M_{N4-6}[1:4]	1	2	nmos3v
M_{P1-2}[1:4]	12.5	10	pmos3v
M_{P3}[1:2]	12.5	10	pmos3v
M_{P4-5}[1:4]	1.5	1	pmos3v
M_{P6}[1:2]	1.5	1	pmos3v

W and L are single finger dimensions.

Furthermore, considering the following:

$$I_{REF} = V_{REF}/R_{REF}, \tag{3.10}$$

the expression for the oscillation period of the proposed core with self–compensating chopped comparator (3.9) becomes equal to

$$T_{osc} = 2R_{REF}C_{REF}. \tag{3.11}$$

The test bench from Fig. 3.7 is assumed for the oscillator core transient simulations presented within the following section. The default value of the supply voltage is $V_{DD} = 3.3$ V, while the values of the externally sourced references are $V_{REF} = 1.2$ V for the reference voltage and $I_{REF} = 10$ µA for the reference current. Also, to offset the systematic first–order temperature coefficient of the reference PIP capacitor, the temperature dependency of the current I_{REF} is set to -40 ppm/°C.

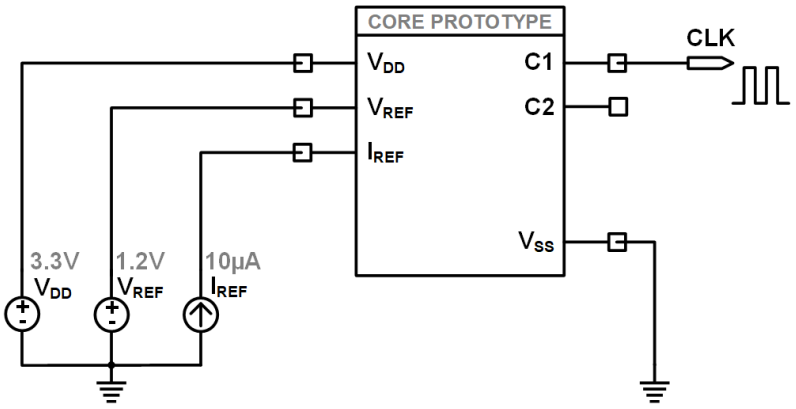


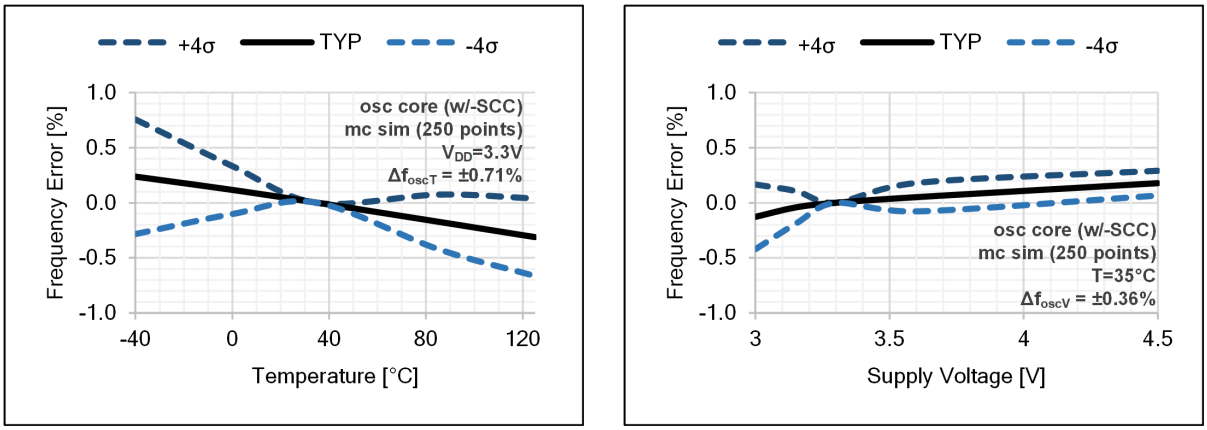
Figure 3.7: The test bench for the transient simulations of the oscillator core with self–compensating chopped comparator.

3.3 Simulation Results

The designed prototype of the oscillator core with self–compensating chopped comparator (w/–SCC) is simulated assuming the test setup described in Section 3.2.3. The oscillator core consumes around $P = 160$ µW ($I_{DD} \approx 48$ µA) at the nominal conditions ($T = 35°C$ and $V_{DD} = 3.3$ V), having an average nominal frequency f_{osc0} of 1 MHz. The core starts with a half–cycle delay (0.5 µs) after the settling of the references.

3.3.1 Temperature and Supply Variation

The simulated frequency variation of the proposed oscillator core with self–compensating chopped comparator versus temperature and supply voltage is shown in Fig. 3.8. The simulations are performed on 250 Monte Carlo points. The simulated frequency drift Δf_{oscT} versus temperature is from -0.67% to $+0.75\%$ in the temperature range from $-40°C$ to $125°C$. The simulated frequency drift Δf_{oscV} versus supply voltage is from -0.42% to $+0.29\%$ in the supply range from 3.0 V to 4.5 V.



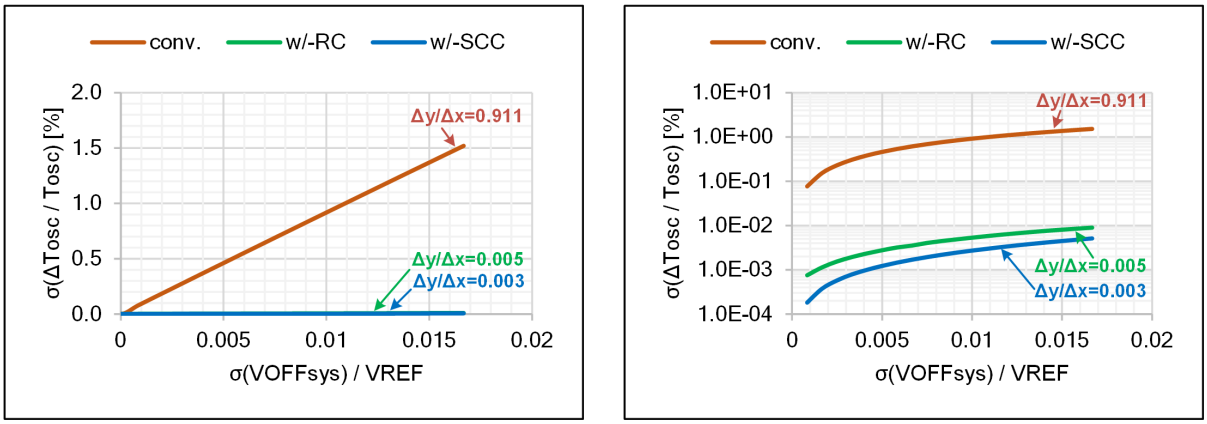
(a) (b)

Figure 3.8: The simulated frequency error of the proposed relaxation oscillator core prototype with self–compensating chopped comparator vs. (a) temperature (at $V_{DD} = 3.3$ V) (b) supply voltage (at $T = 35°C$). The simulations are performed on 250 Monte Carlo points.

3.3.2 Sensitivity to Offset Voltage

Fig. 3.9 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the systematic offset voltage (V_{OFFsys}) for the proposed core with self–compensating chopped comparator (w/–SCC). Here, the identical offset voltage is applied to both core comparators with the standard deviation $\sigma(V_{OFFsys})$ ranging from 0 mV to 20 mV. The figure also includes the results for the two core architectures presented in the previous chapter, namely the conventional oscillator core (conv.) and core with replica comparators (w/–RC). As seen from the figure, the simulated

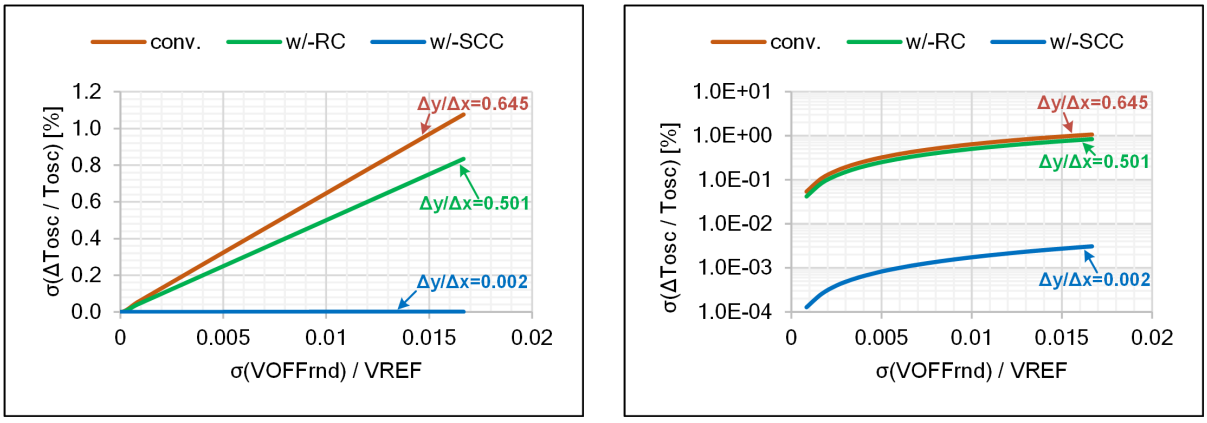
sensitivity for the proposed core (w/–SCC) is $S_{VOFFsys} = 0.003$. Therefore, the frequency is exceptionally stable with respect to the systematic offset voltage of the comparators, similar to the oscillator core with replica comparators (w/–RC), and significantly improved compared to the conventional oscillator core.



(a) (b)

Figure 3.9: The simulated sensitivity of the oscillation period to the systematic offset voltage, shown for three different oscillator cores (conv., w/–RC, and w/–SCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

Fig. 3.10 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the random offset voltage (V_{OFFrnd}) for the proposed core (w/–SCC). Here, the offset voltage of the two comparators is assumed independent, with the standard deviation $\sigma(V_{OFFrnd})$ ranging from 0 mV to 20 mV. The figure also includes the results of the two cores (conv. and w/–RC) presented in the previous chapter. The sensitivity of the proposed architecture (w/–SCC) to the random offset voltage, specifically $S_{VOFFrnd} = 0.002$, is more than two orders of magnitude smaller compared to the two cores presented in the previous chapter (conv. and w/–RC).

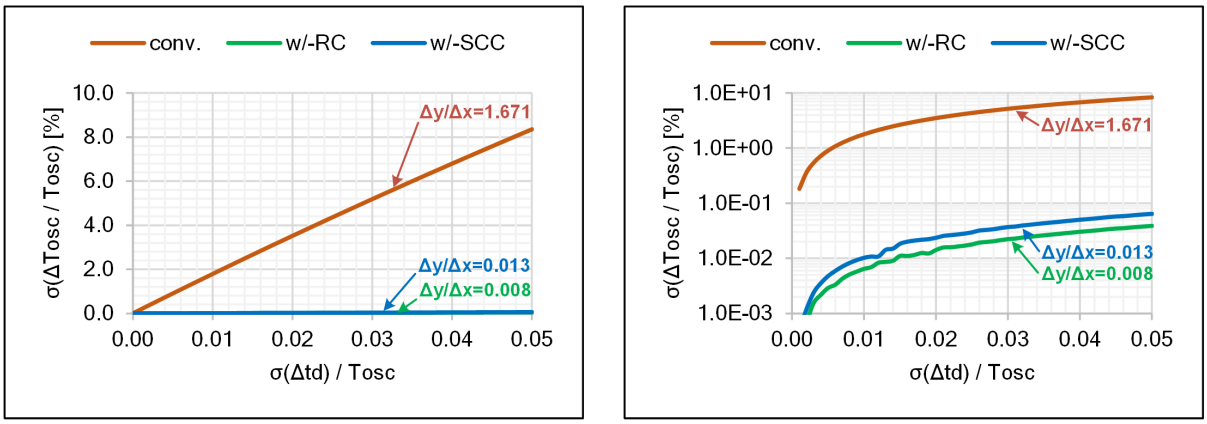


(a) (b)

Figure 3.10: The simulated sensitivity of the oscillation period to the random offset voltage, shown for three different oscillator cores (conv., w/–RC, and w/–SCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

3.3.3 Sensitivity to Propagation Delay

Fig. 3.11 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the propagation delay of the comparator (t_d) for the proposed core with self–compensating chopped comparator (w/–SCC). Here, both comparators are subjected to the same delay variation, with the standard deviation $\sigma(\Delta t_d)$ ranging from 0 ns to 50 ns. The figure also includes the results of the two cores (conv. and w/–RC) presented in the previous chapter. Relatively low sensitivity to the propagation delay is observed for the proposed oscillator core (w/–SCC), specifically $S_{td} = 0.013$. In this sense, the proposed core is comparable to w/–RC core and more than two orders of magnitude better than the conventional core.



(a) (b)

Figure 3.11: The simulated sensitivity of the oscillation period to comparator delay, shown for three different oscillator cores (conv., w/–RC, and w/–SCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

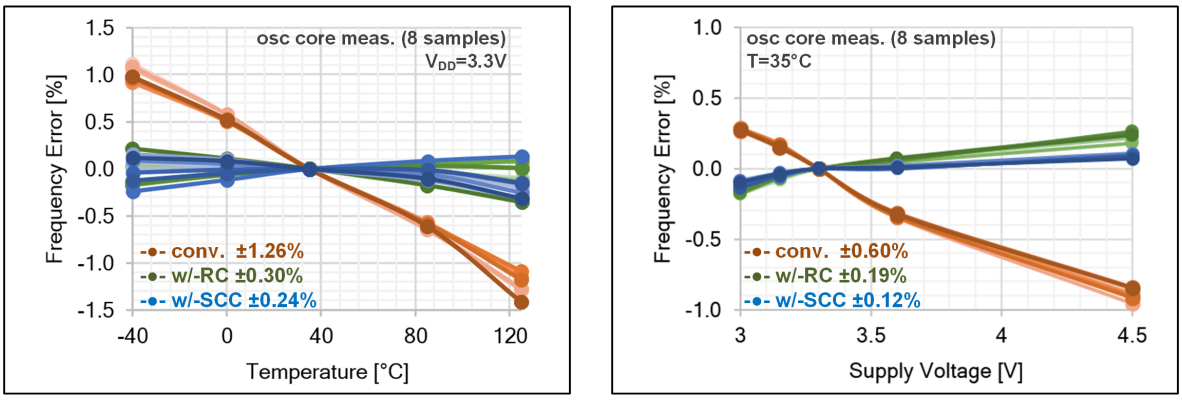
3.4 Measurement Results

The relaxation oscillator prototype with self–compensating chopped comparator (w/–SCC), shown in Fig. 3.3, is manufactured in 0.35–µm CMOS technology with eight samples packaged for measurement. The reference voltage and current (V_{REF} and I_{REF}) are sourced externally, according to Fig. 3.7. The nominal frequency f_{osc0} of the measured samples is around 1 MHz, consuming around $P = 160$ µW ($I_{DD} \approx 48$ µA) under the typical conditions ($T = 35°C$ and $V_{DD} = 3.3$ V). The measured process sensitivity of the pre–calibrated frequency is $\sigma(f_{osc0})/\mu(f_{osc0}) = 0.61\%$.

3.4.1 Temperature and Supply Variation

The measured frequency variation versus temperature is plotted in Fig. 3.12a for the proposed oscillator core (w/–SCC), also showing the comparison with the conventional core (conv.) and core with replica comparators (w/–RC). The measured frequency drift of the proposed core Δf_{oscT} versus temperature is from -0.32% to $+0.16\%$ in the temperature range from $-40°C$ to $125°C$. Therefore, the proposed core (w/–SCC) shows an improvement of around five times compared to the conventional core ($\pm 0.24\%$ vs. $\pm 1.26\%$) and a slight improvement compared to the core with replica comparators ($\pm 0.24\%$ vs. $\pm 0.30\%$).

The measured frequency variation versus supply voltage is plotted in Fig. 3.12b for the proposed oscillator core (w/–SCC), also showing the comparison with the conventional core (conv.) and core with replica comparators (w/–RC). The frequency drift of the proposed core Δf_{oscV} versus supply voltage is from -0.14% to $+0.11\%$ in the supply range from 3.0 V to 4.5 V. Similar to before, the proposed core (w/–SCC) shows an improvement of around five times compared to the conventional core ($\pm 0.12\%$ vs. $\pm 0.6\%$) and a slight improvement compared to the core with replica comparators ($\pm 0.12\%$ vs. $\pm 0.19\%$).

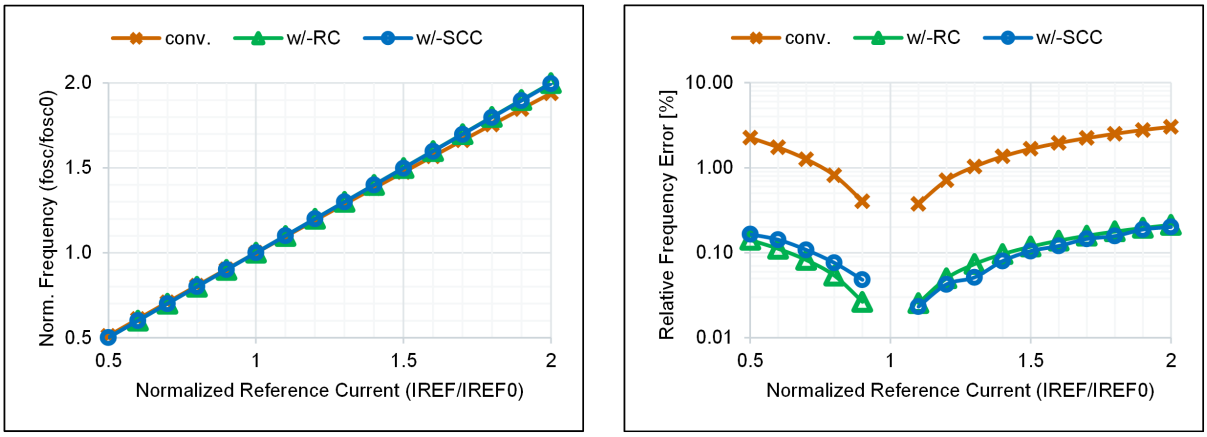


(a) (b)

Figure 3.12: The measured frequency error of three different oscillator cores (conv., w/–RC, and w/–SCC) vs. (a) temperature (at $V_{DD} = 3.3$ V) (b) supply voltage (at $T = 35°C$). The measurements are performed on eight test chip samples.

3.4.2 Control Linearity

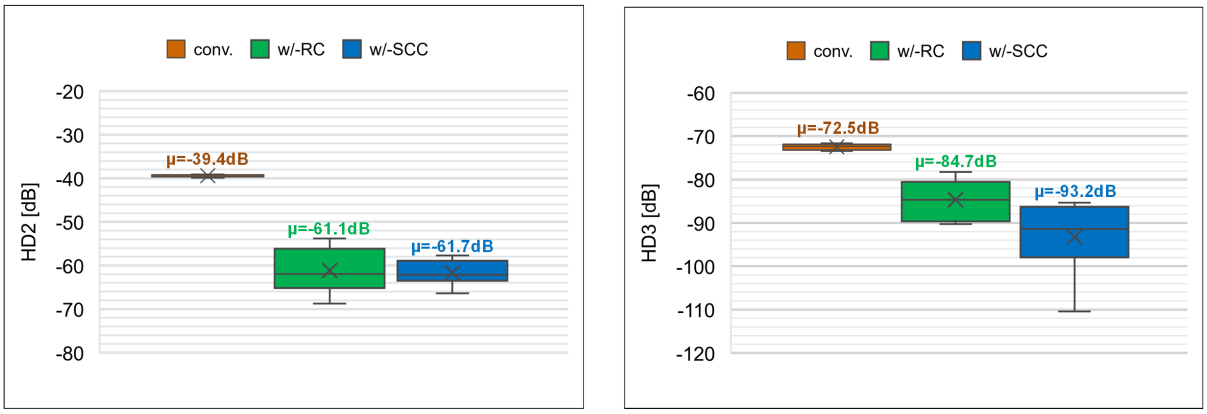
The response of the normalized output frequency f_{osc}/f_{osc0} to the normalized control current I_{REF}/I_{REF0} is measured for the proposed oscillator core (w/–SCC) under the nominal conditions ($T = 35°C$ and $V_{DD} = 3.3$ V) on eight samples. The results of a typical sample are plotted in Fig. 3.13, also showing the comparison with the measurements of the conventional oscillator core (conv.) and core with replica comparators (w/–RC).



(a) (b)

Figure 3.13: (a) The typical normalized frequency response vs. the normalized reference current, shown for three different oscillator cores (conv., w/–RC, and w/–SCC). (b) The relative error of the normalized frequency (compared to the ideal case $y = x$) vs. the normalized reference current.

The distortion parameters HD_2 and HD_3 of the proposed core (w/–SCC) are calculated using (2.24) and (2.25) with $\Delta f_{osc} = 500$ kHz ($\Delta I_{REF}/I_{REF0} = 0.5$), having the mean values equal to $HD_2 = -61.7$ dB and $HD_3 = -93.2$ dB. The results of 8 measured samples are presented in Fig. 3.14, including the two cores (conv. and w/–RC) presented in the previous chapter. As



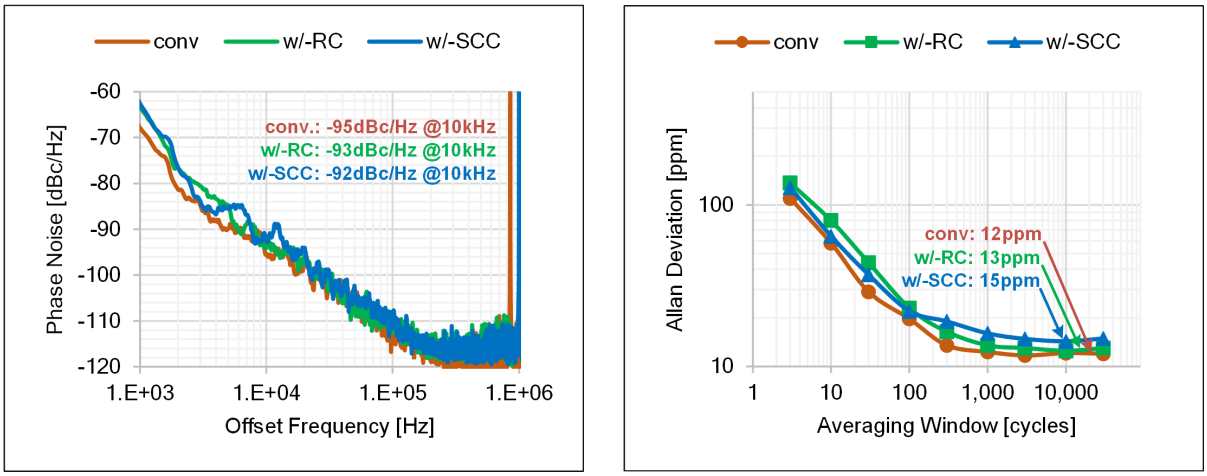
(a) (b)

Figure 3.14: The distortion parameters of the control characteristic, shown for three different oscillator cores (conv., w/–RC, and w/–SCC) (a) HD_2 (b) HD_3. The distortion parameters are calculated for $\Delta f_{osc} = 500$ kHz.

concluded from the presented results, the oscillator core with chopped comparator (w/–SCC) offers further improvement compared to the two previous architectures, especially regarding the HD_3 parameter.

3.4.3 Noise Performance

The noise performance of the proposed relaxation oscillator core (w/–SCC) is evaluated using the phase noise and Allan deviation measurements, shown in Fig. 3.15. The comparison with the conventional core (conv.) and core with replica comparators (w/–RC) is also included in the figure. The measurements are performed under the nominal conditions ($T = 35°C$ and $V_{DD} = 3.3$ V). For the proposed core (w/–SCC), the period jitter equals $\sigma_{Tosc} = 235$ ppm, phase noise at 10 kHz is -92 dBc/Hz, and Allan deviation floor is $\sigma_y = 15$ ppm.



(a) (b)

Figure 3.15: (a) The phase noise measurement of three different oscillator cores (conv., w/–RC, and w/–SCC). (b) The Allan deviation vs. averaging window length for three different oscillator cores (conv., w/–RC, and w/–SCC).

3.5 Summary

In this chapter, the novel relaxation oscillator core architecture employing a self–compensating chopped comparator was introduced. The comparator stage is implemented as a chopped original/replica comparator pair, altering the operation with each half–cycle and actively compensating for the influence of the offset voltage and the propagation delay on the timing. The enhanced performance of the proposed core was demonstrated with the sensitivity analysis, performance simulations, and measurements of the developed prototype. The prototype designed in 0.35–µm CMOS technology has an area of 0.032 mm^2, typically operates at 1 MHz, and consumes around $I_{DD} = 48$ µA. The measured frequency drift is $\pm 0.24\%$ in the temperature range from -40°C to 125°C and $\pm 0.12\%$ in the supply range from 3.0 V to 4.5 V. The design and performance overview of the proposed core prototype is shown in Table 3.4. In conclusion, compared to the conventional relaxation oscillator, the proposed core exhibits significant improvements in frequency drift versus temperature and supply voltage, control linearity, and sensitivity to comparator offset voltage and propagation delay while having minimal impact on the power consumption and area.

Table 3.4: The design and performance summary of the relaxation oscillator core with self–compensating chopped comparator (w/–SCC).

Parameter	Description	Value	Unit	Conditions
	Technology	350	nm	
A	Area	0.032	mm^2	
f_{osc0}	Nominal Frequency	1	MHz	nominal
P	Power	160	µW	nominal
V_{DD}	Supply Voltage	3.3	V	
Δf_{oscT}	[a]Drift vs. Temperature	± 0.71	%	$T = -40 \sim 125$°C
Δf_{oscV}	[a]Drift vs. Supply	± 0.36	%	$V_{DD} = 3.0 \sim 4.5$ V
$t_{startup}$	[a]Start–Up Time	0.5	µs	nominal
σ_{Tosc}	[b]Period Jitter	235	ppm	nominal
HD_2/HD_3	[b]Distortion Parameters	–61.7/–93.2	dB	$\Delta f_{osc} = 500$ kHz
$\mathscr{L}(f)$	[b]Phase Noise	–92	dBc/Hz	$f_m = 10$ kHz
$\sigma_y(\tau)$	[b]Allan Deviation Floor	15	ppm	$\tau = 30$k cycles
$S_{VOFFsys}$	[a]Sensitivity to Syst. Offset Volt.	0.003	$1/V_{REF}$	nominal
$S_{VOFFrnd}$	[a]Sensitivity to Random Offset Volt.	0.002	$1/V_{REF}$	nominal
S_{td}	[a]Sensitivity to Propagation Delay	0.013	$1/T_{osc}$	nominal

[a]Simulated. [b]Measured.

Chapter 4

Relaxation Oscillator Core with Replica Integrator

4.1 Motivation

Detrimental effects due to the non–ideal characteristics of the comparators may become more pronounced at the processes with relatively low voltage, e.g., 1.2 V or less, as may typically be found in CMOS technology nodes at and below approximately 100 nanometers. While the two proposed cores presented in previous chapters (shown in Fig. 2.11 and Fig. 3.1) deal efficiently with comparator non–idealities in standard analog nodes (>130 nm) and under corresponding supply conditions, difficulties appear in low voltage applications or advanced process nodes. Specifically, the integrators within the cores require two–way reference currents that operate poorly under low voltage swings as of reduced transistor overdrive margins. Therefore, it is desirable to modify the oscillator core architecture so that the circuit is suitable for reuse in applications with a relatively low voltage, as demonstrated in [11].

Accordingly, this chapter presents a core architecture [56] that operates under reduced swing conditions while retaining the offset voltage and delay compensation properties. First, an additional integrator unit is introduced that replicates the reference integrating cycles and measures the influence of the comparator. Likewise, a second reference voltage is introduced to the circuit, and the integrating signals are continuously compared with both reference voltages. Also, the influence of the offset voltage of the comparators is entirely negated by chopper implementation. Finally, the core prototype is designed in 110 nm CMOS technology using the core devices that operate under the supply voltage of 1.2 V or less, having the overall frequency accuracy within the 1% range.

4.2 Relaxation Oscillator Core with Replica Integrator

4.2.1 Core Architecture

The schematic of the relaxation oscillator core with replica integrator [56] is presented in Fig. 4.1. The oscillator core consists of three integrator blocks, a chopped comparator block, and a logic block. The first and second integrator blocks, namely the reference integrators, are identical and include two current sources having the reference current I_{REF}, three switches controlled by the output signals of the logic block, and the capacitor having the capacitance value C_{REF}. The third integrator block, namely the replica integrator, includes a current source having the reference current I_{REF}, two switches controlled by the output signals of the logic block, and the capacitor having the capacitance value C_{REF}. The chopped comparator block includes three identical switching blocks and three identical comparators. The operation of

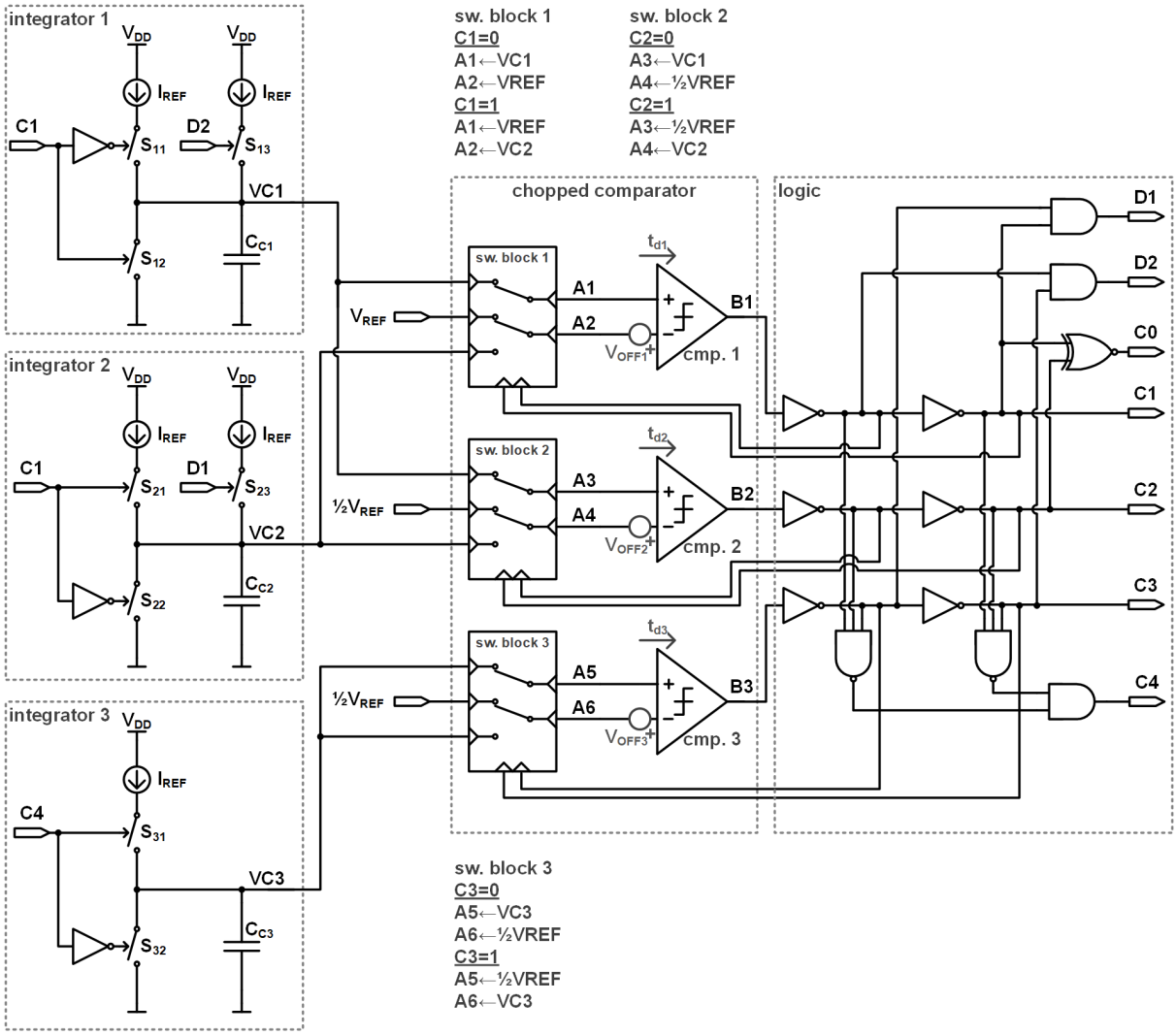


Figure 4.1: The schematic of the relaxation oscillator core with replica integrator, consisting of three integrator blocks, a chopped comparator block, and a logic block.

the switching blocks is described by the signal mappings shown in Fig. 4.1, defining the two states for each chopped comparator depending on the corresponding control signals. Finally, the logic block processes the propagated signals into the control signals, feeding them back to the integrator blocks and chopped comparator block, maintaining the oscillation in this way. The reference current (I_{REF}) and two reference voltages (V_{REF} and $½V_{REF}$) are presumed to be generated within the reference generator, not shown in the schematic.

The operation of the relaxation oscillator core in Fig. 4.1 is described with reference to the corresponding signal waveforms shown in Fig. 4.2. At an initial time ($t = t_0$), it is presumed that all the signals are set to the initial state by a start–up circuit (not shown in the schematic). Initially, the integration occurs within the first integrator in the time interval from t_0 to t_2. The integrating signal $VC1$ rises linearly, having the slope determined by the ratio of the charging current I_{REF} and the capacitor C_{C1}, specifically $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. Due to the initial configuration of the first switching block and the second switching block, while $C1$ and $C2$ are low, the integrating signal $VC1$ is present at the switch outputs $A1$ and $A3$ ($VC1 \mapsto A1 \mapsto A3$). Meanwhile, the second and third integrator blocks remain idle as the integration nodes $VC2$ and $VC3$ are shorted to the ground reference node V_{SS} by the switches S_{22} and S_{32}, respectively. At a subsequent time, $t = t_1$, the integrating signal $VC1$, which is present at the switch output $A3$ ($VC1 \mapsto A3$), becomes equal to the second reference voltage $½V_{REF}$ that is present at the switch output $A4$ ($½V_{REF} \mapsto A4$). Nevertheless, the output of the second comparator $B2$ changes state to high at $t = t_2$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. The timing can be expressed as follows:

$$t_2 = \frac{(½V_{REF} + V_{OFF2})C_{REF}}{I_{REF}} + t_{d2}. \tag{4.1}$$

Following the change of the of the second comparator output $B2$ and the control signal $C2$ from low to high, after $t = t_2$, the second switching block changes state, such that the second reference voltage $½V_{REF}$ is present at the switch output $A3$ ($½V_{REF} \mapsto A3$) and the integrating signal $VC2$ is present at the switch output $A4$ ($VC2 \mapsto A4$). Meanwhile, the integrating signal $VC1$, also present at the switch output $A1$ ($VC1 \mapsto A1$), continues to rise linearly having the same slope as prior to $t = t_2$. Also, at the time $t = t_2$ the control signal $C4$ transitions from low to high, starting the integration within the third integrator block such that the integrating voltage $VC3$, which is present at the switch output $A5$ ($VC3 \mapsto A5$), also rises linearly having the nominal slope $\Delta VC3/\Delta t = I_{REF}/C_{REF}$. Specifically, from the time $t = t_2$ the third integrator block starts replicating the integration cycle of the first integrator block. At a subsequent time, $t = t_3$, the integrating voltage $VC1$ which is present at the switch output $A1$ ($VC1 \mapsto A1$) becomes equal to the reference voltage V_{REF} that is present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the output of the first comparator $B1$ changes state to high at $t = t_4$ due to the non–ideal charac-

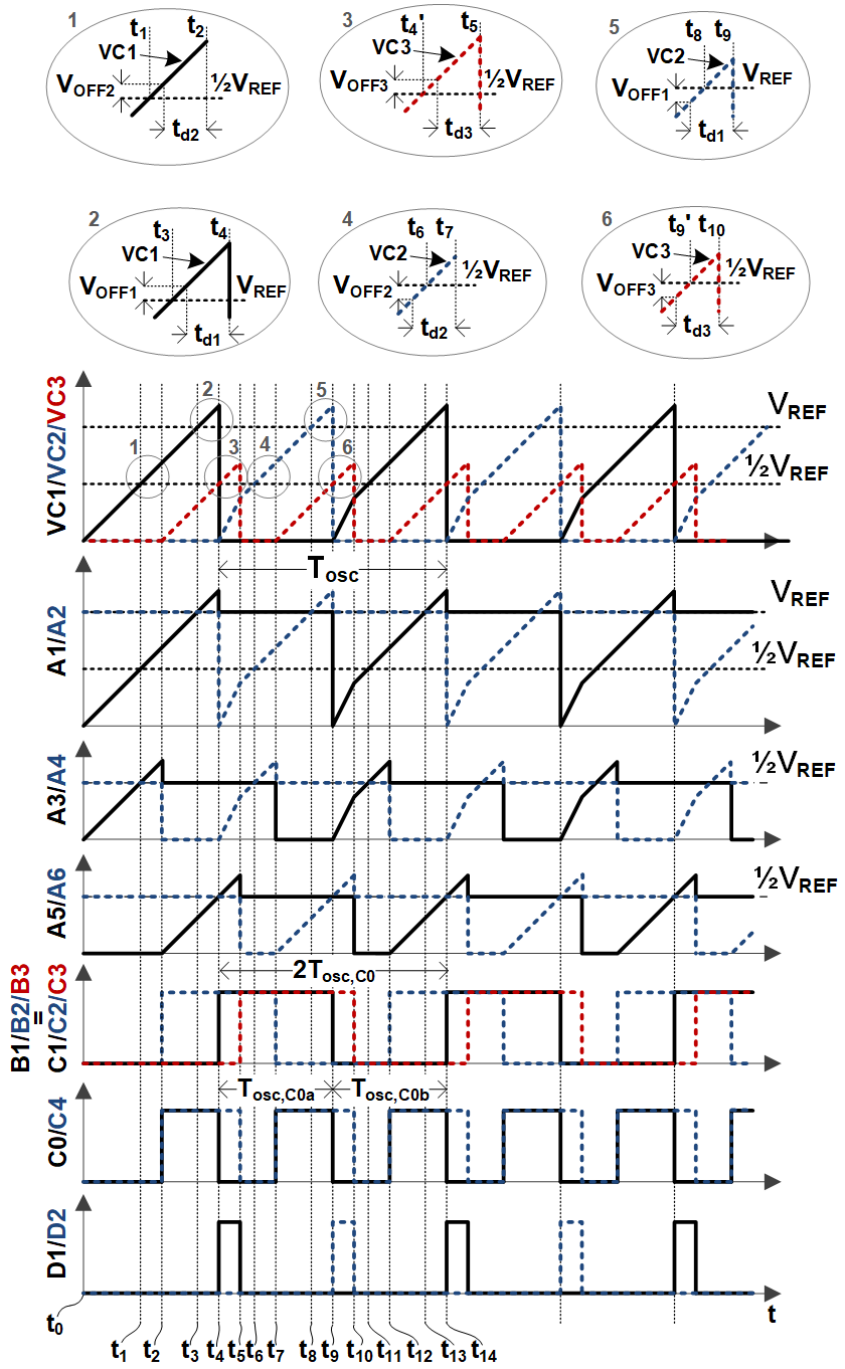


Figure 4.2: The signal waveforms of the relaxation oscillator core with replica integrator.

teristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. Therefore, the following expression is valid:

$$t_4 = \frac{(V_{REF} + V_{OFF1})C_{REF}}{I_{REF}} + t_{d1}. \tag{4.2}$$

Following the change of the comparator output $B1$ and the control signal $C1$ from low to high, the first switching block changes state, meaning the reference voltage V_{REF} is now present at the switch output $A1$ ($V_{REF} \mapsto A1$) and the integrating signal $VC2$ is present at the switch output

$A2$. Consequently, the integration starts within the second integrator block. Due to the state of the first comparator output signal $B1$ and the third comparator output $B3$, the measurement signal $D1$ is set to high, meaning the additional current I_{REF} charges the capacitor within the second integrator block. Therefore, the integrating signal $VC2$ also present as the switch output $A2$ ($VC2 \mapsto A2$) rises linearly having the slope $\Delta VC2/\Delta t = 2I_{REF}/C_{REF}$. Meanwhile, at $t = t_4'$, the integrating signal $VC3$, which is present at the switch output $A5$ ($VC3 \mapsto A5$), becomes equal to the second reference voltage $½V_{REF}$ that is present at the switch output $A6$ ($½V_{REF} \mapsto A6$). Note that the time instance t_4' is same as t_4 in the case where the first comparator, the second comparator and the third comparator are presumed identical. However, the timing of the first, second and third comparator may differ slightly due to variations in properties of the comparators. Due to the offset voltage and the propagation delay of the third comparator (V_{OFF3} and t_{d3}), the third comparator output $B3$ changes state to high at $t = t_5$. Therefore, the following is valid:

$$t_5 - t_2 = \frac{(½V_{REF} + V_{OFF3})C_{REF}}{I_{REF}} + t_{d3}. \tag{4.3}$$

Following the change of the comparator output $B3$ and the control signal $C3$ from low to high, the third switching block changes state, such that the integrating signal $VC3$ is present at the switch output $A6$ ($VC3 \mapsto A6$) and the second reference voltage $½V_{REF}$ is present at the switch output $A5$ ($½V_{REF} \mapsto A5$). Also, the control signal $C4$ transitions from high to low, meaning that the integration node $VC3$ is shorted to the ground and the third integrator block is idle. At this state, the measurement signal $D1$ transitions from high to low, making the duration of the measurement signal pulse t_{D1} equal to:

$$t_{D1} = t_5 - t_4 = -t_{d1} + t_{d2} + t_{d3} + \frac{(-V_{OFF1} + V_{OFF2} + V_{OFF3})C_{REF}}{I_{REF}}. \tag{4.4}$$

The voltage of the integration node $VC2$ at the time $t = t_5$, hereafter denoted $VC2(t_5)$, can be calculated as a function of the slope of the integrating signal $VC2$ ($\Delta VC2/\Delta t = 2I_{REF}/C_{REF}$) and the duration of the measurement signal pulse t_{D1}, and can be represented as follows:

$$VC2(t_5) = \Delta VC2/\Delta t \cdot t_{D1} = \frac{2I_{REF}(-t_{d1} + t_{d2} + t_{d3})}{C_{REF}} + 2(-V_{OFF1} + V_{OFF2} + V_{OFF3}). \tag{4.5}$$

Also, after the time $t = t_5$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), continues to rise linearly having the nominal slope $\Delta VC2/\Delta t = I_{REF}/C_{REF}$. At a subsequent time, $t = t_6$, the integrating signal $VC2$ present at the switch output $A4$ ($VC2 \mapsto A4$) becomes equal to the second reference voltage $½V_{REF}$, which is present at the switch output $A3$ ($½V_{REF} \mapsto A3$). At a subsequent time, $t = t_7$, the second comparator output $B2$ changes state to low due to the non–ideal characteristics of the second comparator, namely the propagation

delay t_{d2} and the offset voltage V_{OFF2}. The timing can be expressed as follows:

$$t_7 - t_5 = \frac{(½V_{REF} - V_{OFF2} - VC2(t_5))C_{REF}}{I_{REF}} + t_{d2}, \tag{4.6}$$

where the offset voltage V_{OFF2} has the opposite contribution compared to the previous half–cycle (4.1), resulting from the switched polarity of the comparator. Following the change of the second comparator output $B2$ and the control signal $C2$ from high to low, after $t = t_7$, the second switching block changes the state, such that the second reference voltage $½V_{REF}$ is present at the switch output $A4$ ($½V_{REF} \mapsto A4$) and the integrating signal $VC1$ is present at the switch output $A3$ ($VC1 \mapsto A3$). Meanwhile, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), continues to rise linearly having the same slope as prior to $t = t_7$. Also, the control signal $C4$ transitions from low to high, starting the integration on the third integrator block, such that the integrating signal $VC3$ present at the switch output $A6$ ($VC3 \mapsto A6$) rises linearly having the nominal slope $\Delta VC3/\Delta t = I_{REF}/C_{REF}$. Specifically, from the time $t = t_7$ the third integrator block starts replicating the integration cycle of the second integrator block. At a subsequent time, $t = t_8$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), becomes equal to the reference voltage V_{REF} that is present at the switch output $A1$ ($V_{REF} \mapsto A1$). As such, the first comparator output $B1$ transitions to low at $t = t_9$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. Therefore, the following expression is valid:

$$t_9 - t_5 = \frac{(V_{REF} - V_{OFF1} - VC2(t_5))C_{REF}}{I_{REF}} + t_{d1}, \tag{4.7}$$

where the offset voltage V_{OFF1} has the opposite contribution compared to the previous half–cycle (4.2), resulting from the switched polarity of the comparator. Following the transition of the first comparator output $B1$ and the control signal $C1$ from high to low, the first switching block changes state, such that the reference voltage V_{REF} is present at the switch output $A2$ ($V_{REF} \mapsto A2$) and the integrating signal $VC1$ is present at the switch output $A1$ ($VC1 \mapsto A1$). Consequently, the integration starts within the first integrator. As a result of the state of the first comparator output $B1$ and the third comparator output $B3$, the measurement signal $D2$ is set to high, meaning the additional current I_{REF} charges the capacitor within the first integrator block. Therefore, the integrating signal $VC1$ present at the switch output $A1$ ($VC1 \mapsto A1$) rises linearly having the slope $\Delta VC1/\Delta t = 2I_{REF}/C_{REF}$. Meanwhile, at the time $t = t_9'$, the integrating signal $VC3$, which is present at the switch output $A6$ ($VC3 \mapsto A6$), becomes equal to the second reference voltage $½V_{REF}$ present at the switch output $A5$ ($½V_{REF} \mapsto A5$). Again, note that the time t_9' is same as t_9 in case all comparators are presumed identical, but may slightly differ in practice due to the variations in the properties of the comparators. Resulting from the offset voltage and propagation delay of the third comparator (t_{d3} and V_{OFF3}), the third comparator

output $B3$ changes state to low at the time $t = t_{10}$. Therefore, the following is valid:

$$t_{10} - t_7 = \frac{(½V_{REF} - V_{OFF3})C_{REF}}{I_{REF}} + t_{d3}, \tag{4.8}$$

where the offset voltage V_{OFF3} has the opposite contribution compared to the previous half–cycle (4.3), resulting from the switched polarity of the comparator. Following the transition of the third comparator output $B3$ and the control signal $C3$ from high to low, the third switching block changes the state. Therefore, the integrating signal $VC3$ is present at the switch output $A5$ ($VC3 \mapsto A5$) and the second reference voltage $½V_{REF}$ is present at the switch output $A6$ ($½V_{REF} \mapsto A6$). Also, the fourth input clock signal $C4$ transitions from high to low, meaning the third integration node $VC3$ is shorted to the ground and the third integrator is idle. With this, the measurement signal $D2$ transitions from high to low, making the duration of the measurement signal pulse t_{D2} equal to:

$$t_{D2} = t_{10} - t_9 = -t_{d1} + t_{d2} + t_{d3} + \frac{(V_{OFF1} - V_{OFF2} - V_{OFF3})C_{REF}}{I_{REF}}. \tag{4.9}$$

The voltage of the integration node $VC1$ at the time $t = t_{10}$, hereafter denoted $VC1(t_{10})$, can be calculated as a function of the slope of the integrating signal $VC1$ ($\Delta VC1/\Delta t = 2I_{REF}/C_{REF}$) and the duration of the measurement signal pulse t_{D2}, and can be represented as follows:

$$VC1(t_{10}) = \Delta VC1/\Delta t \cdot t_{D2} = \frac{2I_{REF}(-t_{d1} + t_{d2} + t_{d3})}{C_{REF}} + 2(V_{OFF1} - V_{OFF2} - V_{OFF3}). \tag{4.10}$$

Also, after the time $t = t_{10}$, the integrating signal $VC1$ present at the switch output $A1$ ($VC1 \mapsto A1$) continues to rise linearly having the nominal slope $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. At a subsequent time, $t = t_{13}$, the integrating signal $VC1$ present at the switch output $A1$ ($VC1 \mapsto A1$) becomes equal to the reference voltage V_{REF} present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the first comparator output $B1$ transitions from low to high at $t = t_{14}$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. Therefore, the following expression is valid:

$$t_{14} - t_{10} = \frac{(V_{REF} + V_{OFF1} - VC1(t_{10}))C_{REF}}{I_{REF}} + t_{d1}. \tag{4.11}$$

With this, a complete oscillation cycle is described from t_4 to t_{14}. The duration of the oscillation period can be calculated by adding the time segments as follows:

$$T_{osc} = (t_5 - t_4) + (t_9 - t_5) + (t_{10} - t_9) + (t_{14} - t_{10}), \tag{4.12}$$

resulting in

$$T_{osc} = \frac{2V_{REF}C_{REF}}{I_{REF}} + 4t_{d1} - 2t_{d2} - 2t_{d3}. \tag{4.13}$$

Accordingly, the stability of the oscillation period is dependent on the stability of the references (V_{REF}, I_{REF}, C_{REF}) since the contribution of the comparator offset voltage is completely negated. Furthermore, the difference between the propagation delays of the three comparators, as demonstrated in Section 2.3.2, is expected to remain relatively small ($t_{d1} \approx t_{d2} \approx t_{d3}$) if appropriate matching techniques are applied. Also, other minor effects neglected within this analysis may influence the frequency stability, including the delay of the logic gates, switching non–idealities, parasitics, and mismatch between the integrator blocks.

Additionally, the auxiliary clock signal $C0$ has the average frequency twice as high compared to the other signals usable as clock reference ($C1$, $C2$, and $C3$), having the average period of

$$T_{osc,C0} = \frac{V_{REF}C_{REF}}{I_{REF}} + 2t_{d1} - t_{d2} - t_{d3}. \tag{4.14}$$

where the duration of the odd cycle is

$$T_{osc,C0a} = \frac{(V_{REF} - V_{OFF2} - V_{OFF3})C_{REF}}{I_{REF}} + 2t_{d1} - t_{d2} - t_{d3} \tag{4.15}$$

and the duration of the even cycle is

$$T_{osc,C0b} = \frac{(V_{REF} + V_{OFF2} + V_{OFF3})C_{REF}}{I_{REF}} + 2t_{d1} - t_{d2} - t_{d3}. \tag{4.16}$$

Note that the auxiliary clock signal $C0$ has a relatively big discrepancy between the two consecutive cycles, determined by the mismatch of the integrator–comparator units, namely

$$\frac{\Delta T_{osc,C0}}{T_{osc,C0}} = \frac{T_{osc,C0b} - T_{osc,C0a}}{T_{osc0}} \approx \frac{2(V_{OFF2} + V_{OFF3})}{V_{REF}}. \tag{4.17}$$

As such, while not usable in applications that require low cycle–to–cycle jitter, using the clock signal $C0$ as a clock source in other types of applications where only long term jitter is relevant (e.g. timekeeping) would result in 2 times improvement of energy efficiency.

4.2.2 Core Prototype

The 2–MHz prototype of the relaxation oscillator core with replica integrator from Fig. 4.1 is designed in 110 nm CMOS technology. The prototype layout is shown in Fig. 4.3, having a total area of 255 µm × 175 µm (0.045 mm^2).

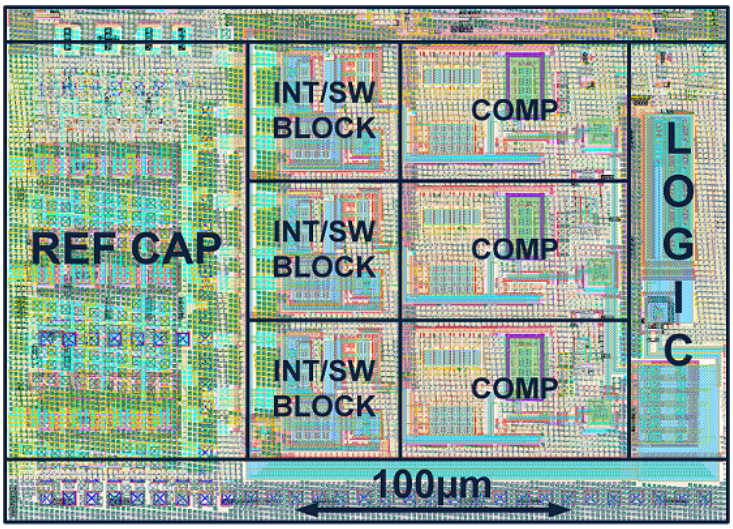


Figure 4.3: The layout of the oscillator core with replica integrator (w/–RI) designed in 110 nm CMOS technology. The overall size is 255 µm × 175 µm.

The design parameters of the core prototype are shown in Table 4.1. The switches within the three integrator blocks, denoted as S_{int} (S_{11-13}, S_{21-23}, S_{31-32}), are identical and implemented with a single nMOS transistor. On the other hand, the switches within the three switching blocks, denoted as S_{chop}, are implemented as CMOS analog switches with identically sized nMOS and pMOS transistors. The three reference capacitors C_{C1-3} are metal–insulator–metal type (MIM). The schematic of the three comparators used in the core is shown in Fig. 4.4, comprising a symmetrical OTA (M_{P1-4} and M_{N1-4}) and two inverter buffers (M_{N5-6} and M_{P5-6}). The comparator's design parameters are listed in Table 4.2.

Table 4.1: The design parameters of the relaxation oscillator core prototype with replica integrator.

Switch	W [µm]	L [µm]		Device
S_{int}	2	0.55		nmos1v
S_{chop}	2	0.8		nmos1v+pmos1v
Capacitor	**W [µm]**	**L [µm]**	**Cap [pF]**	**Device**
C_{C1-3}[1:12]	10.5	10.5	1.65	cmim

W and L are single finger dimensions.
Cap is overall capacitance.

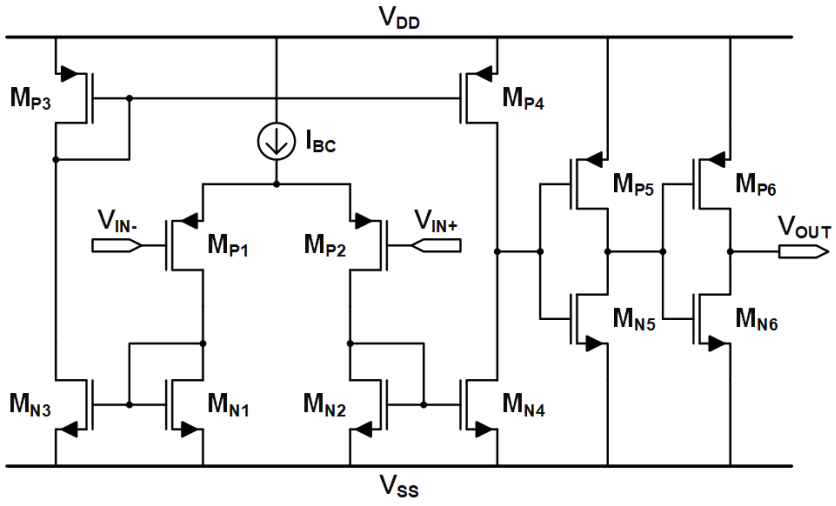


Figure 4.4: The schematic of the comparator.

Table 4.2: The design parameters of the comparator.

Transistor	W [µm]	L [µm]	Device
M_{N1-2}[1:2]	2	1	nmos1v
M_{N3-4}[1:4]	2	1	nmos1v
M_{P1-2}[1:2]	3.6	1	pmos1v
M_{P3-4}[1:4]	2	1	pmos1v
M_{N5-6}	0.55	0.55	nmos1v
M_{P5-6}	0.55	0.55	pmos1v

W and L are single finger dimensions.

4.2.3 Reference Circuitry

A typical implementation of the relaxation oscillator core with replica integrator (Fig. 4.1) within a self–sustaining clock generator is shown in Fig. 4.5. The core requires two reference voltages, V_{REF} and $½V_{REF}$, typically generated within the reference generator (VREF GEN).

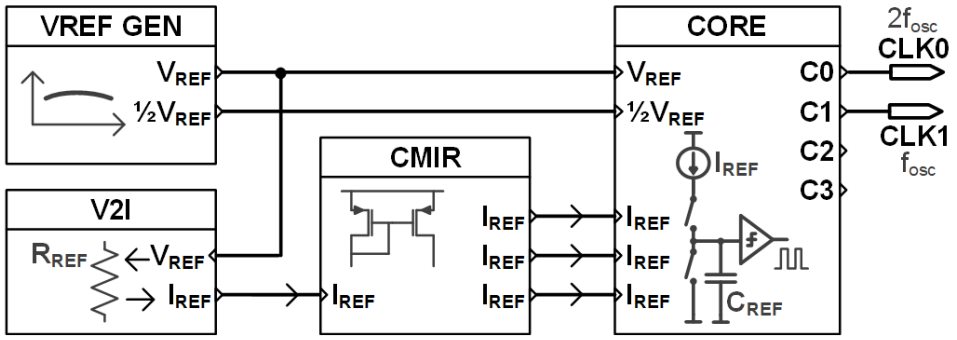


Figure 4.5: The diagram of a self–sustaining clock generator implementation with proposed relaxation oscillator core and reference circuitry (reference voltage generator, V2I, and current mirror).

Furthermore, three required reference currents I_{REF} may be generated within a voltage to current converter block (V2I), having the value determined by the ratio of the reference voltage V_{REF} and reference resistance R_{REF}, further replicated within a current mirror block (CMIR). Note that the core requires only three instances of mirrored current I_{REF} since the two input currents from the first and second integrator block can be shared as they are active during mutually exclusive time segments. The current mirror block also supplies the bias currents for the comparators (not shown in the schematic). Furthermore, considering

$$I_{REF} = V_{REF}/R_{REF}, \tag{4.18}$$

the expression for the oscillation period of the proposed core with replica integrator (4.13) becomes approximately equal to

$$T_{osc} \approx 2R_{REF}C_{REF}. \tag{4.19}$$

The test bench from Fig. 4.6 is assumed for the oscillator core transient simulations presented within the following section. The default value of the supply voltage is $V_{DD} = 1.2$ V, while the values of the externally sourced references are $V_{REF} = 0.3$ V, $½V_{REF} = 0.15$ V, and $I_{REF} = 2$ µA. Also, to offset the systematic first–order temperature coefficient of the reference MIM capacitor, the temperature dependency of the current I_{REF} is set to $+17.5$ ppm/°C.

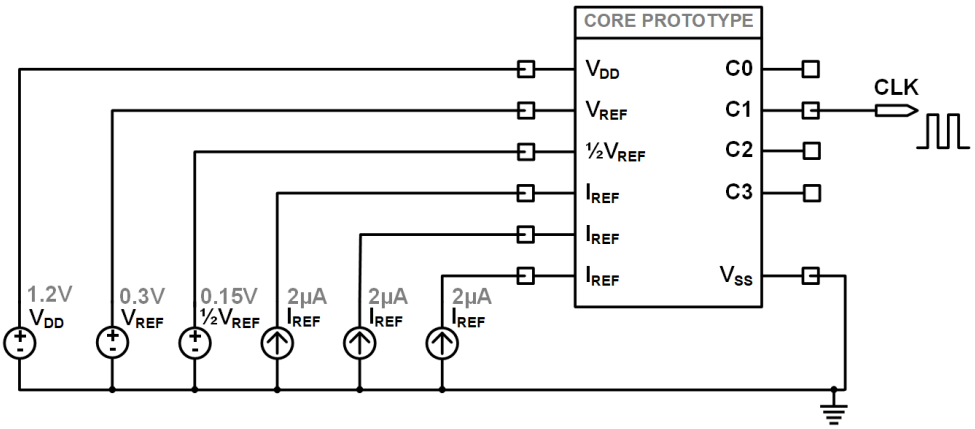


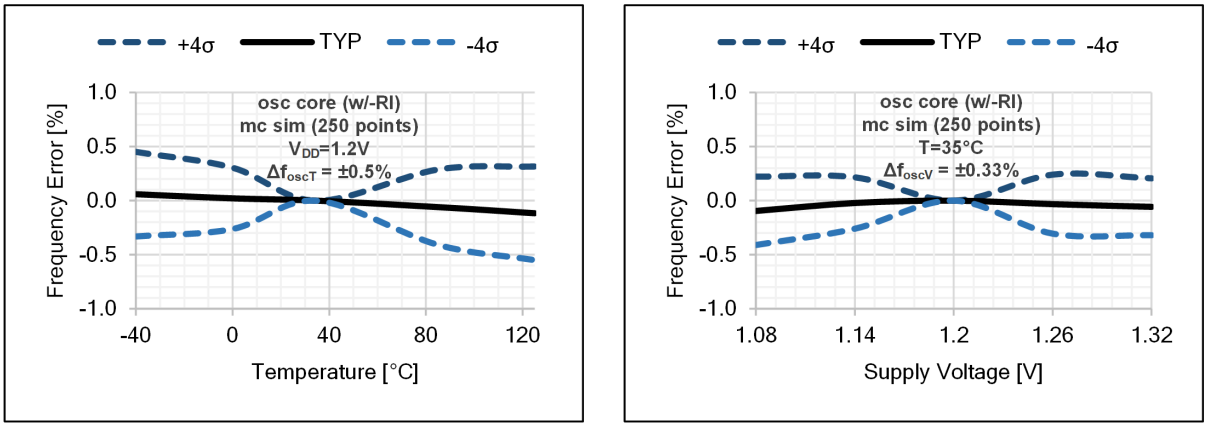
Figure 4.6: The test bench for the transient simulation of the oscillator core with replica integrator.

4.3 Simulation Results

The designed prototype of the oscillator core with replica integrator (w/–RI) is simulated assuming the test bench from Fig. 4.6. The oscillator core consumes $P = 39.6$ µW ($I_{DD} \approx 33$ µA) at the nominal conditions ($T = 35°$C and $V_{DD} = 1.2$ V). The nominal frequency is $f_{osc0} = 2$ MHz (4 MHz in $2\times$ frequency mode), having the process sensitivity of $\sigma(f_{osc0})/\mu(f_{osc0}) = 0.6\%$. The typical period jitter is around $\sigma_{Tosc} = 550$ ps (1100 ppm). The core starts with a half–cycle delay (0.25 µs) after the settling of the references.

4.3.1 Temperature and Supply Variation

The simulated frequency variation of the proposed oscillator core with replica integrator versus temperature and supply voltage is shown in Fig. 4.7. The simulations are performed on 250 Monte Carlo points. The simulated frequency drift Δf_{oscT} versus temperature is from -0.55% to $+0.45\%$ in the temperature range from $-40°$C to 125°C. The simulated frequency drift Δf_{oscV} versus supply voltage is from -0.41% to $+0.24\%$ in the supply range from 1.08 V to 1.32 V.



(a) (b)

Figure 4.7: The simulated frequency error of the proposed relaxation oscillator core prototype with replica integrator vs. (a) temperature (at $V_{DD} = 1.2$ V) (b) supply voltage (at $T = 35°$C). The simulations are performed on 250 Monte Carlo points.

4.3.2 Sensitivity to Offset Voltage

Fig. 4.8 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the systematic offset voltage (V_{OFFsys}) for the proposed core with replica integrator (w/–RI). Here, the identical offset voltage of the three core comparators is assumed, with the standard deviation $\sigma(V_{OFFsys})$ ranging from 0 mV to 5 mV. The figure also includes the results for the three core architectures presented in previous chapters, namely the conventional oscillator core (conv.), core with replica

comparators (w/–RC), and core with self–compensating chopped comparator (w/–SCC). The simulated sensitivity to the systematic offset voltage for the proposed core (w/–RI), specifically $S_{VOFFsys} = 0.018$, is nearly two orders of magnitude smaller compared to the conventional core, while being slightly inferior w/–RC and w/–SCC cores.

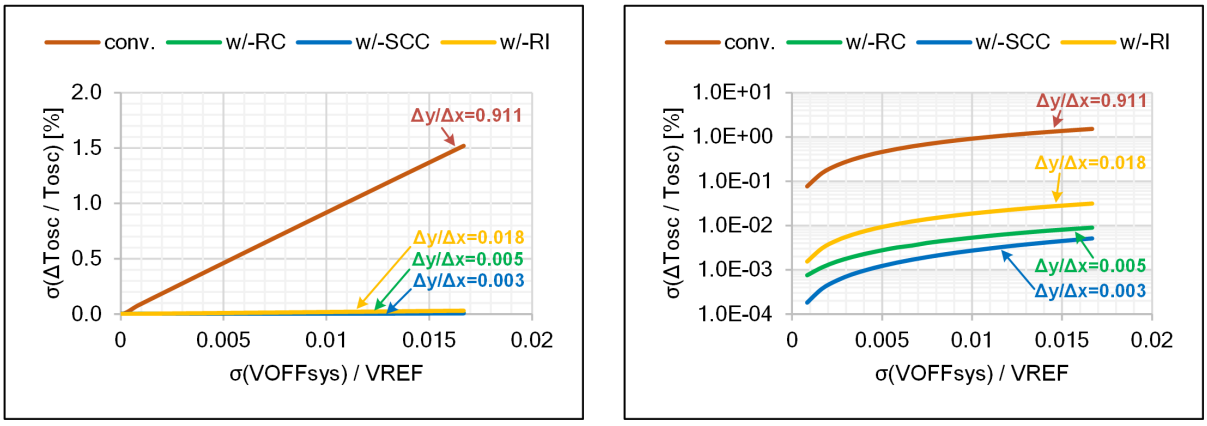


Figure 4.8: The simulated sensitivity of the oscillation period to the systematic offset voltage, shown for four different oscillator cores (conv., w/–RC, w/–SCC, and w/–RI) (a) plotted in linear scale (b) plotted in logarithmic scale.

Fig. 4.9 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the random offset voltage (V_{OFFrnd}) for the proposed core with replica integrator (w/–RI). Here, the offset voltage of the three core comparators is assumed independent, with the standard deviation $\sigma(V_{OFFrnd})$ ranging from 0 mV to 5 mV. The figure also includes the results of the three cores (conv., w/–RC, and w/–SCC) presented in previous chapters. The simulated sensitivity for the proposed core (w/–RI) is $S_{VOFFrnd} = 0.05$, being around one order of magnitude better than the conventional oscillator core and oscillator core with replica comparators (w/–RC).

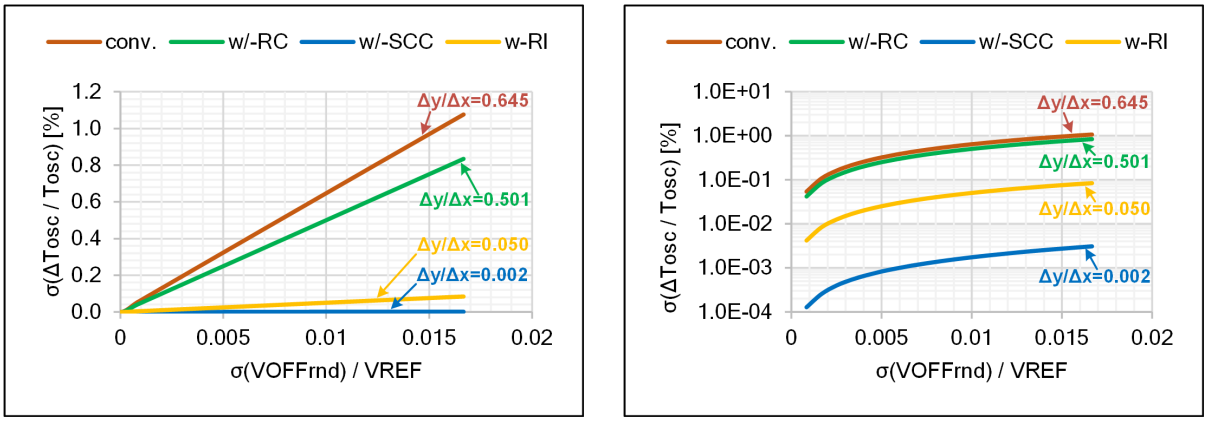
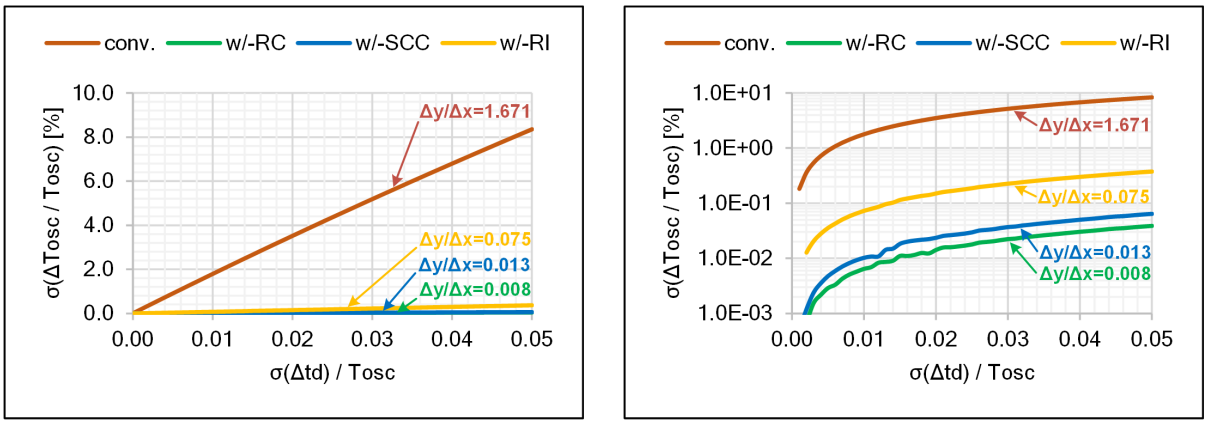


Figure 4.9: The simulated sensitivity of the oscillation period to the random offset voltage, shown for four different oscillator cores (conv., w/–RC, w/–SCC, and w/–RI) (a) plotted in linear scale (b) plotted in logarithmic scale.

4.3.3 Sensitivity to Propagation Delay

Fig. 4.10 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the propagation delay of the comparator (t_d) for the proposed core with replica integrator (w/–RI). Here, the identical variation of the propagation delay is assumed for three core comparators, with the standard deviation $\sigma(\Delta t_d)$ ranging from 0 ns to 25 ns. The figure also includes the results of the three cores (conv., w/–RC, and w/–SCC) presented in previous chapters. For the proposed oscillator core (w/–RI), the simulated sensitivity $S_{td} = 0.075$ indicates more than ten times improvement compared to the conventional core. At the same time, the proposed core is inferior to the oscillator core with replica comparators (w/–RC) and self–compensating chopped comparator (w/–SCC).



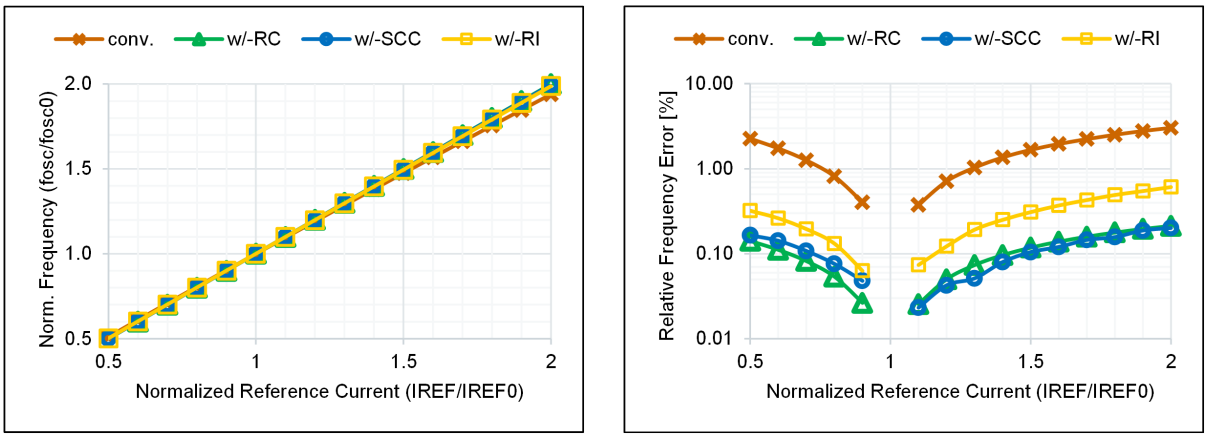
(a) (b)

Figure 4.10: The simulated sensitivity of the oscillation period to the comparator delay, shown for four different oscillator cores (conv., w/–RC, w/–SCC, and w/–RI) (a) plotted in linear scale (b) plotted in logarithmic scale.

4.3.4 Control Linearity

The response of the normalized output frequency f_{osc}/f_{osc0} to the normalized control current I_{REF}/I_{REF0} is simulated for the proposed oscillator core (w/–RI) under the nominal conditions ($T = 35°$C and $V_{DD} = 1.2$ V) on 50 Monte Carlo points. The results for the typical case are plotted in Fig. 4.11, also showing the comparison with the measurements of the conventional oscillator core (conv.), core with replica comparators (w/–RC), and core with self–compensating chopped comparator (w/–SCC).

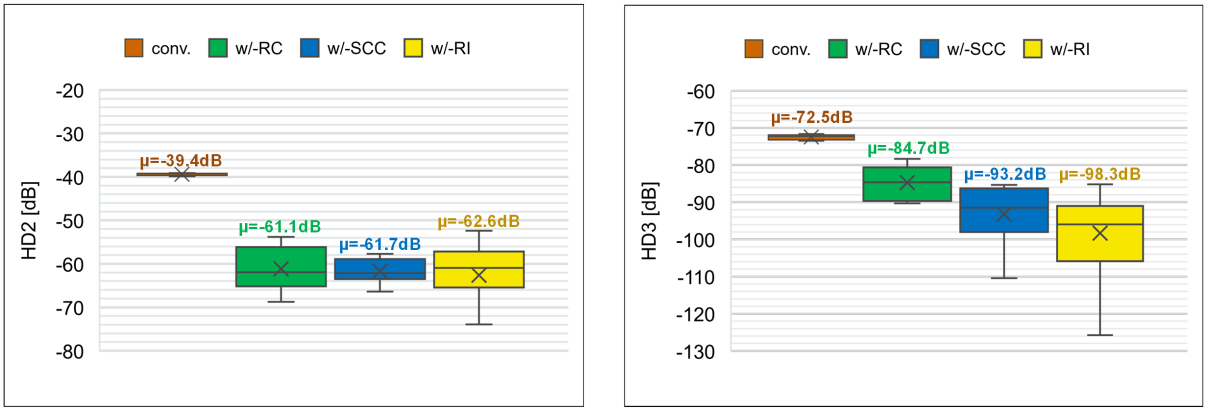
The distortion parameters HD_2 and HD_3 of the proposed core (w/–RI) are calculated using (2.24) and (2.25) with $\Delta f_{osc} = 500$ kHz ($\Delta I_{REF}/I_{REF0} = 0.25$), having the mean values equal to $HD_2 = -62.6$ dB and $HD_3 = -98.3$ dB. The results of 50 simulated samples are presented in Fig. 4.12, including the three cores (conv., w/–RC, and w/–SCC) presented in previous chapters. As concluded from the presented results, the oscillator core with replica integrators (w/–RI)



(a) (b)

Figure 4.11: (a) The typical normalized frequency response vs. the normalized reference current, shown for four different oscillator cores (conv., w/–RC, w/–SCC, and w/–RI). (b) The relative error of the normalized frequency (compared to the ideal case $y = x$) vs. the normalized reference current.

shows comparable performance to w/–RC and w/–SCC architectures in terms of HD_2, at the same time offering a further improvement in terms of HD_3.



(a) (b)

Figure 4.12: The distortion parameters of the control characteristic, shown for four different oscillator cores (conv., w/–RC, w/–SCC, and w/–RI) (a) HD_2 (b) HD_3. The distortion parameters are calculated for $\Delta f_{osc} = 500$ kHz.

4.4 Summary

In this chapter, a novel relaxation oscillator core architecture suitable for low voltage operation was presented. The introduction of a replica integrator and double comparison of the referent integrating cycle enables the compensation of the comparator stage influence on the timing. The core also provides the output clock having a double frequency compared to the core native frequency, significantly improving the power efficiency at the expense of increased cycle–to–cycle jitter. The core prototype designed in 110 nm technology has an area of 0.045 mm^2, typically operates at 2 MHz, and consumes around $I_{DD} = 33$ µA. The simulated frequency drift is $\pm 0.5\%$ in the temperature range from -40°C to 125°C and $\pm 0.33\%$ in the supply range from 1.08 V to 1.32 V. The design and performance summary of the core prototype is shown in Table 4.3. Since the architecture is compatible with low reference voltage values, specifically around 300 mV or smaller, the device may be fabricated in an advanced CMOS technology node configured to operate with a relatively low voltage supply, e.g., 1.2 V, 1.0 V, 0.8 V or even less.

Table 4.3: The design and performance summary of the relaxation oscillator core with replica integrator (w/–RI) – simulation results.

Parameter	Description	Value	Unit	Conditions
	Technology	110	nm	
A	Area	0.045	mm^2	
f_{osc0}	Nominal Frequency	2	MHz	nominal
P	Power	39.6	µW	nominal
V_{DD}	Supply Voltage	1.2	V	
Δf_{oscT}	Drift vs. Temperature	± 0.5	%	$T = -40 \sim 125$°C
Δf_{oscV}	Drift vs. Supply	± 0.33	%	$V_{DD} = 1.08 \sim 1.32$ V
$t_{startup}$	Start–Up Time	0.25	µs	nominal
σ_{Tosc}	Period Jitter	1100	ppm	nominal
HD_2/HD_3	Distortion Parameters	–62.6/–98.3	dB	$\Delta f_{osc} = 500$ kHz
$S_{VOFFsys}$	Sensitivity to Syst. Offset Volt.	0.018	$1/V_{REF}$	nominal
$S_{VOFFrnd}$	Sensitivity to Random Offset Volt.	0.050	$1/V_{REF}$	nominal
S_{td}	Sensitivity to Propagation Delay	0.075	$1/T_{osc}$	nominal

Chapter 5

Relaxation Oscillator Post–Manufacturing Process and Temperature Calibration

5.1 Motivation

While the relaxation oscillator cores presented in previous chapters considerably improve the frequency stability compared to the conventional oscillator core, the systems sensitive to clock accuracy would benefit from further performance improvement. While the line sensitivity may be easily eliminated with a voltage regulator [25–27], sample–to–sample temperature calibration is required in the post–production phase to improve the temperature accuracy beyond a specific limit, especially in high–volume production. In [24], the output frequency of a relaxation oscillator is digitally compensated over the temperature, where the higher–order temperature coefficients are extracted by an on–chip heater. Likewise, in [25–28], the oscillator's temperature dependency is calibrated with measurements at several different temperatures, including very low temperatures ($-35°$C to $-40°$C). Although achieving remarkable accuracy (around $\pm 0.1\%$ or less), both approaches introduce significant cost overhead and are not appropriate for low–cost SoCs.

An alternative method for the post–manufacturing process and temperature calibration is proposed within this chapter, requiring frequency measurement at two arbitrary temperatures. Here, the assumed second–order temperature characteristic of an oscillator [27] can be estimated without measurements below the room temperature, therefore limiting the cost increase related to the second measurement point. Furthermore, a standalone relaxation oscillator is designed and manufactured in 180 nm CMOS technology, comprising a novel oscillator core architecture that combines low complexity with good standalone performance [57]. Finally, the proposed temperature calibration method is demonstrated on the test–case oscillator with simulations and measurements on eight samples.

5.2 Oscillator Architecture

The block diagram of the proposed self–sustaining relaxation oscillator is shown in Fig. 5.1, consisting of a voltage reference generator (VREF GEN), voltage–to–current converter (V2I), current mirror (CMIR), and oscillator core. The start–up circuitry and clock buffer are not shown in the schematic. The oscillator receives the 8–bit frequency trim word FQT[7:0] and the 4–bit temperature coefficient trim word TCT[3:0]. Also, the enable signal EN and the supply and ground voltages V_{DD} and V_{SS} are provided to each block (not shown in the diagram). The output clock is provided at the CLK terminal.

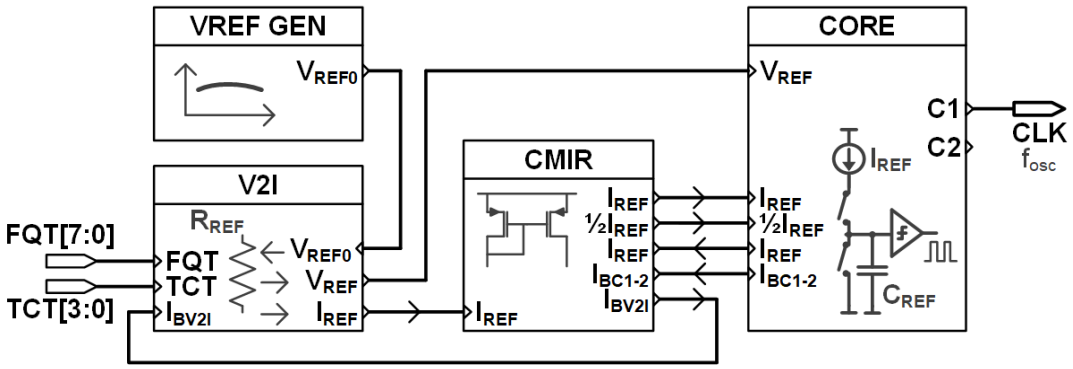


Figure 5.1: The block diagram of the relaxation oscillator, comprising the voltage reference generator (VREF GEN), voltage to current converter (V2I), current mirror (CMIR), and oscillator core.

The clock generator operates as follows. The reference generator supplies the reference voltage V_{REF0} for the voltage–to–current converter. The voltage–to–current converter scales the reference voltage V_{REF0} to the core reference voltage V_{REF} and generates the reference current I_{REF}. Nominally, the ratio of the reference voltage and current is determined by the reference resistance R_{REF} within the V2I block, specifically

$$R_{REF} = \frac{V_{REF}}{I_{REF}}. \tag{5.1}$$

Additionally, the core reference current I_{REF} is trimmable within the V2I converter with 8–bit accuracy (using FQT[7:0]) to correct for the process variation effects on the nominal output frequency f_{osc0}. In the post–trimmed case, R_{REF} represents the effective value of the reference resistance (i.e., the ratio of the reference voltage and the trimmed reference current) rather than a physical value. In addition, the reference resistor has a tunable first–order temperature coefficient $TC1_R$ with 4–bit accuracy (using TCT[3:0]), which is used to compensate for the temperature dependency of the output frequency. Furthermore, the current mirror block receives the reference current I_{REF} as an input and provides: three core reference currents (two instances of I_{REF} and a single instance of half the reference current $½I_{REF}$), comparator bias currents (I_{BC1-2}), and the bias current for the voltage–to–current converter (I_{BV2I}). Finally, the oscillator

core generates the clock having the oscillation period

$$T_{osc} = \frac{2V_{REF}C_{REF}}{I_{REF}} + t_c, \tag{5.2}$$

where C_{REF} is the value of the reference capacitance, and t_c is the influence of the comparator stage and other non–idealities within the oscillator core. Considering (5.1) and (5.2), the clock frequency f_{osc} is determined by the reference resistance R_{REF} and the reference capacitance C_{REF}, together with the timing influence of the oscillator core (t_c), specifically

$$\frac{1}{f_{osc}} = T_{osc} = 2R_{REF}C_{REF} + t_c. \tag{5.3}$$

Taking into account the offset and delay cancellation property of the oscillator core, as will be demonstrated in the continuation, the timing influence of the oscillator core is expected to be negligible ($t_c \approx 0$), therefore approximating the oscillation period with

$$T_{osc} \approx 2R_{REF}C_{REF}, \tag{5.4}$$

or in terms of frequency:

$$f_{osc} \approx \frac{1}{2R_{REF}C_{REF}} = \frac{I_{REF}}{2V_{REF}C_{REF}}. \tag{5.5}$$

5.2.1 Voltage Reference Generator

The schematic of the voltage reference generator (VREF GEN) is shown in Fig. 5.2, with the design parameters listed in Table 5.1. The reference generator includes the PTAT current generator (M_{N1-2}, M_{P1-2}, R_1), the CTAT current generator (M_{N3-5}, M_{P3-4}, R_2), and the output branch (M_{P5-6}, R_3) where the PTAT and CTAT currents are combined, generating the reference voltage V_{REF0} over the resistor R_3. The capacitor C_1 is included to reduce the noise influence. The start–up circuit is not shown in the schematic.

Assuming the weak inversion of the transistors M_{N1-2}, the PTAT current I_{PTAT} can be expressed as [13, 64]

$$I_{PTAT} = \frac{nV_T}{R_1} ln\left(\frac{W_{N1}}{W_{N2}}\right), \tag{5.6}$$

while the CTAT current I_{CTAT} can be written as

$$I_{CTAT} = \frac{V_{GS,N5}}{R_2}, \tag{5.7}$$

where W is the width of the corresponding transistor, n is the subthreshold slope factor, V_T is the thermal voltage ($V_T = kT/q$), and $V_{GS,N5}$ is the gate–source voltage of the transistor M_{N5}.

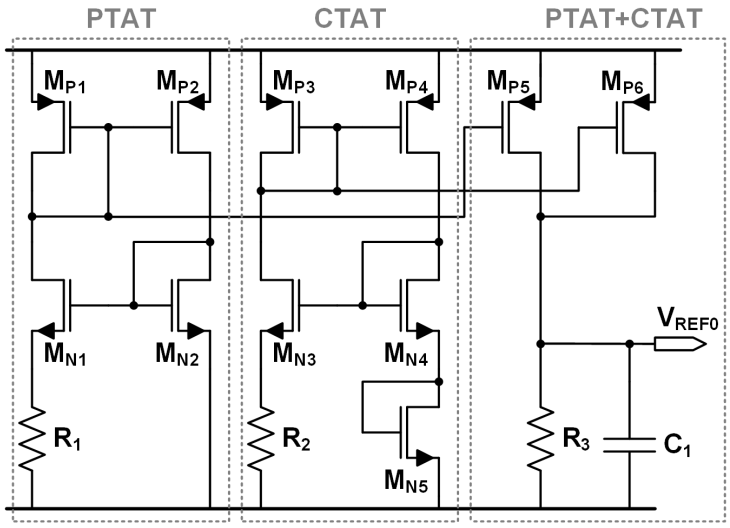


Figure 5.2: The schematic of the voltage reference generator (VREF GEN), comprising the PTAT current generator, CTAT current generator, and the output branch (PTAT+CTAT).

Table 5.1: The design parameters of the voltage reference generator block.

Transistor	W [µm]	L [µm]	I_D [µA]	Device
M_{N1}[1:20]	4	1.8	2.6	nmos2v
M_{N2-5}[1:4]	4	1.8	2.6	nmos2v
M_{P1-4}[1:8]	0.36	4	2.6	pmos2v
M_{P5}[1:5]	0.36	4	1.63	pmos2v
M_{P6}[1:3]	0.36	4	0.97	pmos2v
Resistor	**W [µm]**	**L [µm]**	**Res [kΩ]**	**Device**
R_1	0.75	50	22.7	rpoly
R_2	0.75	350	158	rpoly
R_3	0.75	280	127	rpoly
Capacitor	**W [µm]**	**L [µm]**	**Cap [pF]**	**Device**
C_1[1:10]	10	12	2.52	cmim

W and L are single finger dimensions.
I_D is overall device current.
Cap is overall capacitance.

Consequently, the output reference voltage V_{REF0} can be expressed as

$$V_{REF0} = \frac{W_{P5}}{W_{P1}} I_{PTAT} R_3 + \frac{W_{P6}}{W_{P3}} I_{CTAT} R_3, \tag{5.8}$$

where the nominal value and temperature coefficient of the reference voltage V_{REF0} can be set arbitrarily during the design phase using the independent PTAT and CTAT currents.

5.2.2 Voltage to Current Converter

The schematic of the voltage–to–current converter (V2I) is shown in Fig. 5.3, with the design parameters listed in Table 5.2. The block consists of a first amplifier stage (M_{N1-4}, M_{P1-4}), the second amplifier stage (M_{P5-6}, R_{REF}), the Miller compensation (C_M, R_M), the current DAC (M_{P7-8}), and the cascode bias (M_{N5-6}, M_{P9-11}).

The voltage–to–current converter receives the reference voltage V_{REF0} and scales it to the core reference voltage V_{REF}

$$V_{REF} = \frac{3}{2} V_{REF0}, \tag{5.9}$$

due to the feedback factor of $2/3$ implemented with the reference resistor. The reference resistor R_{REF} also defines the ratio between the reference voltage V_{REF} and the reference current I_{REF0}:

$$R_{REF} = \frac{V_{REF}}{I_{REF0}}. \tag{5.10}$$

Furthermore, the 8–bit current DAC receives the reference current I_{REF0} and generates the trimmed reference current I_{REF}. In order to improve the linearity and guarantee the monotonicity of the DAC, transistor M_{P7} is divided into 4 binary–weighted segments controlled by FQT[3:0] and 15 thermometer segments weighted with 16 LSB values and controlled by FQT[7:4]. Also, having a single LSB segment always on, the effective width of the transistor M_{P7} can be weighted from 1 to 256 LSB values, depending on the applied frequency trim code FQT. Moreover, considering that the width of the transistor M_{P5} is always weighted with 128 LSB values, the relation between the trimmed and untrimmed reference current (I_{REF} and I_{REF0}) is

$$I_{REF}(FQT) = I_{REF0} \cdot \frac{FQT + 129}{128}, \tag{5.11}$$

where FQT is the signed integer equivalent of the 8–bit FQT[7:0] configuration word in 2's complement format.

Considering (5.11) and the linear dependency of the oscillation frequency f_{osc} on the reference current I_{REF} (5.5), the relation between the output frequency and the frequency trim code FQT is defined as

$$f_{osc}(FQT) = f_{osc}(FQT = 0) \cdot \frac{FQT + 129}{129}. \tag{5.12}$$

This allows the correction of the process variations and trimming the nominal frequency value to the desired frequency, as commonly done in relaxation oscillators [41]. Here, the frequency trim code FQT has the nominal value $FQT = 0$ and the allowed range from $FQT = -128$ to $FQT = +127$.

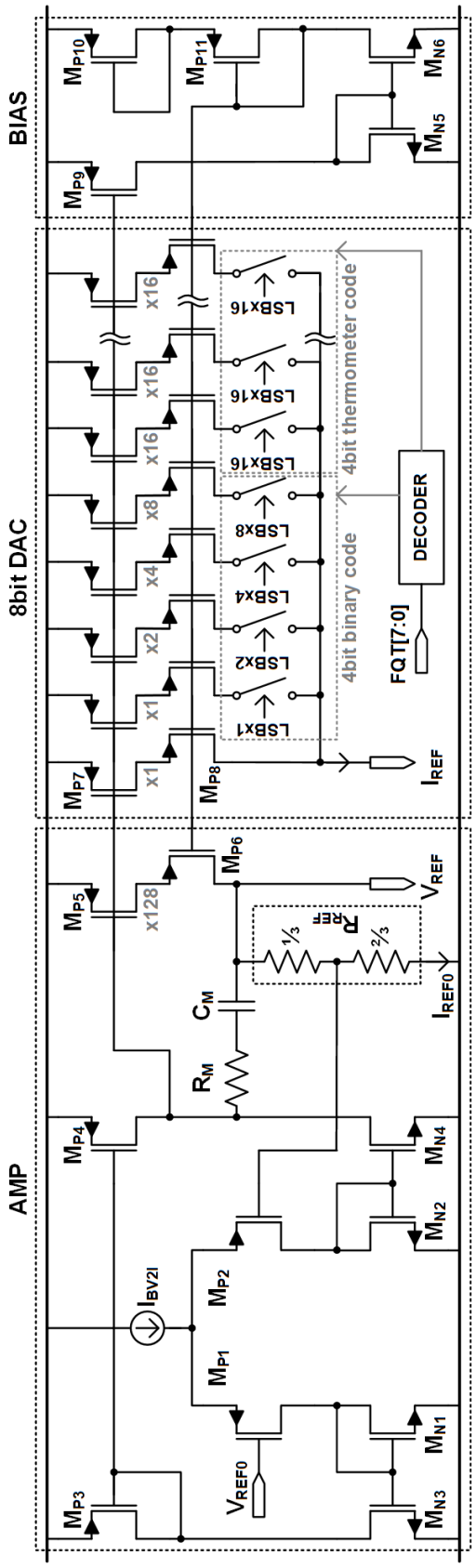


Figure 5.3: The schematic of the voltage to current converter, comprising the two–stage amplifier with the Miller compensation, the 8–bit DAC, and the cascode bias circuit.

Table 5.2: The design parameters of the voltage–to–current converter.

Transistor	W [µm]	L [µm]	I_D [µA]	Device
M_{N1-2}[1:2]	1.08	2.7	1.25	nmos2v
M_{N3-4}[1:4]	1.08	2.7	2.5	nmos2v
M_{N5-6}[1:8]	0.36	7.2	1.25	nmos2v
M_{P1-2}[1:2]	1.8	2.4	1.25	pmos2v
M_{P3-4}[1:4]	1.44	2.4	2.5	pmos2v
M_{P5}[1:128]	0.24	5.4	5	pmos2v
M_{P6}[1:128]	0.24	1.8	5	pmos2v
M_{P7}[1:256]	0.24	5.4	0.039∼10	pmos2v
M_{P8}[1:256]	0.24	1.8	0.039∼10	pmos2v
M_{P9-10}[1:32]	0.24	5.4	1.25	pmos2v
M_{P11}[1:32]	0.24	1.8	1.25	pmos2v
Resistor	W [µm]	L [µm]	Res [kΩ]	Device
R_{REF}	–	–	98.6	rpoly+rdiff
R_M	0.5	35	26.9	rpoly
Capacitor	W [µm]	L [µm]	Cap [pF]	Device
C_M[1:9]	10	10	1.89	cmim

W and L are single finger dimensions.
I_D is overall device current.
Cap is overall capacitance.

5.2.3 Reference Resistor

The schematic of the reference resistor (RREF) is shown in Fig 5.4, with the design parameters listed in Table 5.3. The resistor is implemented as a composite resistor consisting of two different resistor types [39, 51]: the polysilicon resistor having a negative first–order temperature coefficient and the diffusion resistor having a positive first–order temperature coefficient.

Considering the expression for the oscillation period (5.3), the overall first–order temperature coefficient of the clock reference $TC1_T$ can be compensated using a composite resistor with a tunable first–order temperature coefficient, as described in the continuation. Specifically, differentiating the oscillation period T_{osc} (5.3) with respect to temperature T leads to

$$\frac{\partial T_{osc}}{\partial T} = 2R_{REF}\frac{\partial C_{REF}}{\partial T} + 2C_{REF}\frac{\partial R_{REF}}{\partial T} + \frac{\partial t_c}{\partial T}. \tag{5.13}$$

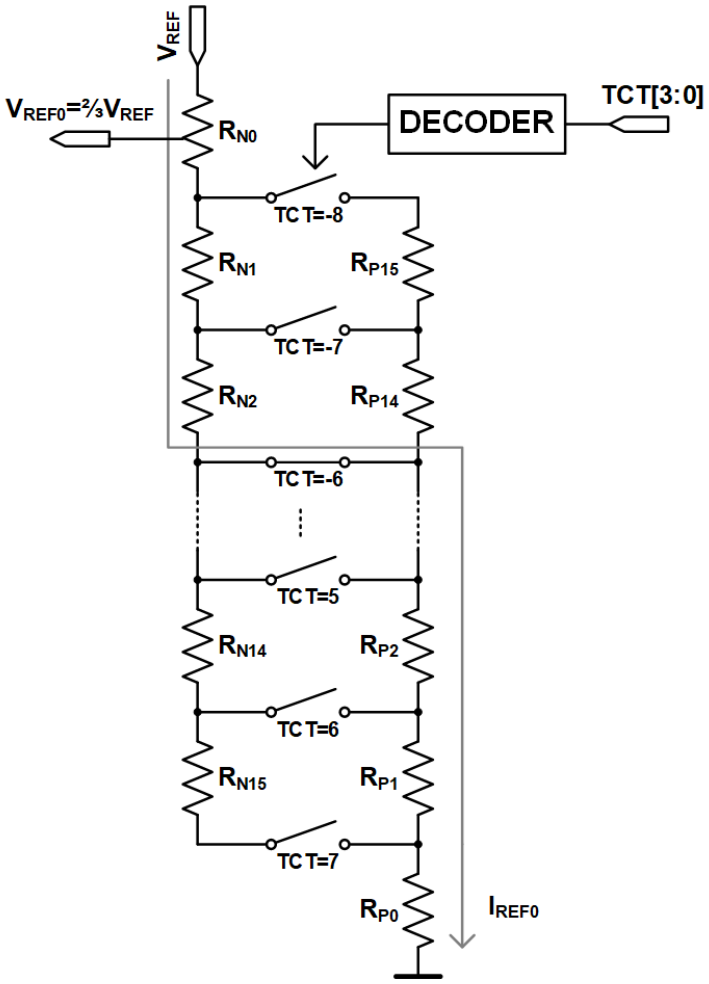


Figure 5.4: The schematic of the reference resistor with a tunable first–order temperature coefficient. The resistor is comprised of two different resistor types: the polysilicon resistor (R_{Ni}) and the p–diffusion resistor (R_{Pi}), having negative and positive temperature coefficients, respectively.

Table 5.3: The design parameters of the reference resistor.

Resistor	W [µm]	L [µm]	Res [kΩ]	Device
R_{N0}	0.86	129.8	62.54	rpoly
R_{N1-15}	0.86	2.2	1.06	rpoly
R_{P0}	1	143	20.14	rdiff
R_{P1-15}	1	7.5	1.06	rdiff
Resistor	$TC1$ [ppm/°C]	$TC2$ [ppb/°C^2]	**Res [Ω]**	**Device**
R_N	–565	629	337/□	rpoly
R_P	1330	854	133/□	rdiff
R_{REF}	–40	683	98.6	rpoly+rdiff

Furthermore, considering (5.4), (5.13) can also be expressed as

$$\frac{1}{T_{osc}} \cdot \frac{\partial T_{osc}}{\partial T} = \frac{1}{C_{REF}} \cdot \frac{\partial C_{REF}}{\partial T} + \frac{1}{R_{REF}} \cdot \frac{\partial R_{REF}}{\partial T} + \frac{1}{T_{osc}} \cdot \frac{\partial t_c}{dT}. \tag{5.14}$$

Also, defining the first–order temperature coefficients as

$$TC1_T = \frac{1}{T_{osc}} \cdot \frac{\partial T_{osc}}{\partial T}\bigg|_{T=T_0}, \tag{5.15}$$

$$TC1_R = \frac{1}{R_{REF}} \cdot \frac{\partial R_{REF}}{\partial T}\bigg|_{T=T_0}, \tag{5.16}$$

$$TC1_C = \frac{1}{C_{REF}} \cdot \frac{\partial C_{REF}}{\partial T}\bigg|_{T=T_0}, \tag{5.17}$$

$$TC1_{tc} = \frac{1}{T_{osc}} \cdot \frac{\partial t_c}{\partial T}\bigg|_{T=T_0}, \tag{5.18}$$

where T_0 is the nominal temperature, the overall first–order temperature coefficient $TC1_T$ of the clock period T_{osc} can be expressed as the sum of the first–order temperature coefficients of the reference resistor $TC1_R$, reference capacitor $TC1_C$, and oscillator core $TC1_{tc}$:

$$TC1_T = TC1_R + TC1_C + TC1_{tc}, \tag{5.19}$$

or, for the output frequency temperature coefficient

$$TC1_f = -TC1_T = -TC1_R - TC1_C - TC1_{tc}. \tag{5.20}$$

Accordingly, the overall first–order temperature coefficient $TC1_f$ can be compensated post-manufacturing ($TC1_f \approx 0$) by adjusting the reference resistance temperature coefficient $TC1_R$ to the optimal value ($TC1_R^*$), specifically

$$TC1_R^* = -TC1_C - TC1_{tc}. \tag{5.21}$$

Similarly, the second–order temperature coefficient $TC2_f$ of the output frequency can be written as

$$TC2_f \approx -TC2_T \approx -TC2_R - TC2_C - TC2_{tc}, \tag{5.22}$$

where

$$TC2_R = \frac{1}{2R_{REF}} \cdot \frac{\partial^2 R_{REF}}{\partial T^2}\bigg|_{T=T_0}, \tag{5.23}$$

$$TC2_C = \frac{1}{2C_{REF}} \cdot \frac{\partial^2 C_{REF}}{\partial T^2}\bigg|_{T=T_0}, \tag{5.24}$$

and

$$TC2_{tc} = \frac{1}{2T_{osc}} \cdot \frac{\partial^2 t_c}{\partial T^2}\bigg|_{T=T_0}. \tag{5.25}$$

Unlike $TC1_f$, the second–order output frequency temperature coefficient $TC2_f$ can not be compensated with the composite resistor since both used resistor types have positive $TC2$, as shown in Table 5.3. Also, in (5.22), $TC2_f$ is primarily determined by the reference resistor's second–order temperature coefficient $TC2_R$ since the second–order temperature coefficients of the reference capacitor $TC2_C$ and the oscillator core $TC2_{tc}$ are expected to have a limited influence.

The reference resistor with a tunable first–order temperature coefficient $TC1_R$ is implemented as follows. Both resistor types are organized in 16 segments (polysilicon resistors: R_{N0-15}; diffusion resistors: R_{P0-15}) and coupled in the switch–ladder arrangement shown in Fig. 5.4. Here, only one lateral switch is in the "on" state at the time, controlled by the temperature coefficient trim code TCT. Therefore, changing the trim code TCT adjusts the ratio of the resistors with positive and negative temperature coefficient, which in turn adjusts the overall temperature coefficient $TC1_R$ of the reference resistor. In order to keep the value of the overall nominal resistance R_{REF0} constant and maintain a constant temperature coefficient tuning step versus the trim code TCT, the ladder segments must have the same nominal resistance R_S:

$$R_{N1-15}(T_0) = R_{P1-15}(T_0) = R_S. \tag{5.26}$$

On the other hand, the resistors R_{N0} and R_{P0} may have any nominal resistance.

Since the reference resistor consists of the two resistor arrays having the opposite first–order temperature coefficient, the expression for the overall resistance R_{REF} can be expressed as the sum of the R_N array and the R_P array, specifically

$$R_{REF}(T) = R_N(T) + R_P(T). \tag{5.27}$$

Here, the overall resistance of each array, namely $R_N(T)$ and $R_P(T)$, depends on the state of the switch ladder controlled by the trim factor of the temperature coefficient trim code TCT. In particular, their nominal resistance values (at $T = T_0$) can be expressed as

$$R_N(T_0) = \sum_{i=0}^{i=8+TCT} R_{Ni}(T_0) = R_{N0}(T_0) + R_S(8 + TCT), \tag{5.28}$$

$$R_P(T_0) = \sum_{i=0}^{i=7-TCT} R_{Pi}(T_0) = R_{P0}(T_0) + R_S(7 - TCT), \tag{5.29}$$

where TCT is the signed integer value of the TCT[3:0] configuration word in 2's complement notation, having the range from $TCT = -8$ to $+7$ with $TCT = 0$ being the nominal value. Considering the first–order temperature coefficients of the two resistor types, specifically $TC1_N$ for the negative temperature coefficient resistor and $TC1_P$ for the positive temperature coefficient

resistor, the resistance of the ladder segments versus temperature delta ($\Delta T = T - T_0$) is

$$R_{Ni}(T) = R_{Ni}(T_0) \cdot (1 + TC1_N \cdot \Delta T), \tag{5.30}$$

$$R_{Pi}(T) = R_{Pi}(T_0) \cdot (1 + TC1_P \cdot \Delta T), \tag{5.31}$$

which, in conjunction with (5.28) and (5.29), results in

$$R_N(T) = \Big[R_{N0}(T_0) + R_S(8 + TCT)\Big](1 + TC1_N \cdot \Delta T), \tag{5.32}$$

and

$$R_P(T) = \Big[R_{P0}(T_0) + R_S(7 - TCT)\Big](1 + TC1_P \cdot \Delta T). \tag{5.33}$$

Taking into account (5.26)–(5.33), the final expression for the reference resistance R_{REF} is

$$R_{REF}(T) = R_{REF0}\Big[1 + (TC1_{R0} + TCT \cdot \delta TC1_R)\Delta T\Big], \tag{5.34}$$

where R_{REF0} is the nominal resistance value (at $T = T_0$),

$$R_{REF0} = R_{N0}(T_0) + R_{P0}(T_0) + 15R_S, \tag{5.35}$$

$TC1_{R0}$ is the nominal first–order temperature coefficient of the reference resistor (at $TCT = 0$),

$$TC1_{R0} = TC1_N \frac{R_{N0}(T_0) + 8R_S}{R_{REF0}} + TC1_P \frac{R_{P0}(T_0) + 7R_S}{R_{REF0}}, \tag{5.36}$$

and $\delta TC1_R$ is the tuning step of the resistor's first–order temperature coefficient ($TC1_R$),

$$\delta TC1_R = -\frac{R_S}{R_{REF0}}(TC1_P - TC1_N). \tag{5.37}$$

Note that $\delta TC1_R$ has a negative value (since $TC1_P > 0$ and $TC1_N < 0$), meaning that $TC1_R$ decreases as the value of the temperature coefficient trim code TCT increases. Accordingly, this is opposite for the output frequency (5.20), where the frequency temperature coefficient $TC1_f$ increases together with the increase of TCT value, having a typical step of

$$\delta TC1_f = \frac{R_S}{R_{REF0}}(TC1_P - TC1_N). \tag{5.38}$$

Furthermore, considering (5.16), (5.34), and (5.38), $TC1_R$ can be expressed as

$$TC1_R = TC1_{R0} + TCT \cdot \delta TC1_R = TC1_{R0} - TCT \cdot \delta TC1_f, \tag{5.39}$$

which, combined with (5.20), leads to:

$$TC1_f = -TC1_{R0} - TC1_C - TC1_{tc} + TCT \cdot \delta TC1_f. \tag{5.40}$$

The output frequency first–order temperature coefficient trim value can be defined as

$$\Delta TC1_f = TCT \cdot \delta TC1_f, \tag{5.41}$$

having the optimal value $\Delta TC1_f^*$ equal to

$$\Delta TC1_f^* = TC1_{R0} + TC1_C + TC1_{tc}, \tag{5.42}$$

as calculated from (5.40) under the condition $TC1_f = 0$. However, since the trim code TCT is limited to integer values, the first–order temperature coefficient of the output frequency can be tuned within half of the trimming step, specifically

$$-\left|\frac{\delta TC1_f}{2}\right| \leq TC1_f \leq \left|\frac{\delta TC1_f}{2}\right|. \tag{5.43}$$

Accordingly, the trim code optimal value TCT^* can be expressed as

$$TCT^* = round\left[\frac{\Delta TC1_f^*}{\delta TC1_f}\right] = round\left[\frac{TC1_{R0} + TC1_C + TC1_{tc}}{\delta TC1_f}\right]. \tag{5.44}$$

In conclusion, the nominal temperature coefficient of the reference resistor $TC1_{R0}$ should be adjusted to compensate for the combined contribution of the reference capacitor and the oscillator core ($TC1_C + TC1_{tc}$) under the typical conditions, while sample–to–sample variations can be compensated using the appropriate temperature coefficient trim code TCT in the post–production phase.

5.2.4 Current Mirror

The schematic of the current mirror (CMIR) is shown in Fig. 5.5, with the design parameters listed in Table 5.4. The block consists of the current mirrors (M_{N1-5}, M_{P1-4}), the bias circuit (M_{N6-8}, M_{P5-6}, R_1), and the cascode transistors (M_{N9-11}, M_{P7-9}). The current mirror receives the reference current I_{REF} and provides three core reference currents (two having the value I_{REF} and one with half the value $½I_{REF}$). Also, the bias currents for the core comparators (I_{BC1-2}) and the voltage–to–current converter (I_{BV2I}) are supplied from the block. The sizing of the devices within the current mirror block must be considered carefully to provide good matching for high–performance core operation.

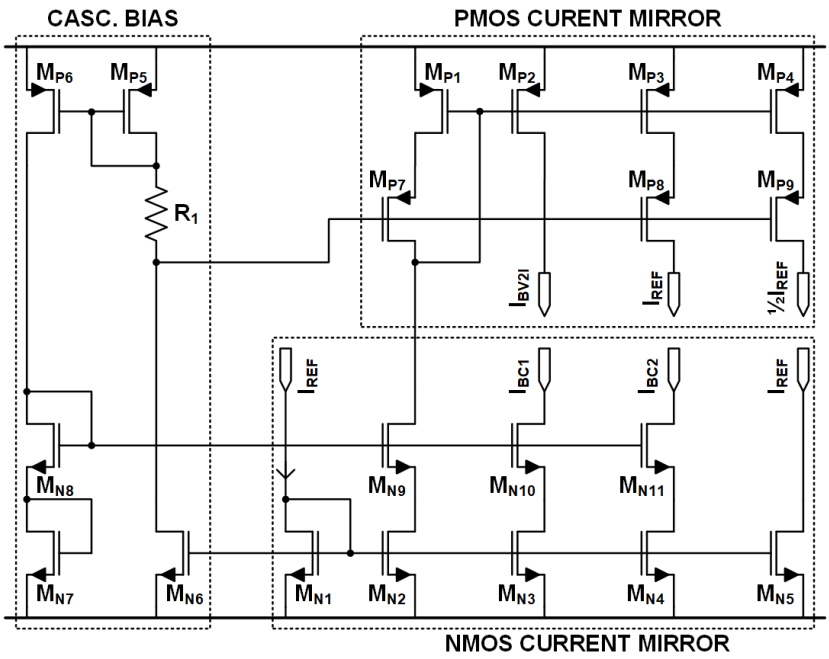


Figure 5.5: The schematic of the current mirror. The input reference current is mirrored to provide the core reference currents, together with the V2I and comparator bias currents (I_{BV2I}, I_{BC1-2}).

Table 5.4: The design parameters of the current mirror.

Transistor	W [µm]	L [µm]	I_D [µA]	Device
$M_{N1-2,5}$[1:8]	0.48	3.6	5	nmos2v
M_{N3-4}[1:3]	0.48	3.6	1.88	nmos2v
M_{N6}[1:4]	0.48	3.6	2.5	nmos2v
M_{N7}[1:2]	0.48	3.6	1.25	nmos2v
M_{N8}[1:2]	1.44	0.36	1.25	nmos2v
M_{N9}[1:8]	1.44	0.36	5	nmos2v
M_{N10-11}[1:3]	1.44	0.36	1.88	nmos2v
$M_{P1,3}$[1:8]	1.8	3.6	5	pmos2v
$M_{P2,4}$[1:4]	1.8	3.6	2.5	pmos2v
M_{P5}[1:4]	2	7.2	2.5	pmos2v
M_{P6}[1:2]	2	7.2	1.25	pmos2v
M_{P7-8}[1:8]	0.72	0.54	5	pmos2v
M_{P9}[1:4]	0.72	0.54	2.5	pmos2v
Resistor	W [µm]	L [µm]	Res [kΩ]	**Device**
R_1	0.5	100	70.8	rpoly

W and L are single finger dimensions.
I_D is overall device current.

5.2.5 Core Architecture

The schematic of the relaxation oscillator core with replica chopped comparator [57] is shown in Fig. 5.6. The core is a modified version of the self–compensating relaxation oscillator core presented in Chapter 3, having the main difference in the chopped comparator arrangement that enables a simpler control logic and better signal integrity. The oscillator core consists of two integrator blocks, a chopped comparator block, and a logic block. Each integrator includes three current sources (the first and third supplying the reference current I_{REF} and the second one having half the reference current $½I_{REF}$), four switches controlled by the output signals of the logic block, and the capacitor having the capacitance value C_{REF}. The chopped comparator block consists of one switching block and two identically designed comparators, where the first comparator always operates as a sensing comparator, while the second comparator operates as a replica comparator. The operation of the switching block is described by the signal mapping shown in Fig. 5.6, defining the two states of the chopper depending on the corresponding control signals. Finally, the logic block processes the comparator outputs into the control signals, feeding them back to the integrator block and chopped comparator block, maintaining the oscillation in this way.

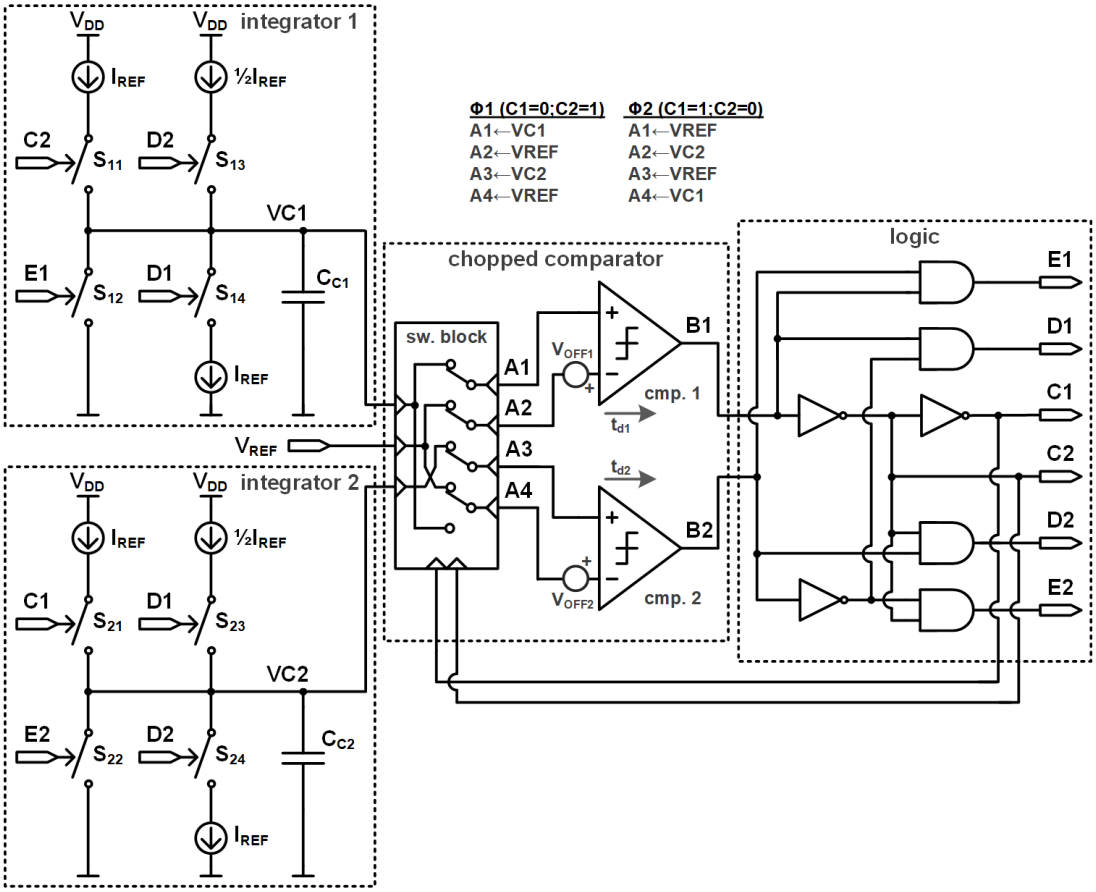


Figure 5.6: The schematic of the relaxation oscillator core with replica chopped comparator, comprising two identical integrator blocks, a chopped comparator block, a masking circuit, and a logic block.

The operation of the oscillator core in Fig. 5.6 is described with reference to the corresponding waveforms shown in Fig. 5.7. At an initial time ($t = t_0$), it is assumed that all the signals are set to the initial state by a start–up circuit (not shown in the schematic). Initially, the chopper state is set to ϕ_1, and the integration occurs within the first integrator in the time interval from t_0 to t_2. The integrating voltage $VC1$ rises linearly, having the nominal slope $\Delta VC1/\Delta t = I_{REF}/C_{REF}$. Due to the initial configuration of the chopper, while $C1$ is low and $C2$ is high, the integrating signal $VC1$ is present at the switch output $A1$ ($VC1 \mapsto A1$). Meanwhile, the second integrator block remains idle as the integration node $VC2$ is shorted to the ground reference node by the switch S_{22}. At a subsequent time, $t = t_1$, the integrating signal $VC1$, which is present at the switch output $A1$ ($VC1 \mapsto A1$), becomes equal to the reference voltage V_{REF} present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the output of the first comparator

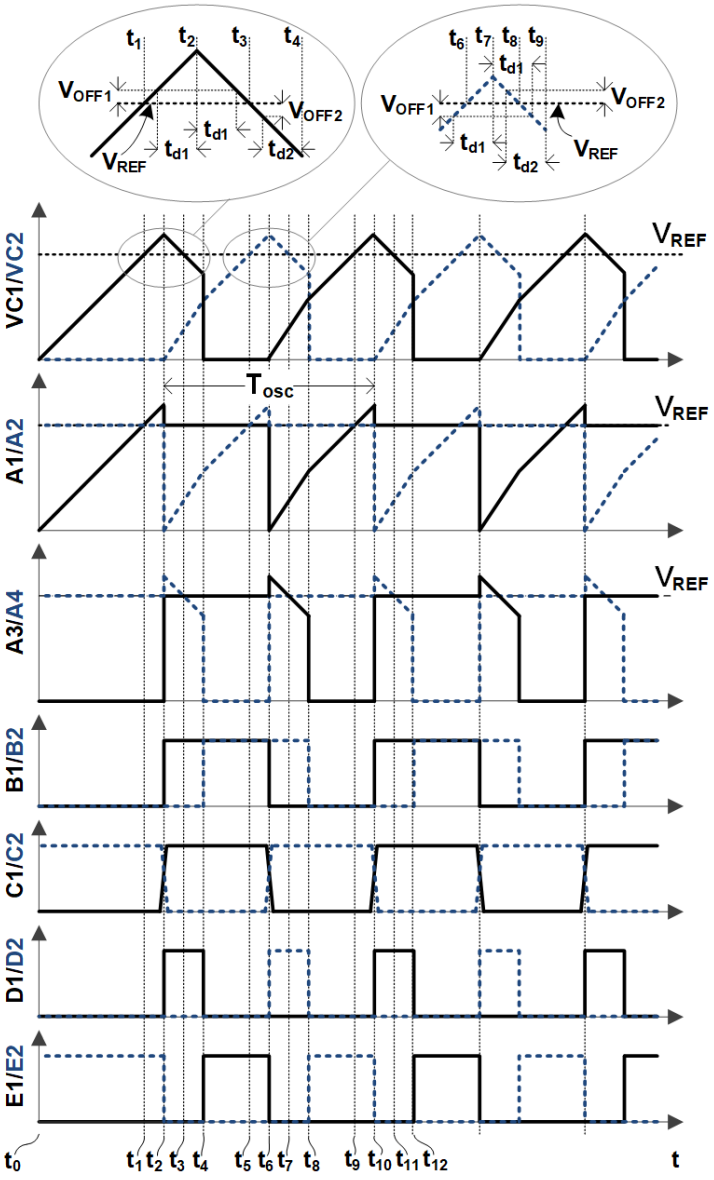


Figure 5.7: The signal waveforms of the relaxation oscillator core with replica chopped comparator.

$B1$ changes to high at $t = t_2$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. The timing can be expressed as follows:

$$t_2 = \frac{(V_{REF} + V_{OFF1})C_{REF}}{I_{REF}} + t_{d1}. \tag{5.45}$$

Following the change of the first comparator output $B1$, the logic block output signals $C1$, $C2$, $D1$, and $E2$ also change to high, low, high, and low, respectively. Consequently, the chopper state is set to ϕ_2. The integration starts within the second integrator block such that the integrating signal $VC2$ present at the switch output $A2$ ($VC2 \mapsto A2$) rises linearly, having the slope $\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC1$, which is also present at the switch output $A4$ ($VC1 \mapsto A4$), starts to decrease, now having the opposite slope $\Delta VC1/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the arrangement of the first and the second comparator and the opposite slopes of the integrating voltage $VC1$ around the crossover points with the reference voltage V_{REF} (t_1 and t_3), the operation of the first (sensing) comparator in the time interval from t_1 to t_2 is replicated by the second (replica) comparator in the time interval from t_3 to t_4. Specifically, at $t = t_3$, the integrating signal $VC1$, which is present at the switch output $A4$ ($VC1 \mapsto A4$), becomes equal to the reference voltage V_{REF} also present at the switch output $A3$ ($V_{REF} \mapsto A3$). Nevertheless, the output of the second comparator $B2$ changes to high at $t = t_4$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. In this way, as a function of the comparator outputs $B1$ and $B2$, the logic block generates a positive pulse on the measurement signal $D1$ in the time interval from t_2 to t_4, having the duration

$$t_{D1} = t_4 - t_2 = t_{d1} + t_{d2} + \frac{(V_{OFF1} + V_{OFF2})C_{REF}}{I_{REF}}. \tag{5.46}$$

The influence of the first comparator prior to $t = t_2$ is compensated with a 50% increase in the slope of the integrating signal $VC2$ compared to the nominal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D1}. The voltage of the integration node $VC2$ at the time $t = t_4$, hereafter denoted $VC2(t_4)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC2/\Delta t = 1.5I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D1}, and can be represented as follows:

$$VC2(t_4) = \Delta VC2/\Delta t \cdot t_{D1} = \frac{3I_{REF}}{2C_{REF}}(t_{d1} + t_{d2}) + \frac{3}{2}(V_{OFF1} + V_{OFF2}). \tag{5.47}$$

Following from the change of the second comparator output $B2$, the logic block output signal $E1$ also changes to high. After $t = t_4$, the integrating signal $VC2$ continues to rise linearly with the nominal slope ($\Delta VC2/\Delta t = I_{REF}/C_{REF}$). Meanwhile, the first integrator block is idle as the integration node $VC1$ is shorted to the ground reference node by the switch S_{12}. At a subsequent

time, $t = t_5$, the integrating signal $VC2$, which is present at the switch output $A2$ ($VC2 \mapsto A2$), becomes equal to the reference voltage V_{REF} present at the switch output $A1$ ($V_{REF} \mapsto A1$). Nevertheless, the output of the first comparator $B1$ changes to low at $t = t_6$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. The timing can be expressed as

$$t_6 - t_4 = \frac{(V_{REF} - V_{OFF1} - VC2(t_4))C_{REF}}{I_{REF}} + t_{d1}, \tag{5.48}$$

where the offset voltage V_{OFF1} has the opposite contribution compared to the previous half–cycle (5.45), resulting from the switched polarity of the comparator. Following the change of the first comparator output $B1$, the logic block output signals $C1$, $C2$, $D2$, and $E1$ also change to low, high, high, and low, respectively. Consequently, the chopper state is set to ϕ_1. The integration starts within the first integrator block such that the integrating signal $VC1$ present at the switch output $A1$ ($VC1 \mapsto A1$) rises linearly, having the slope $\Delta VC1/\Delta t = 1.5 I_{REF}/C_{REF}$. Meanwhile, the integrating signal $VC2$, which is also present at the switch output $A3$ ($VC2 \mapsto A3$), starts to decrease, now having the opposite slope $\Delta VC2/\Delta t = -I_{REF}/C_{REF}$. Resulting from the combination of the arrangement of the first and the second comparator and the opposite slopes of the integrating voltage $VC2$ around the crossover points with the reference voltage V_{REF} (t_5 and t_7), the operation of the first (sensing) comparator in the time interval from t_5 to t_6 is replicated by the second (replica) comparator in the time interval from t_7 to t_8. Specifically, at $t = t_7$, the integrating signal $VC2$, which is present at the switch output $A3$ ($VC2 \mapsto A3$), becomes equal to the reference voltage V_{REF} also present at the switch output $A4$ ($V_{REF} \mapsto A4$). Nevertheless, the output of the second comparator $B2$ changes to low at $t = t_8$ due to the non–ideal characteristics of the second comparator, namely the propagation delay t_{d2} and the offset voltage V_{OFF2}. In this way, as a function of the comparator outputs $B1$ and $B2$, the logic block generates a positive pulse on the measurement signal $D2$ in the time interval from t_6 to t_8, having the duration

$$t_{D2} = t_8 - t_6 = t_{d1} + t_{d2} - \frac{(V_{OFF1} + V_{OFF2})C_{REF}}{I_{REF}}. \tag{5.49}$$

where the offset voltages V_{OFF1} and V_{OFF2} have the opposite contribution compared to the previous half–cycle (5.46), resulting from the switched polarity of both comparators. The influence of the first comparator prior to $t = t_6$ is compensated with a 50% increase in the slope of the integrating signal $VC1$ compared to the nominal ($\Delta VC1/\Delta t = 1.5 I_{REF}/C_{REF}$) for the measurement signal pulse duration t_{D2}. The voltage of the integration node $VC1$ at the time $t = t_8$, hereafter denoted $VC1(t_8)$, can be calculated as a function of the slope of the integrating signal ($\Delta VC1/\Delta t = 1.5 I_{REF}/C_{REF}$) and the measurement signal pulse duration t_{D2}, and can be

represented as follows:

$$VC1(t_8) = \Delta VC1/\Delta t \cdot t_{D2} = \frac{3I_{REF}}{2C_{REF}}(t_{d1} + t_{d2}) - \frac{3}{2}(V_{OFF1} + V_{OFF2}). \tag{5.50}$$

Following the change of the second comparator output $B2$, the logic block output signal $E2$ also changes to high. After $t = t_8$, the integrating signal $VC1$ continues to rise linearly with the nominal slope ($\Delta VC1/\Delta t = I_{REF}/C_{REF}$). Meanwhile, the second integrator block is idle as the integration node $VC2$ is shorted to the ground reference node by the switch S_{22}. At a subsequent time, $t = t_9$, the integrating signal $VC1$, which is present at the switch output $A1$ ($VC1 \mapsto A1$), becomes equal to the reference voltage V_{REF} present at the switch output $A2$ ($V_{REF} \mapsto A2$). Nevertheless, the output of the first comparator $B1$ changes to high at $t = t_{10}$ due to the non–ideal characteristics of the first comparator, namely the propagation delay t_{d1} and the offset voltage V_{OFF1}. The timing can be expressed as follows:

$$t_{10} - t_8 = \frac{(V_{REF} + V_{OFF1} - VC1(t_8))C_{REF}}{I_{REF}} + t_{d1}. \tag{5.51}$$

With this, a complete oscillation cycle is described from t_2 to t_{10}. The duration of one oscillation period can be calculated by adding the time segments as follows:

$$T_{osc} = (t_4 - t_2) + (t_6 - t_4) + (t_8 - t_6) + (t_{10} - t_8), \tag{5.52}$$

resulting in

$$T_{osc} = \frac{2V_{REF}C_{REF}}{I_{REF}} + t_{d1} - t_{d2}. \tag{5.53}$$

As seen from (5.53), the comparator's offset is entirely canceled by switching the polarities of the sensing and replica comparator with each half–cycle, while the delay of the sensing comparator is compensated by measuring the delay of the second comparator. Moreover, the difference between the propagation delays of the two comparators, as demonstrated in Section 2.3.2, is expected to remain relatively small ($t_{d1} - t_{d2} \approx 0$) if appropriate matching techniques are applied. Therefore, the expression for the oscillation period can be further simplified to

$$T_{osc} \approx \frac{2V_{REF}C_{REF}}{I_{REF}}, \tag{5.54}$$

or taking (5.1) into account

$$T_{osc} \approx 2R_{REF}C_{REF}. \tag{5.55}$$

Ultimately, the temperature drift of the oscillator core is primarily determined by the temperature drift of the passive elements, namely the resistor and the capacitor, along with the other minor effects neglected within this analysis (e.g., device mismatch, logic propagation delay, and switching non–idealities).

5.2.6 Oscillator Prototype

The 2–MHz prototype of the self–sustaining oscillator from Fig. 5.1, including the relaxation oscillator core with replica chopped comparator (w/–RCC), is designed and manufactured in 180 nm technology. The prototype layout and the corresponding micro–photography of a manufactured sample are shown in Fig. 5.8, having a total area of 385 µm × 195 µm (0.075 mm^2).

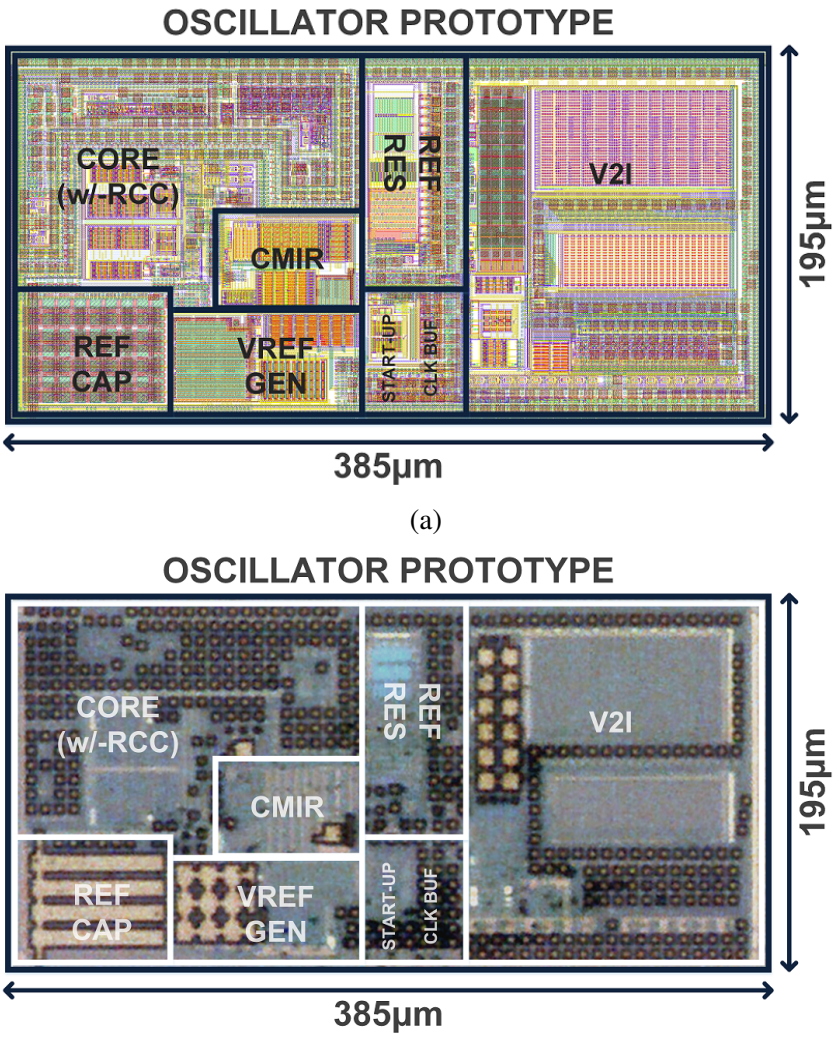


Figure 5.8: The self–sustaining oscillator prototype (a) layout (b) micro–photography. The oscillator occupies an area of 0.075 mm^2, whereas the core occupies an area of 0.021 mm^2.

The design details of the supporting building blocks, namely the voltage reference generator, voltage–to–current converter, tunable reference resistor, and current mirror, are already described in the previous sections of this chapter, respectively 5.2.1, 5.2.2, 5.2.3, and 5.2.4. The top–level design parameters of the oscillator prototype are shown in Table. 5.5. Furthermore, the design parameters of the core from Fig. 5.6 are listed in Table 5.6. The switches within the two integrator blocks (S_{11-14}, S_{21-24}), denoted as S_{int}, are identical and implemented with a single nMOS transistor. On the other hand, the switches within the switching block, denoted

Table 5.5: The top–level design parameters of the oscillator prototype.

Design Parameter	Value
V_{REF0}	330 mV
V_{REF}	500 mV
I_{REF0}	5 µA
I_{REF}	5 µA
I_{BV2I}	2.5 µA
I_{BC1-2}	1.88 µA

Table 5.6: The design parameters of the relaxation oscillator core with replica chopped comparator.

Switch	W [µm]	L [µm]		Device
S_{int}	1.8	0.2		nmos2v
S_{chop}	0.48	0.22		nmos2v+pmos2v
Capacitor	**W [µm]**	**L [µm]**	**Cap [pF]**	**Device**
C_{C1-2}[1:12]	10	10	2.52	cmim

W and L are single finger dimensions.
Cap is overall capacitance.

as S_{chop}, are implemented as CMOS analog switches with identically sized nMOS and pMOS transistors. The two reference capacitors C_{C1-2} are metal–insulator–metal type (MIM). The schematic of two comparators used in the core is shown in Fig. 5.9, consisting of a symmetrical OTA (M_{P1-6} and M_{N1-4}) and a buffer (M_{N5-6} and M_{P7-8}). The design parameters of the comparator from Fig. 5.9 are shown in Table 5.7.

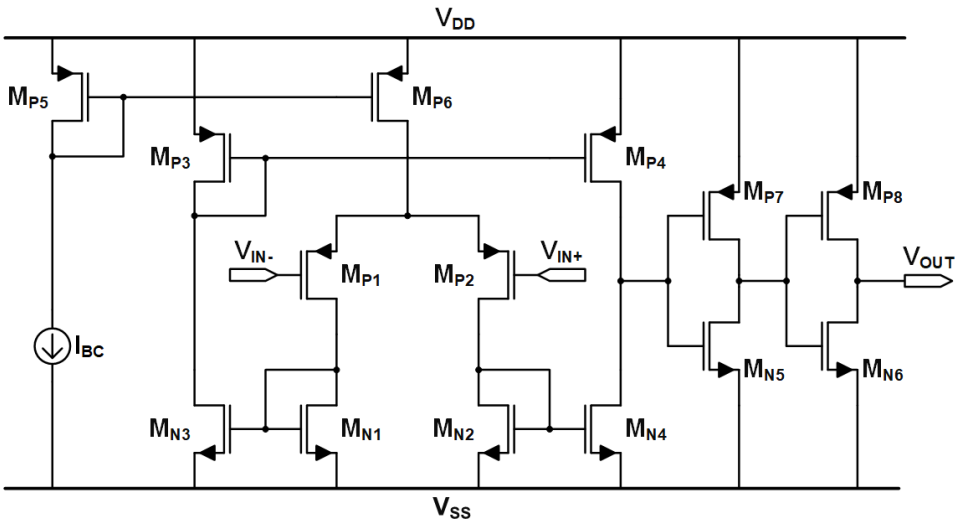


Figure 5.9: The schematic of the comparator.

Table 5.7: The design parameters of the comparator.

Transistor	W [µm]	L [µm]	I_D [µA]	Device
M_{N1-2}[1:2]	1.8	1.8	3.75	nmos2v
M_{N3-4}[1:4]	1.8	1.8	7.5	nmos2v
M_{P1-2}[1:2]	3.6	1.8	3.75	pmos2v
M_{P3-4}[1:4]	1.8	1.8	7.5	pmos2v
M_{P5}[1:2]	1.8	1.8	1.88	pmos2v
M_{P6}[1:8]	1.8	1.8	7.5	pmos2v
M_{N5}	0.24	0.48		nmos2v
M_{N6}	0.48	0.28		nmos2v
M_{P7-8}	0.54	0.24		pmos2v

W and L are single finger dimensions.
I_D is overall device current.

5.2.7 Test Bench

The test bench for the transient simulations of the oscillator prototype is shown in Fig. 5.10. The default value of the supply voltage is $V_{DD} = 1.8$ V. The rising edge of the enable signal EN initiates the start–up of the oscillator. The 8–bit frequency trim word FQT[7:0] and the 4–bit temperature coefficient trim word TCT[3:0] are provided in 2's complement format, having the input range from -128 to $+127$ for the frequency trim code and -8 to $+7$ for the temperature coefficient trim code.

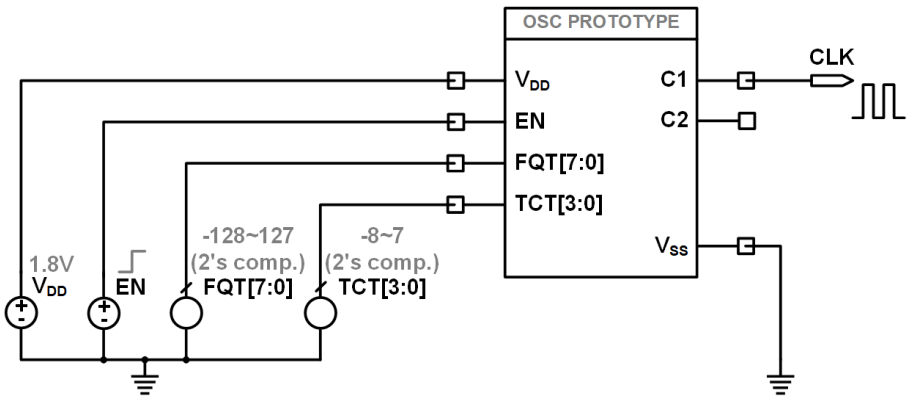


Figure 5.10: The test bench for the transient simulations of the self–sustaining oscillator prototype.

The test bench from Fig. 5.11 is assumed for the transient simulations of the isolated oscillator core (excluding the other building blocks). The default value of the supply voltage is $V_{DD} = 1.8$ V, while the values of the externally sourced references are $V_{REF} = 0.5$ V and $I_{REF} = 5$ µA. The bias currents of the two comparators are not shown in the schematic.

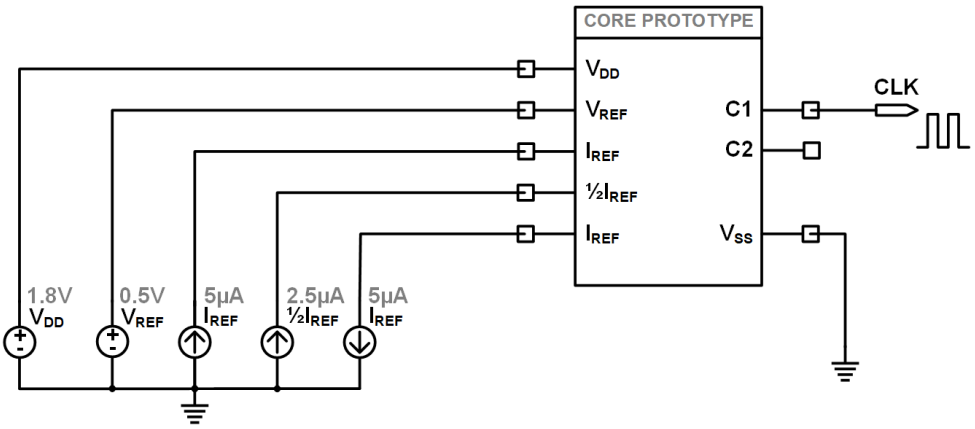


Figure 5.11: The test bench for the transient simulations of the oscillator core.

5.3 Calibration Method

5.3.1 Center Frequency Calibration

The center frequency is tuned by calibrating the reference current I_{REF} within the 8–bit current DAC at the nominal conditions to overcome the process variations of the reference capacitor and resistor. Already demonstrated in (5.12), the linear dependency of the output frequency f_{osc} on the frequency trim code FQT can be expressed as

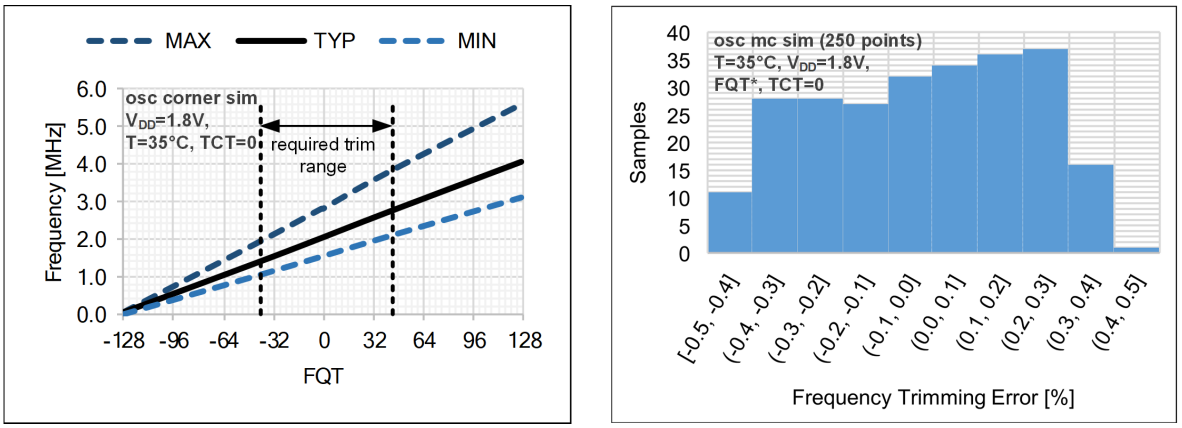
$$f_{osc} = \left(\frac{FQT}{129} + 1\right) f_{osc0}, \tag{5.56}$$

where f_{osc0} is the frequency value of the untrimmed oscillator (at $FQT = 0$). Correspondingly, the value of the frequency trim code that provides the closest output frequency to f_{osc} is

$$FQT(f_{osc}) = round\left[129\left(\frac{f_{osc}}{f_{osc0}} - 1\right)\right], \tag{5.57}$$

assuming an ideal DAC. Considering the eventual DAC non–linearity, inspecting several neighboring codes of the calculated FQT is advisable to determine the optimal value (FQT^*).

The frequency response for different process corners with respect to the frequency trim code FQT is shown in Fig. 5.12a. The oscillator frequency can be set from 15.6 kHz to 4 MHz for the typical corner, where the required frequency trim code range for calibrating the center frequency to 2 MHz is from $FQT = -38$ to $FQT = +42$ across all corners. At the nominal trim step of 15.6 kHz, the expected center frequency accuracy is $\pm 0.39\%$, plus the eventual non–linearity and mismatch effects of the DAC. The histogram of the simulated center frequency error after trimming is shown in Fig. 5.12b. The frequency error is less than $\pm 0.5\%$ relative to the 2 MHz target frequency across 250 Monte Carlo simulations.



(a) (b)

Figure 5.12: (a) The corner simulation of the output frequency f_{osc} vs. frequency trim code FQT. (b) The histogram of the post–trim center frequency error relative to 2 MHz.

5.3.2 Temperature Calibration

The tuning property of the first–order temperature coefficient of the output frequency is implemented within the designed oscillator prototype from Section 5.2.6 using the tunable reference resistor. With this, the accuracy versus temperature is improvable by adjusting the first–order temperature coefficient $TC1_f$ for each oscillator sample. The typical frequency response of the oscillator prototype versus temperature, simulated for different temperature coefficient trim code (TCT) values, is shown in Fig. 5.13. Here, changing the trim code TCT shifts the first–order temperature coefficient $TC1_f$ in $\delta TC1_f = 20$ ppm/°C steps. Therefore, the first–order temperature coefficient is tunable within half the value of the tuning step; specifically $|TC1_f| < ½\delta TC1_f = 10$ ppm/°C, also assuming that the required temperature coefficient trim value $\Delta TC1_f$ is within the absolute tuning range (in this case from -160 ppm/°C to $+140$ ppm/°C).

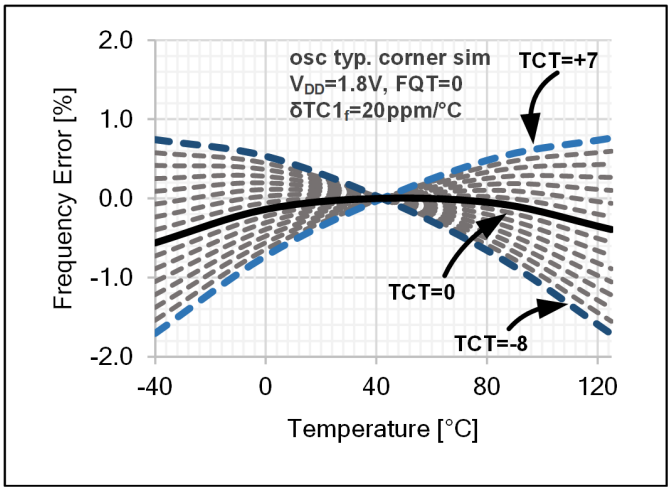


Figure 5.13: The simulated frequency drift vs. temperature for different temperature coefficient trim code TCT values. The first–order temperature coefficient $TC1_f$ is tunable in $\delta TC1_f = 20$ ppm/°C steps.

Most often, the variation of the output frequency over the temperature for relaxation oscillators can be approximated using the second–order polynomial (C.2), especially valid if the contribution of strongly non–linear building blocks (e.g., the oscillator core) is reduced. In this case, the frequency measurement at three different temperatures is sufficient to approximate the frequency characteristic with a polynomial and calculate the corresponding optimal temperature coefficient trim value $\Delta TC1_f^*$ for each sample.

Accordingly, Fig. 5.14 illustrates the concept of the three–point temperature calibration (3PTC). Here, three points are measured for each oscillator sample: the frequency $f_{osc}(T_0)$ at the nominal temperature T_0, $f_{osc}(T_L)$ at $T_L < T_0$, and $f_{osc}(T_H)$ at $T_H > T_0$. The minimal frequency drift over the entire temperature range is achieved if the first–order temperature coefficient $TC1_f$ is adjusted in such a way that the frequency values of the border temperatures (T_{MIN} and T_{MAX}) are equal, particularly, $f_{osc}(T_{MIN}) = f_{osc}(T_{MAX})$.

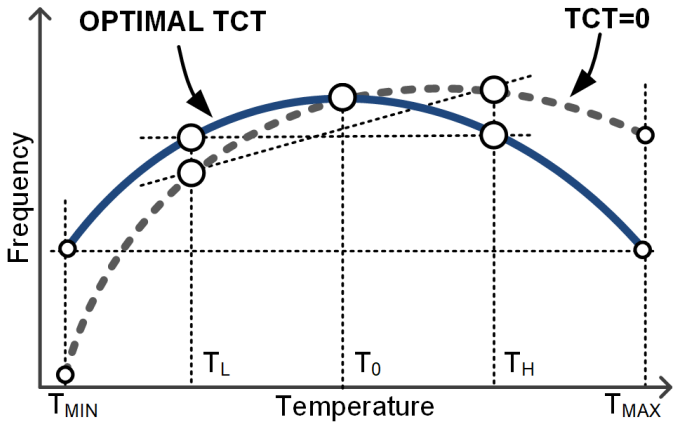


Figure 5.14: The temperature calibration concept with three–point measurement (3PTC). The oscillation frequency is measured at three different temperatures (T_L, T_0, and T_H), and the temperature coefficient trim code TCT is adjusted to achieve a minimum frequency drift over the entire temperature range, assuming the second–order polynomial frequency characteristic.

Derived in Appendix C.2, the optimal first–order temperature coefficient trim value $\Delta TC1_f^*$ (5.42) can be calculated using three–point measurement as

$$\Delta TC1_f^* = \frac{\frac{T_0-T_{MAX}-T_{MIN}+T_L}{T_H-T_0}\left[f_{osc}(T_H)-f_{osc}(T_0)\right]-\frac{T_0-T_{MAX}-T_{MIN}+T_H}{T_L-T_0}\left[f_{osc}(T_L)-f_{osc}(T_0)\right]}{f_{osc}(T_0)\cdot(T_H-T_L)}. \tag{5.58}$$

Also demonstrated in Appendix C.2, in a specific case where the high and low measurement temperatures T_H and T_L are equally distant from their respective border temperatures T_{MAX} and T_{MIN}, in particular, $T_{MAX}-T_H = T_L-T_{MIN}$, the expression for $\Delta TC1_f^*$ reduces to

$$\Delta TC1_f^* = -\frac{f_{osc}(T_H)-f_{osc}(T_L)}{f_{osc}(T_0)\cdot(T_H-T_L)}. \tag{5.59}$$

Although the 3–point temperature calibration would result in the minimum frequency variation with respect to temperature, leaving only the second–order effects, the presented method is rarely applicable in industrial applications. Any additional temperature measurement represents a considerable cost overhead, especially for temperatures lower than the room temperature. For this reason, a high–volume production most often only allows for the measurements at two temperatures, specifically at the nominal temperature and at the second temperature larger than the nominal.

Accordingly, the two–point temperature calibration (2PTC) is illustrated in Fig. 5.15, where only two points are measured for each oscillator sample: the frequency $f_{osc}(T_0)$ at the nominal temperature T_0 and the frequency $f_{osc}(T_H)$ at the high measurement temperature T_H. Unlike the three–point temperature calibration, in this case, it is generally not possible to calculate the optimal value for the temperature coefficient adjustment, considering a second–order characteristic of the temperature dependency [27].

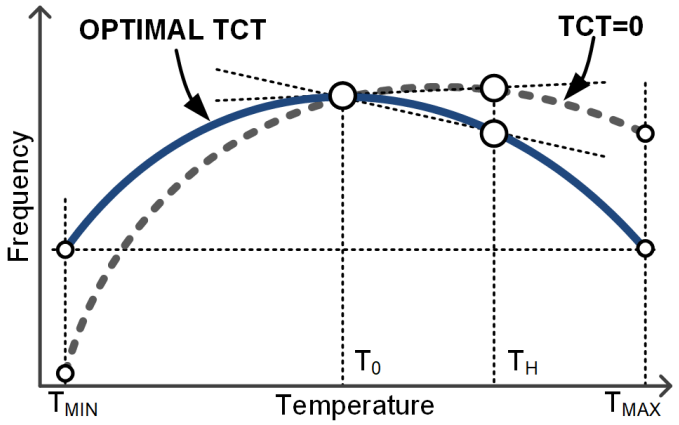


Figure 5.15: The temperature calibration concept with a two–point measurement (2PTC). The oscillation frequency is measured at two different temperatures (T_0 and T_H), and the temperature coefficient trim code TCT is adjusted to achieve a minimum frequency drift over the entire temperature range. The method estimates the optimal trim code assuming the second–order polynomial behavior of the frequency characteristic.

Nevertheless, as demonstrated in Appendix C.3, (C.16)–(C.23), the optimal trim value $\Delta TC1_f^*$ can be calculated with only two measured values if the two temperatures, T_0 and T_H, are equidistant from the midpoint of the temperature range, specifically

$$\frac{T_{MAX}+T_{MIN}}{2} - T_0 = T_H - \frac{T_{MAX}+T_{MIN}}{2}. \tag{5.60}$$

In this case, the two–point measurement variable $\Delta TC1'_f$, defined in (C.28) as

$$\Delta TC1'_f = -\frac{f_{osc}(T_H) - f_{osc}(T_0)}{f_{osc}(T_0)\cdot(T_H - T_0)}, \tag{5.61}$$

is equal to the optimal temperature coefficient trim value $\Delta TC1_f^*$. Otherwise, in a general case where the condition from (5.60) is not fulfilled, $\Delta TC1_f^*$ can be estimated using the linear transformation of the two–point measurement variable $\Delta TC1'_f$, particularly

$$\Delta TC1_f^* \approx a\cdot\Delta TC1'_f + b. \tag{5.62}$$

The detailed analysis leading to (5.62) is described in Appendix C.3, with the expressions for the calculation of the coefficients a and b shown in (C.36) and (C.37), respectively. The values of the linear transformation coefficients a and b will differ regarding the choice of the measurement points (T_0 and T_H) and the observed temperature range (from T_{MIN} to T_{MAX}). Therefore, for a specific measurement setup, the optimal coefficients a and b are to be obtained using either simulations or measurements, calculated on a limited number of samples for which a sufficiently high R^2 value is achieved.

The proposed two–point temperature calibration (2PTC) method is demonstrated with 250 Monte Carlo simulations of the oscillator prototype from Section 5.2.6. Specifically, the optimal temperature coefficient trim value $\Delta TC1_f^*$ and the two–point measurement variable $\Delta TC1'_f$ were calculated for each simulated sample, using the corresponding frequency characteristic over the temperature. The simulated temperature change is from -40°C to 125°C, assuming $T_0 = 35$°C and $T_H = 85$°C for the calculation of $\Delta TC1'_f$ (5.61). The simulation results are exhibited in Fig. 5.16, showing the relation between $\Delta TC1'_f$ and $\Delta TC1_f^*$.

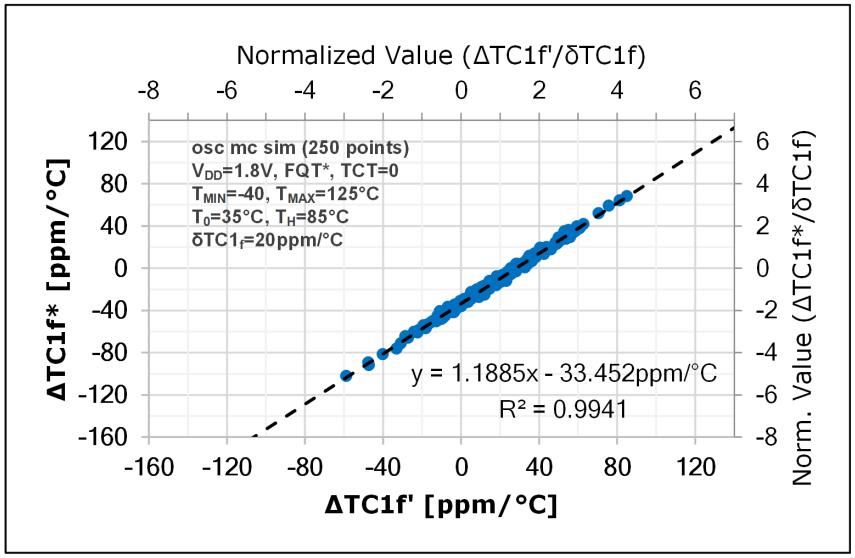


Figure 5.16: The simulation of the optimal temperature coefficient trim value $\Delta TC1_f^*$ plotted versus two–point measurement variable $\Delta TC1'_f$ calculated using the 2PTC method. The optimal trim value $\Delta TC1_f^*$ can be approximated by the linear transformation $\Delta TC1_f^* \approx 1.1885 \cdot \Delta TC1'_f - 33.452$ ppm/°C for $T_0 = 35$°C and $T_H = 85$°C.

The presented results confirm that the optimal trim value $\Delta TC1_f^*$ can be well estimated from only two measured points at different temperatures since $\Delta TC1_f^*$ and $\Delta TC1'_f$ are highly correlated ($R^2 = 0.9941$). Considering (5.62), the calculated linear transformation coefficients, $a = 1.1885$ and $b = -33.452$ ppm/°C, provide the equation for the approximation of the optimal trim code for the test–case oscillator, specifically

$$\Delta TC1_f^* \approx \Delta TC1_f = 1.1885 \cdot \Delta TC1'_f - 33.452 \text{ ppm/°C}, \tag{5.63}$$

or, considering (5.61),

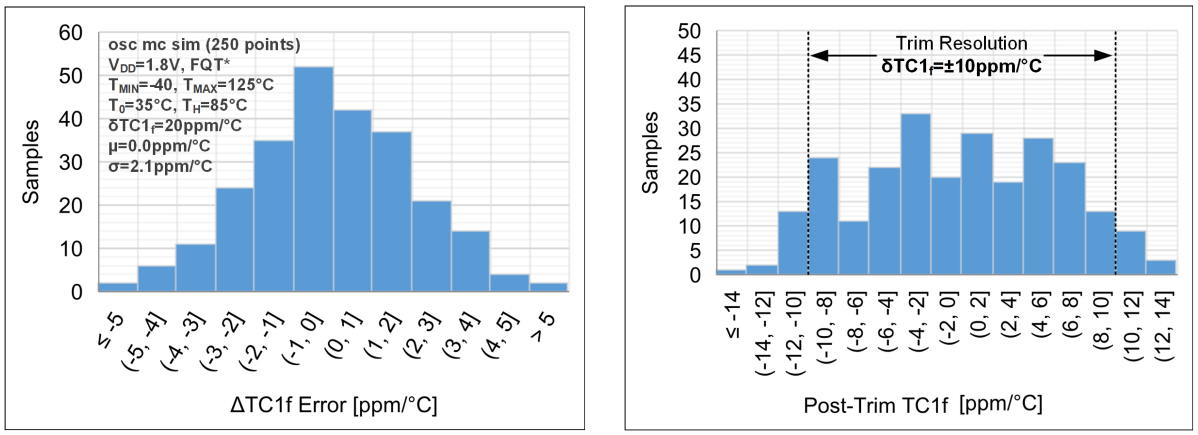
$$\Delta TC1_f^* \approx \Delta TC1_f = -1.1885 \cdot \frac{f_{osc}(T_H) - f_{osc}(T_0)}{f_{osc}(T_0) \cdot (T_H - T_0)} - 33.452 \text{ ppm/°C}. \tag{5.64}$$

From (5.64), the error of the approximated optimal trim value relative to the actual optimal value ($\Delta TC1_f - \Delta TC1_f^*$) is presented in Fig. 5.17a, calculated for the test–case oscillator from the simulation data. The error has the standard deviation of $\sigma(\Delta TC1_f - \Delta TC1_f^*) = 2.1$ ppm/°C,

and ranges from -5.5 ppm/°C to $+6.4$ ppm/°C. Furthermore, since the optimal trim code TCT^* is generally calculated by dividing the optimal temperature coefficient trim value $\Delta TC1_f^*$ with the tuning step $\delta TC1_f$ (5.44), specifically,

$$TCT^* = round\left[\frac{\Delta TC1_f^*}{\delta TC1_f}\right], \tag{5.65}$$

it is also necessary to consider the rounding error to calculate the trimming method's overall accuracy. In particular, the rounding introduces the additional error of $\pm½\delta TC1_f$ (5.43) (in this case ± 10 ppm/°C), uniformly distributed. Accordingly, Fig. 5.17b shows the overall post–trim temperature coefficient $TC1_f$, ranging from -14.9 ppm/°C to $+13.1$ ppm/°C, where both the calculation error of $\Delta TC1_f$ (shown in Fig. 5.17a) and the trimming rounding error are included.



(a) (b)

Figure 5.17: (a) The histogram of the trim value $\Delta TC1_f$ error $(\Delta TC1_f - \Delta TC1_f^*)$ relative to the optimal value, evaluated using Monte Carlo simulations of the 2PTC method. (b) The histogram of the overall post–trim first–order temperature coefficient $TC1_f$, including the error of the 2PTC method from (a) and the finite trimming resolution.

While the demonstrated test–case of the 2PTC method is conducted in the ideal environment assumed within the simulation setup, the post–production measurements incorporate the uncertainty of the measured frequency value versus the actual value. Such measurement errors can be caused by several factors, the most important being the noise influence and the finite accuracy of the measurement setup. Here, primarily $1/f$ noise should be considered since white noise can be averaged out by measuring a sufficiently large time window [24]. Fig. 5.18 shows the simulated influence of the frequency uncertainty (σ_f) on the error of the calculated trim value $\Delta TC1_f$ relative to the optimal value, plotted versus temperature difference $(T_H - T_0)$ of the 2PTC measurement points. As seen from the figure, the accuracy of the 2PTC is best for low $T_H - T_0$ values in the ideal environment $(\sigma_f = 0)$, where the second–order effects of the oscillator are suppressed. Nonetheless, higher $T_H - T_0$ values are required in the setups with limited accuracy to bring the error within the trimming resolution range.

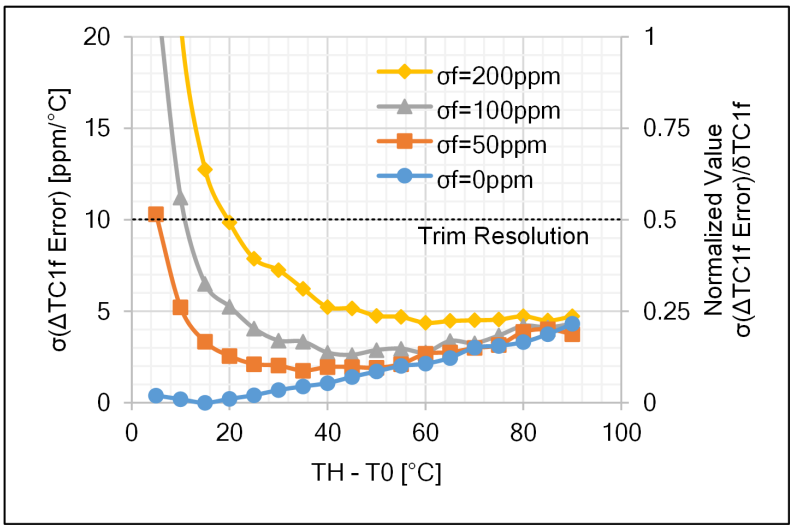


Figure 5.18: The standard deviation of the calculated trim value $\Delta TC1_f$ error relative to the optimal value, $\sigma(\Delta TC1_f - \Delta TC1_f^*)$, vs. temperature difference $(T_H - T_0)$, simulated using the 2PTC method with $T_0 = 35°C$. The simulations are performed assuming the uncertainty of the evaluated 2PTC frequency values $f_{osc}(T_0)$ and $f_{osc}(T_H)$, having the standard deviation $\sigma_f = 0/50/100/200$ ppm.

In summary, the proposed two–point temperature calibration (2PTC) method enables the estimation of the optimal temperature coefficient trim value based on the frequency measurement at only two temperatures. The choice of the two measurement temperatures is dependent on the oscillator design, process, noise, and measurement accuracy. Therefore, the optimal temperatures for a specific test–case should be determined experimentally. The method is applicable for the oscillators having a pronounced second–order behavior of the temperature characteristic and limited influence of the higher–order effects.

5.4 Simulation Results

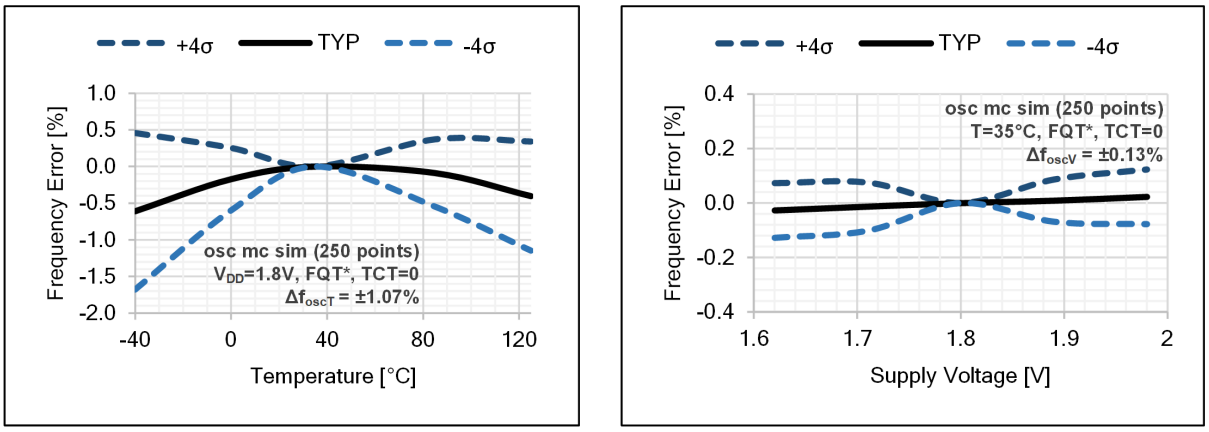
The prototype of the self–sustaining oscillator with replica chopped comparator core from Section 5.2.6 is simulated assuming the test setup described in Section 5.2.7. The oscillator consumes $P = 189.9$ µW ($I_{DD} = 105.5$ µA) at the nominal conditions ($T = 35°C$ and $V_{DD} = 1.8$ V), with the power breakdown of building blocks shown in Table 5.8. The average nominal frequency f_{osc0} (at $FQT = 0$) is around 2 MHz, having the process sensitivity of $\sigma(f_{osc0})/\mu(f_{osc0}) = 7.5\%$. The start–up time of the oscillator is $t_{startup} = 5.5$ µs.

Table 5.8: The power consumption breakdown of the oscillator building blocks.

Block	Power Consumption
Reference Generator	11.2%
Voltage to Current Converter	19.0%
Current Mirror	8.3%
Oscillator Core	61.5%

5.4.1 Temperature and Supply Variation

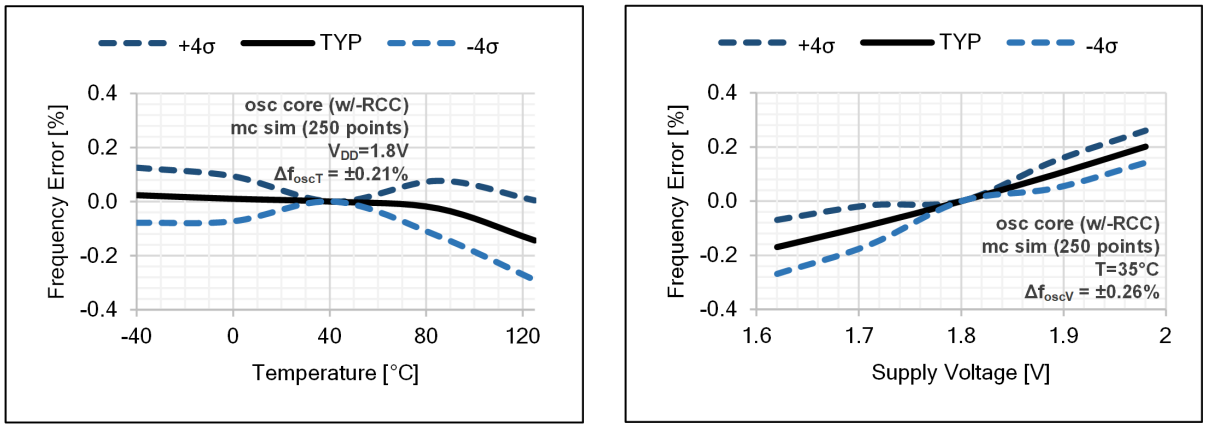
The simulated frequency variation of the proposed oscillator versus temperature and supply voltage is shown in Fig. 5.19. The simulations are performed on 250 Monte Carlo points using the optimal frequency trim code (FQT^*) and nominal temperature coefficient trim code ($TCT = 0$). The simulated frequency drift Δf_{oscT} versus temperature is from -1.68% to $+0.46\%$ in the temperature range from $-40°C$ to $125°C$. The simulated frequency drift Δf_{oscV} versus supply voltage is from -0.13% to $+0.12\%$ in the supply range from 1.62 V to 1.98 V.



(a) (b)

Figure 5.19: The simulated frequency error of the oscillator prototype vs. (a) temperature (at $V_{DD} = 1.8$ V) (b) supply voltage (at $T = 35°C$). The simulations are performed on 250 Monte Carlo points using the optimal frequency trim code (FQT^*) and untrimmed temperature coefficient ($TCT = 0$).

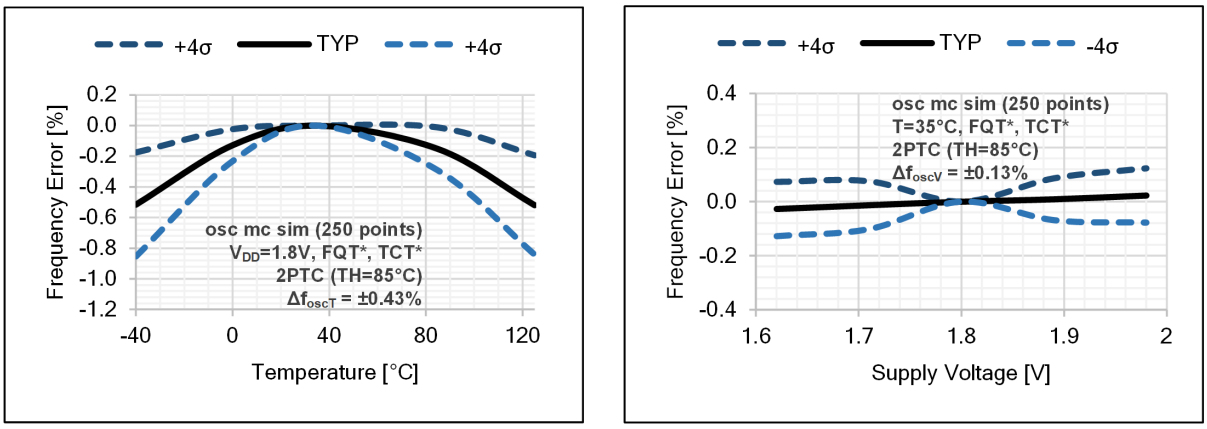
Next, the simulated frequency variation of the oscillator core with replica chopped comparator (excluding the other building blocks) versus temperature and supply voltage is shown in Fig. 5.20. The simulations are performed on 250 Monte Carlo points, assuming the test bench from Fig. 5.11. The simulated frequency drift Δf_{oscT} versus temperature is from -0.29% to $+0.13\%$ in the temperature range from $-40°$C to 125°C. Compared to the overall error shown in Fig. 5.19, this indicates that most of the error originates from the reference blocks of the oscillator. On the other hand, the simulated frequency drift Δf_{oscV} versus supply voltage is from -0.27% to $+0.25\%$ in the supply range from 1.62 V to 1.98 V. Compared to Fig. 5.19, the core is the primary contributor to the supply variation, where the standalone core also exhibits a systematic drift versus supply voltage that is eventually compensated in the overall design.



(a) (b)

Figure 5.20: The simulated frequency error of the oscillator core with replica chopped comparator vs. (a) temperature (at $V_{DD} = 1.8$ V) (b) supply voltage (at $T = 35°$C). The simulations are performed on 250 Monte Carlo points.

Finally, the simulated frequency variation of the temperature calibrated oscillator versus temperature is shown in Fig. 5.21. Here, the two–point temperature calibration (2PTC) method is applied, as described in Section 5.3.2. The optimal temperature coefficient trim code TCT^* is estimated from (5.64) and (5.65) with $T_0 = 35°$C and $T_H = 85°$C. The simulations are performed on 250 Monte Carlo points using the optimal frequency trim code FQT^*. The required range for the temperature coefficient trim code TCT over 250 Monte Carlo points is between -5 and $+4$. The simulated frequency drift Δf_{oscT} versus temperature is from -0.85% to $+0.0\%$ in the temperature range from $-40°$C to 125°C. This implies an improvement of more than two times ($\pm 0.43\%$ vs. $\pm 1.07\%$) compared to the case with the untrimmed temperature coefficient (Fig. 5.19). On the other hand, temperature calibration has a negligible effect on the frequency drift Δf_{oscV} versus supply voltage, ranging from -0.13% to $+0.13\%$ in the supply range from 1.62 V to 1.98 V.

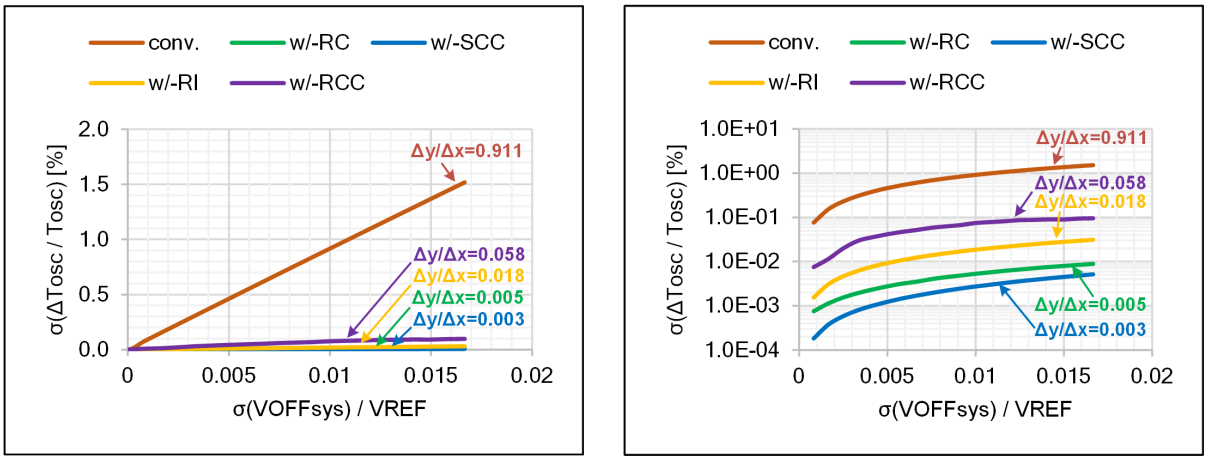


(a) (b)

Figure 5.21: The simulated frequency error of the temperature calibrated oscillator vs. (a) temperature (at $V_{DD} = 1.8$ V) (b) supply voltage (at $T = 35°C$). The optimal temperature coefficient trim code TCT^* is calculated using the 2PTC method. The simulations are performed on 250 Monte Carlo points using the optimal frequency trim code (FQT^*).

5.4.2 Sensitivity to Offset Voltage

Fig. 5.22 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the systematic offset voltage (V_{OFFsys}) for the proposed core with replica chopped comparator (w/–RCC). Here, the identical offset voltage of the two core comparators is assumed, with the standard deviation $\sigma(V_{OFFsys})$ ranging from 0 mV to 8.3 mV. The figure also includes the results for the four core architectures presented in previous chapters, namely the conventional oscillator core (conv.), core with replica comparators (w/–RC), core with self–compensating chopped comparator (w/–SCC), and core with replica integrator (w/–RI). As seen from the figure, the sensitivity of the proposed core (w/–RCC) is $S_{VOFFsys} = 0.058$, exhibiting the improvement

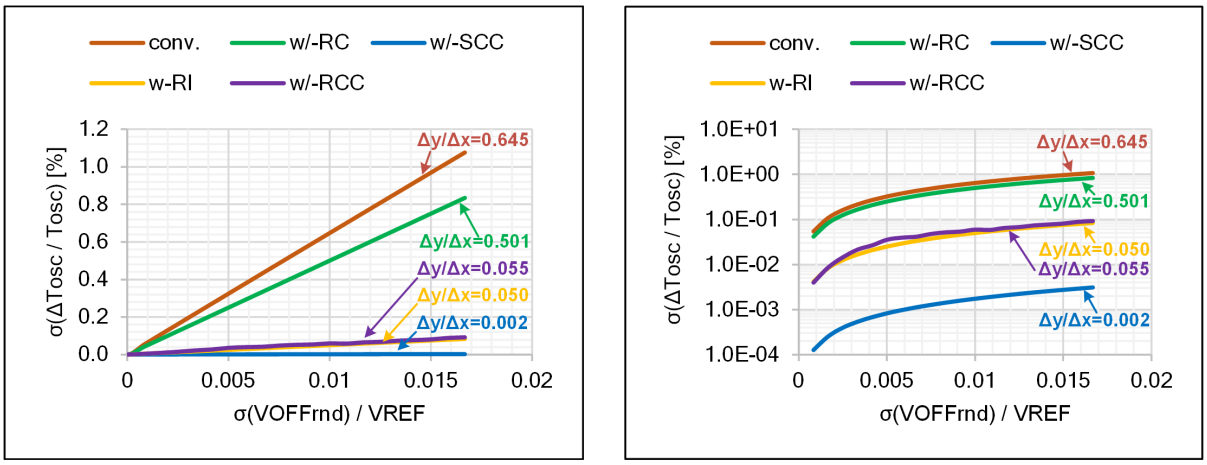


(a) (b)

Figure 5.22: The simulated sensitivity of the oscillation period to the systematic offset voltage, shown for five different oscillator cores (conv., w/–RC, w/–SCC, w/–RI, and w/–RCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

of more than ten times compared to the conventional core, at the same time being inferior to w/–RC, w/–SCC, and w/–RI cores.

Fig. 5.23 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the random offset voltage (V_{OFFrnd}) for the proposed core with replica chopped comparator (w/–RCC). Here, the offset voltage of the two core comparators is assumed independent, with the standard deviation $\sigma(V_{OFFrnd})$ ranging from 0 mV to 8.3 mV. The figure also includes the results of the four cores (conv, w/–RC, w/–SCC, and w/–RI) presented in previous chapters. As seen from the figure, the simulated sensitivity for the proposed core (w/–RCC) is $S_{VOFFrnd} = 0.055$, superior to the conventional and w/–RC core and nearly identical to the w/–RI core.



(a) (b)

Figure 5.23: The simulated sensitivity of the oscillation period to the random offset voltage, shown for five different oscillator cores (conv., w/–RC, w/–SCC, w/–RI, and w/–RCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

5.4.3 Sensitivity to Propagation Delay

Fig. 5.24 shows the relative sensitivity of the oscillation period ($\Delta T_{osc}/T_{osc}$) to the propagation delay of the comparator (t_d) for the proposed core with replica chopped comparator (w/–RCC). Here, the identical variation of the propagation delay is assumed for the two core comparators, with the standard deviation $\sigma(\Delta t_d)$ ranging from 0 ns to 25 ns. The figure also includes the results of the four cores (conv., w/–RC, w/–SCC, and w/–RI) presented in previous chapters. As seen from the figure, the simulated sensitivity for the proposed core (w/–RCC) is $S_{td} = 0.135$, indicating more than ten times the improvement compared to the conventional core. At the same time, the sensitivity is similar to the w/–RI core and inferior to w/–RC and w/–SCC cores.

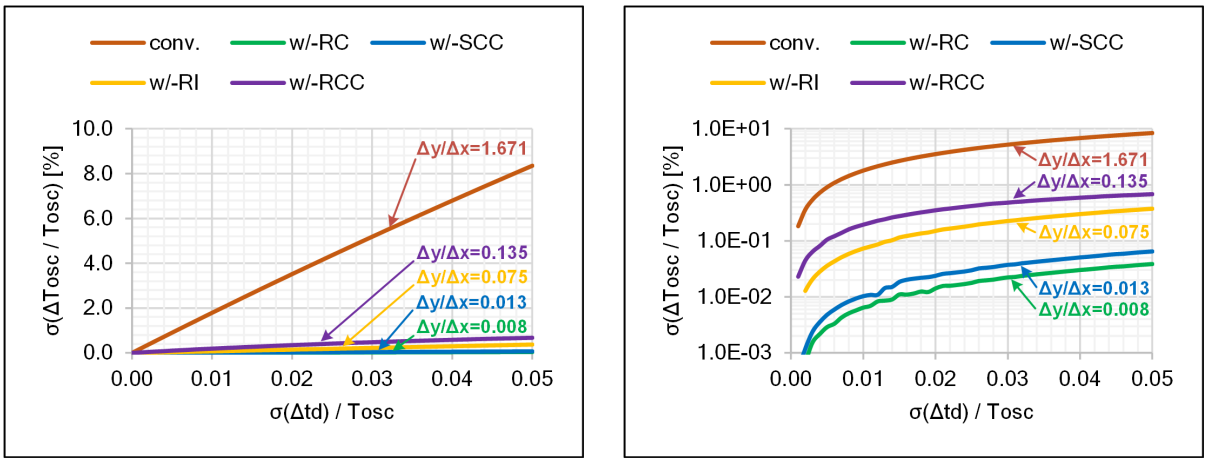


Figure 5.24: The simulated sensitivity of the oscillation period to the comparator delay, shown for five different oscillator cores (conv., w/–RC, w/–SCC, w/–RI, and w/–RCC) (a) plotted in linear scale (b) plotted in logarithmic scale.

5.4.4 Control Linearity

The response of the normalized output frequency f_{osc}/f_{osc0} to the normalized control current I_{REF}/I_{REF0} is simulated for the proposed oscillator core (w/–RCC) under the nominal conditions ($T = 35°\text{C}$ and $V_{DD} = 1.8$ V) on 50 Monte Carlo points. The results for the typical case are plotted in Fig. 5.25, also showing the comparison with the measurements of the conventional oscillator core (conv.), core with replica comparators (w/–RC), core with self–compensating chopped comparator (w/–SCC), and core with replica integrator (w/–RI).

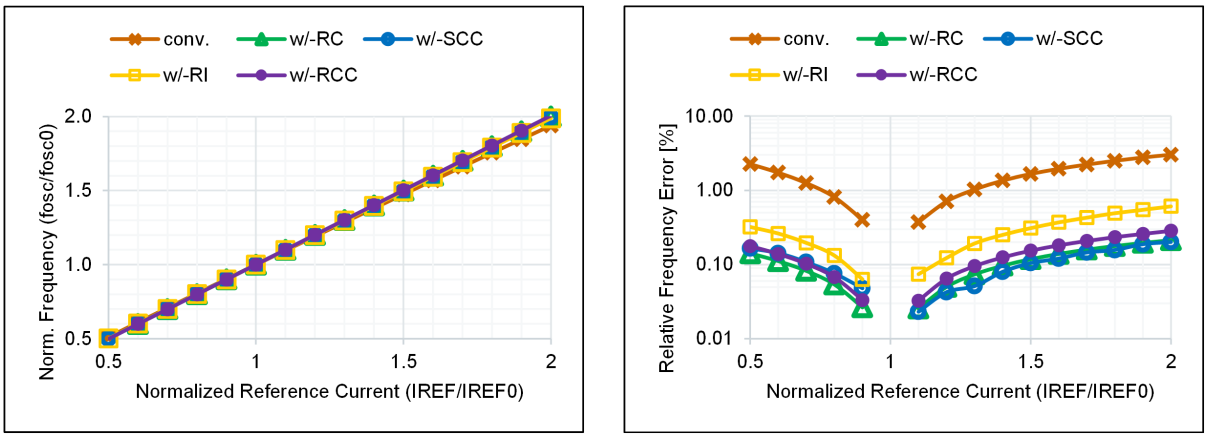
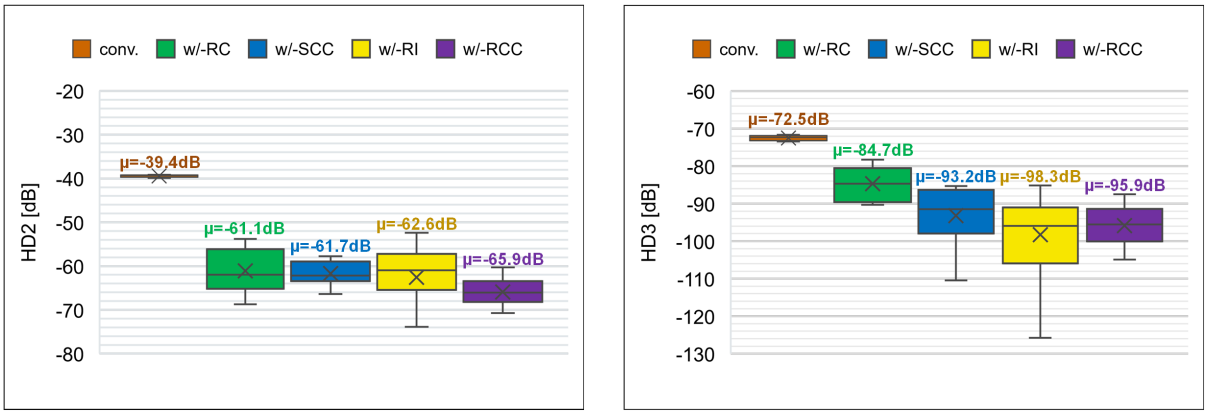


Figure 5.25: (a) The typical normalized frequency response vs. the normalized reference current, shown for five different oscillator cores (conv., w/–RC, w/–SCC, w/–RI, and w/–RCC). (b) The relative error of the normalized frequency (compared to the ideal case $y = x$) vs. the normalized reference current.

The distortion parameters HD_2 and HD_3 of the proposed core (w/–RCC) are calculated using (2.24) and (2.25) with $\Delta f_{osc} = 500$ kHz ($\Delta I_{REF}/I_{REF0} = 0.25$), having the mean values equal to $HD_2 = -65.9$ dB and $HD_3 = -95.9$ dB. The results of 50 simulated samples are

presented in Fig. 5.26, including the four cores (conv., w/–RC, w/–SCC, and w/–RI) presented in previous chapters. As seen from the figure, the proposed oscillator core (w/–RCC) exhibits superior linearity compared to the other cores, especially regarding the HD_2 parameter.



(a) (b)

Figure 5.26: The distortion parameters of the control characteristic, shown for five different oscillator cores (conv., w/–RC, w/–SCC, w/–RI, and w/–RCC) (a) HD_2 (b) HD_3. The distortion parameters are calculated for $\Delta f_{osc} = 500$ kHz.

5.5 Measurement Results

The prototype of the proposed self–sustaining oscillator with replica chopped comparator core, shown in Fig. 5.8, is manufactured in 180 nm CMOS technology with eight samples packaged for measurement. The nominal frequency f_{osc0} of the measured samples is around 2 MHz, having the process sensitivity of $\sigma(f_{osc0})/\mu(f_{osc0}) = 1.6\%$. The oscillators consume around $P = 185$ µW ($I_{DD} = 102.6$ µA) under the typical conditions ($T = 35°$C and $V_{DD} = 1.8$ V). The average measured period jitter is $\sigma_{Tosc} = 238$ ps (476 ppm).

5.5.1 Frequency Trimmed Oscillator Performance

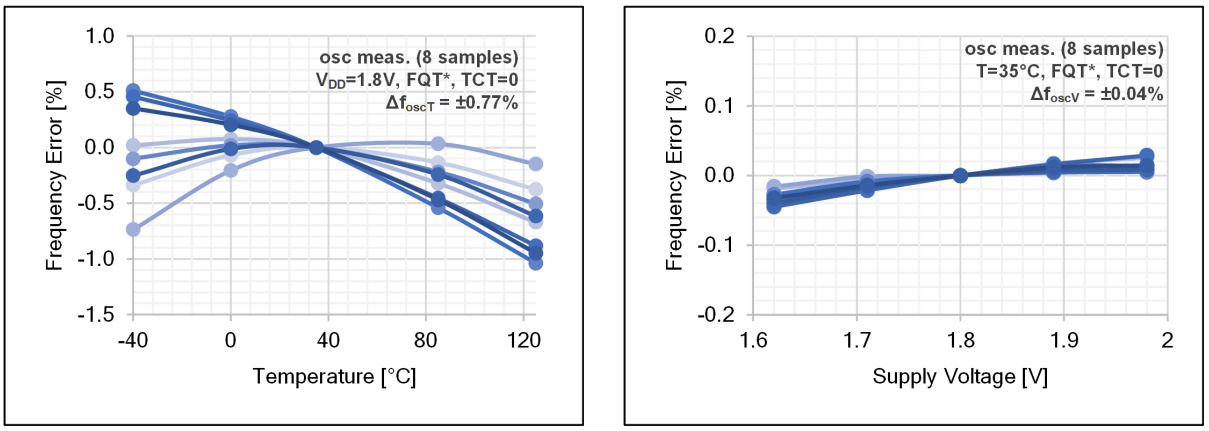
The performance measurements of the manufactured samples are performed over the entire temperature and power supply range, including the calibration of the center frequency with the optimal trim code FQT^* and using the nominal temperature coefficient trim code ($TCT = 0$). First, the output frequency f_{osc0} of each sample is measured at the nominal conditions. Next, the optimal trim code FQT^* is calculated and applied according to (5.57), trimming the oscillator to the frequency f^*_{osc0} under the nominal conditions. The detailed information on the frequency calibration of eight measured samples is shown in Table 5.9.

Table 5.9: The summary of the frequency calibration of eight measured oscillator samples.

Sample	f_{osc0} [MHz]	[a] FQT^*	f^*_{osc0} [MHz]
1	2.035	-2	2.003
2	2.038	-2	2.006
3	2.081	-5	2.000
4	1.973	2	2.004
5	2.025	-2	1.993
6	1.996	0	1.996
7	2.013	-1	1.997
8	2.003	0	2.003

[a] Calculated using (5.57).

The measured frequency variation of eight oscillator samples versus temperature and supply voltage is shown in Fig. 5.27. The measured frequency drift Δf_{oscT} versus temperature is from -1.03% to $+0.51\%$ in the temperature range from $-40°$C to 125°C. The measured frequency drift of the oscillator Δf_{oscV} versus supply voltage is from -0.05% to $+0.03\%$ in the supply range from 1.62 V to 1.98 V.



(a) (b)

Figure 5.27: The measured frequency error of the manufactured oscillator prototype vs. (a) temperature (at $V_{DD} = 1.8$ V) (b) supply voltage (at $T = 35°C$). The measurements are performed on eight test chip samples using the optimal frequency trim code (FQT^*) and untrimmed temperature coefficient ($TCT = 0$).

5.5.2 Temperature Trimmed Oscillator Performance

Along with the frequency calibration of the oscillator prototype, the manufactured samples are additionally calibrated over the temperature using the two–point temperature calibration (2PTC) method. First, the output frequency of each sample is measured at two temperatures, specifically $T_0 = 35°C$ and $T_H = 85°$. Next, the optimal trim code TCT^* is estimated from (5.64) and (5.65) and applied for each sample, significantly reducing the measured frequency drift versus temperature. Table 5.10 shows the detailed information of the performed 2PTC

Table 5.10: The summary of the two–point temperature calibration on 8 measured oscillator samples.

Sample	[a] $\Delta TC1_f^*$ [ppm/°C]	[b] $\Delta TC1'_f$ [ppm/°C]	[c] TCT^*	Post-Trim Error [ppm/°C]
1	2.4	27.1	0	-2.4
2	41.7	64.4	2	-1.7
3	-35.6	-6.5	-2	-4.4
4	24.5	43.8	1	-4.5
5	93.9	108.3	5	6.1
6	81.1	90.9	4	-1.1
7	22	48.4	1	-2
8	78.7	94	4	1.3

[a] Calculated using (5.58).
[b] Calculated using (5.61).
[c] Calculated using (5.64) and (5.65).

method. Also, Fig. 5.28 shows the scatter diagram between the optimal temperature coefficient trim value $\Delta TC1_f^*$ (evaluated over the entire temperature range) and the two–point measurement variable $\Delta TC1'_f$, strongly corresponding to the simulation results from Fig. 5.16.

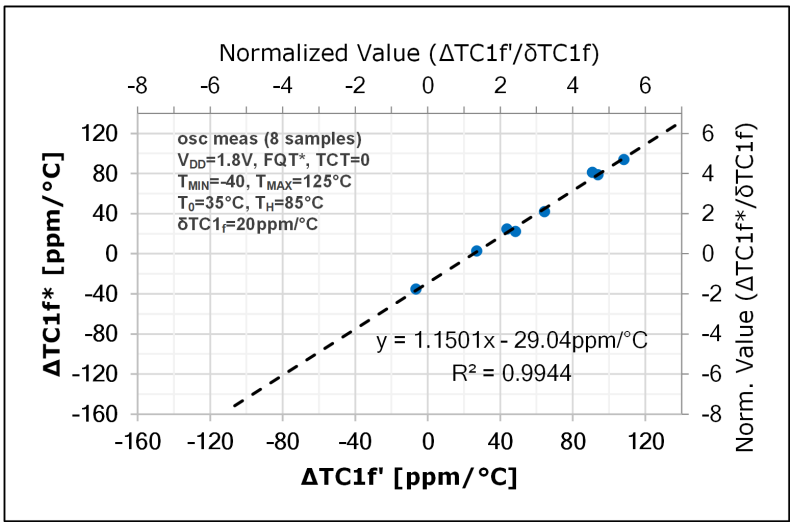
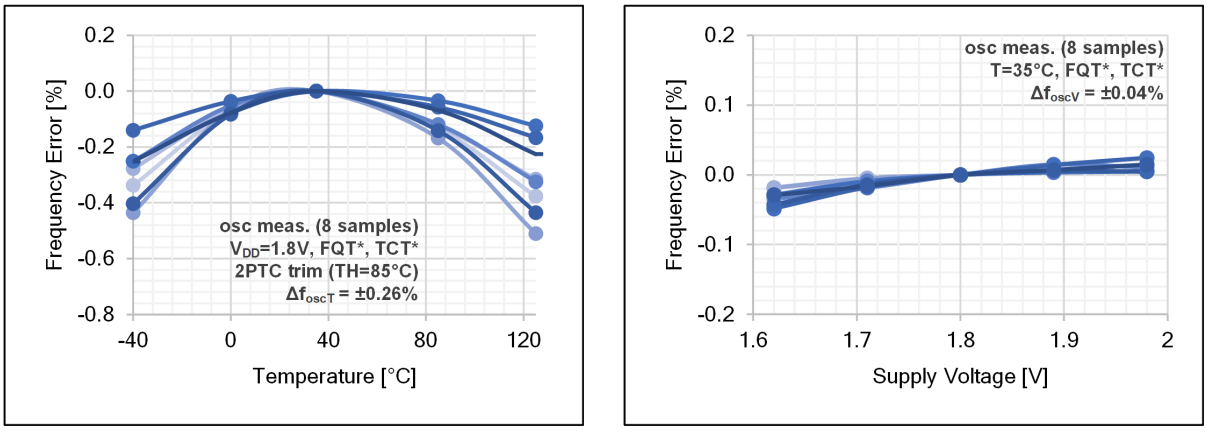


Figure 5.28: The measurement of the optimal temperature coefficient trim value $\Delta TC1_f^*$ plotted vs. two–point measurement variable $\Delta TC1'_f$ calculated using the 2PTC method.

Finally, the measured frequency variation of the temperature calibrated oscillator versus temperature is shown in Fig. 5.29. The measured frequency drift Δf_{oscT} versus temperature is from -0.51% to $+0.0\%$ in the temperature range from $-40°$C to 125°C, implying an improvement of almost three times ($\pm 0.26\%$ vs. $\pm 0.77\%$) compared to the case with the untrimmed temperature coefficient (Fig. 5.27). Meanwhile, temperature calibration has a negligible effect on the frequency drift Δf_{oscV} versus supply voltage, again ranging from -0.05% to $+0.03\%$ in the supply range from 1.62 V to 1.98 V.



(a) (b)

Figure 5.29: The measured frequency error of the temperature calibrated oscillator vs. (a) temperature (at $V_{DD} = 1.8$ V) (b) supply voltage (at $T = 35°$C). The optimal temperature coefficient trim code TCT^* is calculated using the 2PTC method. The measurements are performed on eight test chip samples trimmed using the optimal frequency trim code (FQT^*).

5.6 Summary

This chapter has introduced the architecture of the full on–chip relaxation oscillator with a trimmable first–order temperature coefficient. The oscillator prototype uses the novel relaxation oscillator core architecture with replica chopped comparator. Eight prototype samples have been manufactured in 180 nm technology and experimentally verified, each occupying 0.075 mm^2, having a nominal frequency $f_{osc0} = 2$ MHz, and typically consuming around $I_{DD} = 103$ µA at 1.8 V supply. The measured frequency drift is $\pm 0.77\%$ in the temperature range from -40°C to 125°C and $\pm 0.04\%$ in the supply range from 1.62 V to 1.98 V. The design and performance overviews are shown in Table 5.11 for the proposed oscillator core (standalone) and in Table 5.12 for the self–sustaining oscillator prototype.

Furthermore, the two–point temperature calibration (2PTC) method was introduced and described in detail. The method estimates the optimal temperature coefficient trim value based on only two temperature measurements, thus offering a cost–efficient way for temperature calibration in high–volume production. The demonstration of the 2PTC method on the prototype samples resulted in a threefold reduction of the frequency drift versus temperature, where the optimal temperature trim code was correctly predicted for all samples.

Table 5.11: The design and peformance summary of the relaxation oscillator core with replica chopped comparator (w/–RCC) – simulation results.

Parameter	Description	Value	Unit	Conditions
	Technology	180	nm	
A	Area	0.021	mm^2	
f_{osc0}	Nominal Frequency	2	MHz	nominal
P	Power	116.8	µW	nominal
V_{DD}	Supply Voltage	1.8	V	
Δf_{oscT}	Drift vs. Temperature	± 0.21	%	$T = -40 \sim 125$°C
Δf_{oscV}	Drift vs. Supply	± 0.26	%	$V_{DD} = 1.62 \sim 1.98$ V
$t_{startup}$	Start–Up Time	0.25	µs	nominal
σ_{Tosc}	Period Jitter	320	ppm	nominal
HD_2/HD_3	Distortion Parameters	–65.9/–95.9	dB	$\Delta f_{osc} = 500$ kHz
$S_{VOFFsys}$	Sensitivity to Syst. Offset Volt.	0.058	$1/V_{REF}$	nominal
$S_{VOFFrnd}$	Sensitivity to Random Offset Volt.	0.055	$1/V_{REF}$	nominal
S_{td}	Sensitivity to Propagation Delay	0.135	$1/T_{osc}$	nominal

Table 5.12: The design and peformance summary of the oscillator prototype – measurement results.

Parameter	Description	Value	Unit	Conditions
	Technology	180	nm	
A	Area	0.075	mm^2	
f_{osc0}	Frequency	2	MHz	nominal
P	Power	185	µW	nominal
V_{DD}	Supply Voltage	1.8	V	
Δf_{oscT}	Drift vs. Temperature	$\pm 0.77/\pm$[a]0.26	%	$T = -40 \sim 125^{\circ}C$
Δf_{oscV}	Drift vs. Supply	± 0.04	%	$V_{DD} = 1.62 \sim 1.98$ V
$t_{startup}$	Start–Up Time	5.5	µs	nominal
σ_{Tosc}	Period Jitter	476	ppm	nominal

[a]Temperature calibrated using two–point measurement.

Chapter 6

Conclusion

6.1 Overview of Proposed Core Architectures

Table 6.1 shows the comparison of the conventional (conv.) and four proposed relaxation oscillator cores, namely the core with replica comparators (w/–RC), core with self–compensating chopped comparator (w/–SCC), core with replica integrator (w/–RI), and core with replica chopped comparator (w/–RCC). The table lists the relevant design parameters (process option, chip area, operating frequency, power consumption, and supply voltage) and the simulated performance figures (accuracy, control linearity, noise, and sensitivity to comparator non–idealities).

Table 6.1: The comparison of the conventional relaxation oscillator core (conv.), oscillator core with replica comparators (w/–RC), self–compensating oscillator core with chopped comparator (w/–SCC), oscillator core with replica integrator (w/–RI), and oscillator core with replica chopped comparator (w/–RCC).

Parameter	conv.	w/–RC	w/–SCC	w/–RI	w/–RCC	Unit
Technology	350	350	350	110	180	nm
Area	0.03	0.04	0.032	0.045	0.021	mm^2
Frequency	0.85	1	1	2	2	MHz
Power	150	210	160	39.6	116.8	µW
Supply	3.3	3.3	3.3	1.2	1.8	V
Drift vs temperature[a]	±1.92[b]	±0.93[b]	±0.71[b]	±0.5[b]	±0.21[b]	%
Drift vs supply[a]	±0.72[c]	±0.52[c]	±0.36[c]	±0.33[d]	±0.26[e]	%
Start–up time	0.6	0.5	0.5	0.25	0.25	µs
Energy/cycle	176	210	160	19.8	58.4	pJ
FoM	80.7	83.3	88.2	84.7	92.0	dB
HD_2	–39.4	–61.1	–61.7	–62.6	–65.9	dB
HD_3	–72.5	–84.7	–93.2	–98.3	–95.9	dB
RMS period jitter	195	230	235	1100	320	ppm
Phase noise @10kHz	–95	–93	–92	NA	NA	dBc/Hz
Allan deviation floor	12	13	15	NA	NA	ppm
Sensitivity to V_{OFFsys}	0.911	0.005	0.003	0.018	0.058	$1/V_{REF}$
Sensitivity to V_{OFFrnd}	0.645	0.501	0.002	0.050	0.055	$1/V_{REF}$
Sensitivity to t_d	1.671	0.008	0.013	0.075	0.135	$1/T_{osc}$

[a] 4σ significance.
[b] @–40°C∼125°C.
[c] @3.0∼4.5 V.
[d] @1.08∼1.32 V.
[e] @1.62∼1.98 V.

The figure–of–merit (FoM) [17] used for the performance comparison is defined as

$$FoM\ [\text{dB}] = 10log\left(\frac{f_{osc}\ [\text{MHz}]\cdot L_{min}\ [\text{nm}]}{P\ [\mu\text{W}]\cdot TC\ [\frac{\pm\text{ppm}}{^{\circ}\text{C}}]\cdot LS\ [\frac{\pm\text{ppm}}{\text{mV}}]\cdot A\ [\text{mm}^2]}\right), \tag{6.1}$$

taking into account the frequency (f_{osc}), process node (L_{min}), area (A), power (P), temperature coefficient (TC), and line sensitivity (LS).

As shown in Table 6.1, the proposed cores operate at the frequency of 1 MHz (w/–RC and w/–SCC) and 2 MHz (w/–RCC and w/–RI), all having a relatively small area (< 0.05 mm^2). Specifically, the w/–SCC core, manufactured in 0.35–µm technology, has a minimal area and power overhead relative to the benchmark conventional core. However, the power efficiency figure of 0.35–µm architectures (w/–RC and w/–SCC) is lower than the designs in smaller processes (w/–RI and w/–RCC), primarily because of the considerably higher supply voltage (3.3 V). Furthermore, on top of a greatly improved control linearity, all proposed cores show improved frequency accuracy over temperature and supply voltage. The advancements are particularly noticeable for the w/–SCC and w/–RCC cores, as reflected in their superior figure–of–merit. Likewise, the start–up time of the cores is not compromised with the circuit modifications, always requiring only one half–cycle for a settled frequency (assuming the settled voltage and current references). The proposed cores are comparable in terms of noise, having the period jitter in the $200 \sim 300$ ppm range, except for the w/–RI core, which has a more pronounced noise figure due to low reference voltage and smaller process. The sensitivity to the delay and offset are also significantly improved in all cores, especially for the w/–SCC core.

Conclusively, the choice of an appropriate oscillator core varies depending on the system requirements. For instance, the w/–RC core does not contain a chopper element, and accordingly, it is suitable for applications having the supply line sensitive to excessive switching activities. On the other hand, considering the chopped comparator core architectures, w/–RCC is featured with better signal integrity than w/–SCC and, therefore, more suitable at higher frequencies, while the w/–RI core is developed for reliable operation at lower supply conditions and smaller process nodes.

6.2 Comparison of Published RC Oscillators

The comparison of relevant published works on RC oscillator architectures is shown in Table 6.2, including the design and performance figures, namely the used process node, area, operating frequency and supply voltage, power, temperature coefficient (TC), line sensitivity (LS), energy per cycle (E/cyc), figure–of–merit (FoM) from (6.1), and the start–up time.

Relaxation oscillators with integrated error feedback (IEF), reported in [1–5], perform considerably well at relatively high frequencies ($>$ 10 MHz) with reasonable power consumption ($<$ 100 µW) but may suffer from a longer start–up time needed for loop stabilization. Similarly, [6, 7] present the implementations where the relaxation oscillator is stabilized using a digital compensation loop (DCL). In [8, 9], chopped comparator architectures are used to cancel the offset voltage of the comparator while being susceptible to propagation delay. Likewise, self–clocked offset–cancellation scheme reported in [10] removes the influence of the offset, also having beneficial effects in terms of low–frequency noise. Next, the solutions combining a low–power operation with decent performance were proposed in [11–16], achieved with replica circuitry [11, 12] and current–mode comparator architectures [13–16]. Also, [17] demonstrated the operation of a relaxation oscillator up to 200°C while the improved noise figure was reported in [20–22], in both cases, without a significant loss in performance. In [23], the oscillator's accuracy was enhanced by implementing a programmable switch array (PSA) to compensate for the temperature drift of a reference resistor. On the other hand, the FLL–based closed–loop clock generators presented in [26–30], similar to the IEF closed–loop oscillators, are capable of oscillating at higher frequencies ($>$ 10 MHz). Combined with the temperature calibration [26–28] and voltage regulation [26, 27, 30], these architectures can deliver an exceptional performance at the price of considerable cost–overhead due to the increase in area and the necessity for low–temperature measurements. Furthermore, compared to the relaxation oscillators, ring oscillators may achieve substantially higher frequencies ($>$ 100 MHz) with lower frequency accuracy (around 10%) [48]. Also, in [49], an implementation of a ring oscillator running at 7 MHz with sub–1% temperature dependency was presented, requiring a power–hungry voltage regulator to keep the voltage sensitivity at a reasonable level.

Finally, the table also includes the design and performance summary of the 2–MHz oscillator prototype presented in Chapter 5. The temperature dependency of the output frequency ($\pm$46.7 ppm/°C), caused mainly by the reference blocks, is significantly improved with the proposed two–point temperature calibration, specifically to $\pm$15.8 ppm/°C. Moreover, the oscillator prototype is featured with a relatively small area (0.075 mm^2) and exceptional line sensitivity ($\pm$1.1 ppm/mV) compared to the reported oscillators without a voltage regulation.

Table 6.2: The performance comparison of published on–chip RC oscillators.

Ref	Year	Tech. [nm]	Area [mm^2]	Freq. [MHz]	Power [µW]	V_{DD} [V]	TC [$\frac{\pm ppm}{°C}$]	LS [$\frac{\pm ppm}{mV}$]	E/cyc [pJ]	FoM [dB]	Start time
[1]	2013	65	0.010	12.6	98.4	1.2	103	1.8	7.8	96.7	NA
[2]	2010	180	0.040	14.0	45.0	1.8	11.5	8.0	3.2	101.8	10µs
[3]	2016	180	0.032	13.5	48.8	1.8	33.3	5.0	3.6	99.7	NA
[4]	2017	90	0.027	51.3	18.0	0.8	10.8	13.3	0.4	108.2	150cyc
[5]	2014	180	0.013	32.8	16.6	1.5	67.0	1.3	0.5	115.0	5µs
[6]	2016	180	0.012	12.77	56.2	0.9	26.7	5.0	4.4	104.1	NA
[7]	2019	180	0.100	0.943	5.2	0.9	63.6	21.9	5.5	83.7	NA
[8]	2016	65	0.032	0.0185	0.13	1.0	42.3	25.0	7.0	84.4	4cyc
[9]	2009	65	0.110	0.1	41.0	1.2	93.5	3.7	410	66.2	NA
[10]	2009	130	0.073	3.2	38.4	1.5	62.5	20.0	12.0	80.7	NA
[11]	2012	90	0.120	0.1	0.28	0.8	52.3	46.9	2.8	80.4	1cyc
[12]	2013	180	0.105	0.0325	0.47	1.0	60.0	5.5	14.5	85.6	108µs
[13]	2013	180	0.075	1.1	0.859	1.8	50.0	15.0	0.8	96.1	NA
[14]	2015	180	0.030	0.122	0.014	0.6	163	29.2	0.1	100.4	NA
[15]	2010	350	0.100	0.0033	0.011	1.0	250	11.7	3.3	85.6	NA
[16]	2012	60	0.048	0.0328	4.48	1.6	8.3	0.6	137	92.4	NA
[17]	2013	130	0.007	1.0	428	2.5	54.0	10.9	428	78.7	NA
[20]	2020	180	0.015	10.5	220	1.4	68.5	22.0	20.9	85.8	NA
[21]	2019	180	0.058	0.445	21.3	1.8	113	0.4	47.9	92.2	NA
[22]	2019	180	0.028	8.2	46.3	1.0	61.5	45.5	5.6	86.1	NA
[23]	2013	350	0.162	0.13	3.7	1.5	41.7	2.0	28.5	89.6	NA
[26]	2022	65	0.180	32	34.0	1.2	[a]4.2	[b]0.04	1.1	122.8	NA
[27]	2018	180	0.170	24	200	1.8	[a]7.4	[b]0.05	8.3	115.7	2µs
[28]	2020	180	0.300	16	400	1.8	[a]3.1	0.6	25.0	101.0	NA
[29]	2009	350	0.080	30	180	1.8	50.0	20.0	6.0	88.6	2.5µs
[30]	2009	180	0.220	10	80.0	1.2	28.6	[b]0.3	8.0	101.1	NA
[48]	2010	180	0.004	130	2740	1.8	499	150	21.1	74.6	NA
[49]	2006	250	[c]1.60	7.0	1500	2.4	50.9	[b]8.9	214	62.1	NA
This	2023	180	0.075	2.0	185	1.8	46.7 [d]15.8	1.1	92.5	87.0 [d]91.7	5.5µs

[1] 0∼80°C; 1.1∼1.5V [2] -40∼125°C; 1.7∼1.9V [3] -30∼120°C; 1.5∼2.1V [4] -20∼100°C; 0.8∼1.2V [5] -40∼85°C; 1.5∼3.6V [6] -30∼120°C; 0.6∼1.1V [7] -10∼100°C; 0.8∼1.5V [8] -40∼90°C; 0.95∼1.05V [9] -22∼85°C; 1.12∼1.39V [10] 20∼60°C; 1.4∼1.6V [11] -40∼90°C; 0.725∼0.9V [12] -40∼100°C; 1∼1.8V [13] -20∼80°C; 1.2∼2.4V [14] -20∼100°C; 0.6∼1.8V [15] -20∼80°C; 1∼2.5V [16] -20∼100°C; 1.6∼3.2V [17] 25∼200°C; 2∼3V [20] -40∼125°C; 1.4∼2V [21] -20∼100°C; 1.2∼2.8V [22] -20∼100°C; 0.75∼0.95V [23] -20∼100°C; 1∼3V [26] -40∼85°C; 1.1∼2.3V [27] -40∼150°C; 1.8∼5V [28] -45∼85°C; 1.6∼2V [29] -20∼100°C; 1.8∼3V [30] -20∼120°C; 1.2∼3V [48] 0∼100°C; 1.62∼1.98V; [49] -40∼125°C; 2.4∼2.75V
This work -40∼125°C; 1.62∼1.98V

[a] Temperature calibrated.
[b] Regulated supply voltage.
[c] Pads included.
[d] Temperature calibrated using 2PTC method.

6.3 Outcomes of the Dissertation

The research on fully–integrated RC oscillators was conducted within this thesis, having an emphasis on the implementations based on relaxation oscillators. The implications of the propagation delay and offset voltage of the comparator stage were analyzed in detail, being the two most important sources of the frequency drift in the conventional relaxation oscillator core.

Accordingly, four improved core architectures were proposed within the thesis, namely the oscillator core with replica comparators, self–compensating oscillator core with chopped comparator, oscillator core with replica integrator, and oscillator core with replica chopped comparator. A core prototype was designed for each proposed core architecture and evaluated with simulations and measurements. Here, it was demonstrated that the cancellation of the propagation delay and offset voltage of the comparator stage significantly improves the temperature and supply dependency of a core, hence reducing the overall frequency drift to the sub–1% range. The proposed cores retain the beneficial properties of the relaxation oscillators, such as fast start–up, compatibility with wide temperature and supply voltage range, high tuning linearity, low implementation cost, and scalability in terms of power consumption and operating frequency. Therefore, having improved performance and compatibility with full–scale integration, the proposed cores are suitable for a wide range of industrial applications.

Furthermore, a temperature calibration method for further reduction of an oscillator's temperature dependency was presented in this thesis. Specifically, the method requires frequency measurements at two temperatures and estimates an oscillator's assumed second-order temperature characteristic. Most importantly, the choice of the measurement temperatures is arbitrary, thereby avoiding the measurements below room temperature and limiting the cost overhead incurred by the additional temperature measurement. Eventually, the proposed temperature calibration method was demonstrated on a manufactured oscillator.

Conclusively, this thesis has presented novel oscillator cores highly adaptable in various SoC applications, significantly improving clock accuracy while minimally affecting the system's complexity. Likewise, the presented temperature calibration method may further increase the performance of the proposed clock references.

Appendix A

Analysis of Comparator Non–Idealities

A.1 Offset Voltage

A.1.1 Systematic Offset Voltage

The systematic offset voltage of a comparator assumes the absence of any mismatch effects on the devices, and it is determined exclusively by the process variations at a given supply voltage and temperature. Specifically, for the comparators in Fig. 2.3, the systematic offset voltage originates from the imbalance in the currents of the matched and identically designed devices due to the channel length modulation effect.

First, to express the systematic offset voltage of the comparators analytically, the equation for the drain current I_D of a MOS transistor in the strong inversion region is considered, specifically [59]

$$I_D = K_T (V_{GS} - V_{th})^2 \left[1 + \lambda (V_{DS} - V_{GS} + V_{th})\right], \tag{A.1}$$

where V_{GS} is the gate–source voltage, V_{th} is the threshold voltage, V_{DS} is the drain–source voltage, and λ is the output impedance constant. Also, K_T is the current factor, determined by the technology and design parameters, specifically

$$K_T = \frac{\mu_c C_{ox}}{2} \cdot \frac{W}{L}, \tag{A.2}$$

where μ_c is the mobility of the carrier charges, C_{ox} is the oxide capacitance per unit area, and W and L are the channel width and length of the corresponding transistor. Furthermore, using (A.1), the difference in currents between the two otherwise identical transistors under the different drain–source voltage V_{DS} conditions can be expressed as [59]

$$\Delta I_D = I_D \cdot \lambda \cdot \Delta V_{DS}, \tag{A.3}$$

where ΔI_D is the current difference ($\Delta I_D = I_{D2} - I_{D1}$) and ΔV_{DS} is the difference in drain–source voltages ($\Delta V_{DS} = V_{DS2} - V_{DS1}$). Also considering the definition of the dynamic resistance, specifically

$$r_{ds} = \frac{1}{\lambda I_D}, \tag{A.4}$$

(A.3) can be expressed as

$$I_{D2} - I_{D1} = \frac{V_{DS2} - V_{DS1}}{r_{ds}}. \tag{A.5}$$

Accordingly, for the comparator with nMOS input pair from Fig. 2.3a, the following equations are valid for the three current mirrors, in particular,

$$I_{D,P3} - I_{D,P1} = \frac{V_{GS,N3} - V_{DD} - V_{GS,P1}}{r_{ds,P3}} \tag{A.6}$$

for the current mirror with M_{P1} and M_{P3},

$$I_{D,P4} - I_{D,P2} = \frac{-½V_{DD} - V_{GS,P2}}{r_{ds,P4}} \tag{A.7}$$

for the current mirror with M_{P2} and M_{P4}, and

$$I_{D,N4} - I_{D,N3} = \frac{½V_{DD} - V_{GS,N3}}{r_{ds,N4}} \tag{A.8}$$

for the current mirror with M_{N3} and M_{N4}, under the assumption that the inverter threshold voltage is $½V_{DD}$. On the other hand, for the considered OTA, the differential input transistors M_{N1} and M_{N2} are symmetrically loaded ($V_{GS,N1} \approx V_{GS,N2}$) and therefore do not contribute to the systematic offset voltage. Therefore, considering (A.6)–(A.8), the overall current imbalance at the output node due to the channel length modulation effect can be expressed as

$$\Delta I_{OUT} = (I_{D,P3} - I_{D,P1}) - (I_{D,P4} - I_{D,P2}) - (I_{D,N4} - I_{D,N3}), \tag{A.9}$$

or specifically

$$\Delta I_{OUT} = \frac{(V_{GS,N3} - V_{DD}) - V_{GS,P1}}{r_{ds,P3}} - \frac{-½V_{DD} - V_{GS,P2}}{r_{ds,P4}} - \frac{½V_{DD} - V_{GS,N3}}{r_{ds,N4}}. \tag{A.10}$$

Assuming a proper matching of the mirror transistors, the following approximations are made:

$$V_{GS,P1} \approx V_{GS,P2} \tag{A.11}$$

and

$$r_{ds,P3} \approx r_{ds,P4}. \tag{A.12}$$

This eventually leads to

$$\Delta I_{OUT} = (V_{GS,N3} - ½V_{DD}) \left(\frac{1}{r_{ds,N4}} + \frac{1}{r_{ds,P4}} \right). \tag{A.13}$$

Finally, the expression for the systematic offset voltage V_{OFFsys} is calculated by dividing the output current imbalance ΔI_{OUT} with the transconductance of the differential input transistors $g_{m,dp}$ [58], specifically

$$V_{OFFsys} = \frac{\Delta I_{OUT}}{g_{m,dp}} = \frac{V_{GS,N3} - ½V_{DD}}{g_{m,dp}(r_{ds,N4} || r_{ds,P4})}. \tag{A.14}$$

Similarly, for the comparator with pMOS input pair from Fig. 2.3b, the following equations

are valid for the three current mirrors, in particular,

$$I_{D,N3} - I_{D,N1} = \frac{V_{GS,P3} + V_{DD} - V_{GS,N1}}{r_{ds,N3}} \tag{A.15}$$

for the current mirror with M_{N1} and M_{N3},

$$I_{D,N4} - I_{D,N2} = \frac{½V_{DD} - V_{GS,N2}}{r_{ds,N4}} \tag{A.16}$$

for the current mirror with M_{N2} and M_{N4}, and

$$I_{D,P4} - I_{D,P3} = \frac{-½V_{DD} - V_{GS,P3}}{r_{ds,P4}} \tag{A.17}$$

for the current mirror with M_{P3} and M_{P4}, under the assumption that the inverter threshold voltage is $½V_{DD}$. On the other hand, for the considered OTA, the differential input transistors M_{P1} and M_{P2} are symmetrically loaded ($V_{GS,P1} \approx V_{GS,P2}$) and therefore do not contribute to the systematic offset voltage. Therefore, considering (A.15)–(A.17), the overall current imbalance at the output node due to the channel length modulation effect can be expressed as

$$\Delta I_{OUT} = (I_{D,N3} - I_{D,N1}) - (I_{D,N4} - I_{D,N2}) - (I_{D,P4} - I_{D,P3}), \tag{A.18}$$

or specifically

$$\Delta I_{OUT} = \frac{V_{GS,P3} + V_{DD} - V_{GS,N1}}{r_{ds,N3}} - \frac{½V_{DD} - V_{GS,N2}}{r_{ds,N4}} - \frac{-½V_{DD} - V_{GS,P3}}{r_{ds,P4}}. \tag{A.19}$$

Assuming a proper matching of the mirror transistors, the following approximations are made:

$$V_{GS,N1} \approx V_{GS,N2} \tag{A.20}$$

and

$$r_{ds,N3} \approx r_{ds,N4}. \tag{A.21}$$

This eventually leads to

$$\Delta I_{OUT} = (V_{GS,P3} + ½V_{DD}) \left(\frac{1}{r_{ds,N4}} + \frac{1}{r_{ds,P4}} \right). \tag{A.22}$$

Finally, the expression for the systematic offset voltage V_{OFFsys} is calculated by dividing the output current imbalance ΔI_{OUT} with the transconductance of the differential input transistors $g_{m,dp}$, specifically

$$V_{OFFsys} = \frac{\Delta I_{OUT}}{g_{m,dp}} = \frac{V_{GS,P3} + ½V_{DD}}{g_{m,dp}(r_{ds,N4} || r_{ds,P4})}. \tag{A.23}$$

A.1.2 Random Offset Voltage

Contrary to the systematic offset voltage, the random offset voltage is primarily mismatch–related [58]. Here, random variations of each device, unique for every sample, contribute to the current imbalance within a comparator. Considering the MOS transistor equation for strong inversion (A.1), the difference between two identical, closely spaced MOS transistors can be observed primarily as the threshold voltage difference (ΔV_{th}) and current factor difference (ΔK_T) [65]. Here, ΔK_T and ΔV_{th} depend on the mismatch proportionality parameters (A_{KT} and A_{Vth}) and the overall device area ($W \times L$), specifically

$$\sigma^2\left(\frac{\Delta K_T}{K_T}\right) = \frac{A_{KT}^2}{WL} \tag{A.24}$$

and

$$\sigma^2\left(\Delta V_{th}\right) = \frac{A_{Vth}^2}{WL}. \tag{A.25}$$

Differentiating (A.1) with respect to K_T and V_{th}, also neglecting the channel length modulation, leads to the following expression:

$$dI_D = (V_{GS} - V_{th})^2 dK_T - 2K_T(V_{GS} - V_{th})dV_{th}. \tag{A.26}$$

Hence, for relatively small changes in the current factor (ΔK_T) and threshold voltage (ΔV_{th}), the expression for the current difference ΔI_D relative to a mismatch–free transistor is

$$\Delta I_D = (V_{GS} - V_{th})^2 \Delta K_T - 2K_T(V_{GS} - V_{th})\Delta V_{th}. \tag{A.27}$$

Moreover, (A.27) can be rewritten as

$$\Delta I_D = \frac{I_D}{K_T}\Delta K_T - g_m \Delta V_{th}, \tag{A.28}$$

where g_m is the transconductance, specifically $g_m = 2K_T(V_{GS} - V_{th})$. On the other hand, the current difference ΔI_D in weak inversion is dominated by the threshold voltage difference ΔV_{th} [59, 60], implying

$$\Delta I_D = -g_m \Delta V_{th}. \tag{A.29}$$

The current difference ΔI_D represents the contribution of each device to the imbalance of the OTA, eventually reflected as an input–referred offset voltage. Since ΔK_T and ΔV_{th} are independent random variables, the variance of the current difference for each device can be expressed as

$$\sigma^2\left(\Delta I_D\right) = I_D^2 \sigma^2\left(\frac{\Delta K_T}{K_T}\right) + g_m^2 \sigma^2\left(\Delta V_{th}\right) \tag{A.30}$$

for the strong inversion case, and

$$\sigma^2(\Delta I_D) = g_m^2 \sigma^2(\Delta V_{th}) \tag{A.31}$$

for the weak inversion. Also, considering (A.24) and (A.25), $\sigma^2(\Delta I_D)$ can be expressed as

$$\sigma^2(\Delta I_D) = I_D^2 \frac{A_{KT}^2}{WL} + g_m^2 \frac{A_{Vth}^2}{WL} \tag{A.32}$$

for the transistors in strong inversion, and

$$\sigma^2(\Delta I_D) = g_m^2 \frac{A_{Vth}^2}{WL} \tag{A.33}$$

for the transistors in weak inversion. Ultimately, the variance of the overall random offset voltage V_{OFFrnd} can be calculated by dividing the overall current difference (sum of the particular contributions of OTA transistors) with the transconductance of the differential pair $g_{m,dp}$, specifically

$$\sigma^2(V_{OFFrnd}) = \frac{\sum \sigma^2(\Delta I_D)}{g_{m,dp}^2}. \tag{A.34}$$

A.2 Propagation Delay

A.2.1 Differential Pair in Strong Inversion

Assuming that the differential input pair of a comparator is in the strong inversion region, the drain current of the input transistor pair, specifically M_{N1} and M_{N2} from Fig. 2.3a, can be expressed as

$$I_D \approx K_T (V_{GS} - V_{th})^2, \tag{A.35}$$

where the channel length modulation effect from (A.1) is neglected. Considering the input voltages at the non–inverting and inverting terminal, specifically V_{IN+} and V_{IN-}, the gate–source voltage V_{GS} of M_{N1} and M_{N2} is

$$V_{GS,N1} = V_{IN+} - V_S \tag{A.36}$$

and

$$V_{GS,N2} = V_{IN-} - V_S, \tag{A.37}$$

where V_S is the common source voltage of the two transistors. Hence, the drain currents can be expressed as

$$I_{D,N1} = K_T (V_{IN+} - V_S - V_{th})^2 \tag{A.38}$$

for M_{N1}, and

$$I_{D,N2} = K_T (V_{IN-} - V_S - V_{th})^2 \tag{A.39}$$

for M_{N2}. Taking the square root of (A.38) and (A.39) leads to

$$\sqrt{I_{D,N1}} = \sqrt{K_T}(V_{IN+} - V_S - V_{th}) \tag{A.40}$$

and

$$\sqrt{I_{D,N2}} = \sqrt{K_T}(V_{IN-} - V_S - V_{th}). \tag{A.41}$$

Furthermore, subtracting (A.41) from (A.40) results in

$$\sqrt{I_{D,N1}} - \sqrt{I_{D,N2}} = \sqrt{K_T}\Delta V_{IN}, \tag{A.42}$$

where ΔV_{IN} is the differential input voltage, defined as

$$\Delta V_{IN} = V_{IN+} - V_{IN-}. \tag{A.43}$$

Taking the square value of both sides in (A.42) provides the following:

$$I_{D,N1} - 2\sqrt{I_{D,N1} I_{D,N2}} + I_{D,N2} = K_T \Delta V_{IN}^2. \tag{A.44}$$

Moreover, the sum of the two drain currents always equals the bias current I_{BC}, specifically

$$I_{BC} = I_{D,N1} + I_{D,N2}, \tag{A.45}$$

which combined with (A.44) eventually leads to:

$$I_{BC} - 2\sqrt{I_{D,N1}(I_{BC} - I_{D,N1})} = K_T \Delta V_{IN}^2, \tag{A.46}$$

or otherwise expressed as

$$I_{BC}\left[1 - 2\sqrt{\frac{I_{D,N1}}{I_{BC}} - \left(\frac{I_{D,N1}}{I_{BC}}\right)^2}\right] = K_T \Delta V_{IN}^2, \tag{A.47}$$

and finally

$$\sqrt{\frac{I_{D,N1}}{I_{BC}} - \left(\frac{I_{D,N1}}{I_{BC}}\right)^2} = \frac{1}{2} - \frac{K_T \Delta V_{IN}^2}{2I_{BC}}. \tag{A.48}$$

According to (A.35) and (A.45), the ratio of I_{BC} and K_T can be written as

$$\frac{I_{BC}}{K_T} = 2(V_{GS0} - V_{th})^2, \tag{A.49}$$

where V_{GS0} is the nominal gate–source voltage of the input pair transistors under the condition $V_{IN+} = V_{IN-}$, for which the drain currents of the transistors M_{N1} and M_{N2} are approximately equal. With this, (A.48) can be written as

$$\sqrt{\frac{I_{D,N1}}{I_{BC}} - \left(\frac{I_{D,N1}}{I_{BC}}\right)^2} = \frac{1}{2} - \frac{\Delta V_{IN}^2}{4(V_{GS0} - V_{th})^2}, \tag{A.50}$$

or, after squaring both sides, as

$$\left(\frac{I_{D,N1}}{I_{BC}}\right)^2 - \frac{I_{D,N1}}{I_{BC}} + \left(\frac{1}{2} - \frac{\Delta V_{IN}^2}{4(V_{GS0} - V_{th})^2}\right)^2 = 0. \tag{A.51}$$

Solving (A.51) for $I_{D,N1}/I_{BC}$ variable provides the following expression for the differential currents of the transistors M_{N1} and M_{N2}, specifically

$$\frac{I_{D,N1/2}}{I_{BC}} = \frac{1}{2}\left(1 \pm \frac{\Delta V_{IN}}{(V_{GS0} - V_{th})}\sqrt{1 - \left(\frac{\Delta V_{IN}}{2(V_{GS0} - V_{th})}\right)^2}\right). \tag{A.52}$$

Furthermore, if the higher order effects of ΔV_{IN} are neglected, (A.52) is simplified to

$$\frac{I_{D,N1/2}}{I_{BC}} = \frac{1}{2}\left(1 \pm \frac{\Delta V_{IN}}{(V_{GS0} - V_{th})}\right). \tag{A.53}$$

The transient behavior of the drain currents $I_{D,N1}$ and $I_{D,N2}$, assuming the test bench from Fig. 2.6, is depicted in Fig. A.1, demonstrating a comparison event of the integrating voltage VC with the reference voltage V_{REF}.

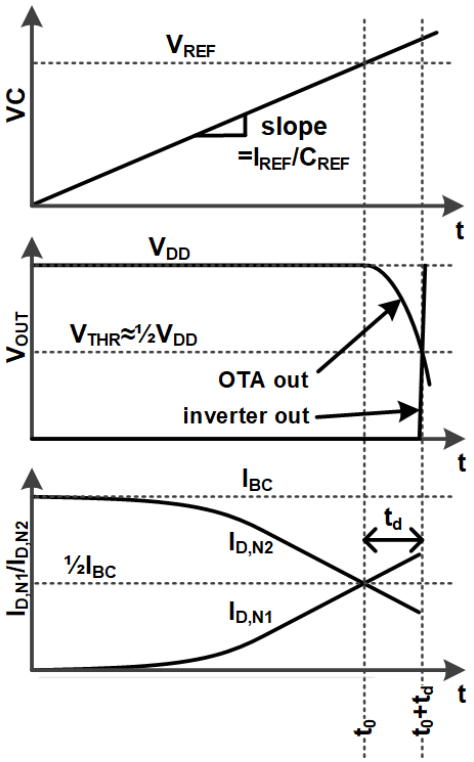


Figure A.1: The transient waveforms of the comparator signals during the comparison event.

Here, for $t_0 < t < t_0 + t_d$, the expression for the output current I_{OUT} which charges and discharges the effective output capacitance C_{out} of the OTA can be written as

$$I_{OUT} = -I_{D,P4} - I_{D,N4} \approx I_{D,N2} - I_{D,N1}. \tag{A.54}$$

Considering (A.53) and (A.49), the expression for the two drain currents is

$$I_{D,N1/2} = \frac{I_{BC}}{2}\left(1 \pm \frac{\sqrt{2K_T}}{\sqrt{I_{BC}}}\Delta V_{IN}\right), \tag{A.55}$$

eventually leading to

$$I_{OUT} = -\Delta V_{IN}\sqrt{2K_T I_{BC}}. \tag{A.56}$$

For $t_0 < t < t_0 + t_d$, the differential input voltage ΔV_{IN} can be written as a function of time in

the following way:

$$\Delta V_{IN}(t) = \frac{I_{REF}}{C_{REF}}(t - t_0). \tag{A.57}$$

Consequently, considering (A.56) and (A.57), the output current I_{OUT} as a function of time for $t_0 < t < t_0 + t_d$ can be expressed in the following way:

$$I_{OUT}(t) = -\frac{I_{REF}\sqrt{2K_T I_{BC}}}{C_{REF}}(t - t_0). \tag{A.58}$$

Finally, the propagation delay t_d of the comparator is experienced as the time needed for the output voltage of the OTA to reach the digital voltage threshold V_{THR}, where the value of V_{THR} is usually around half of the supply voltage ($V_{THR} \approx ½V_{DD}$). In this case, the output current needs to discharge the output node of the OTA, starting from V_{DD}, down to V_{THR}. Therefore, the following is valid:

$$V_{THR} = V_{DD} + \frac{1}{C_{out}}\int_{t_0}^{t_d+t_0} I_{OUT}(t)dt, \tag{A.59}$$

or

$$-\frac{1}{C_{out}}\int_{t_0}^{t_d+t_0} I_{OUT}(t)dt = V_{DD} - V_{THR} \approx \frac{V_{DD}}{2}. \tag{A.60}$$

Considering (A.58) and (A.60), the following is valid:

$$\frac{1}{C_{out}}\int_{t_0}^{t_d+t_0} \frac{I_{REF}\sqrt{2K_T I_{BC}}}{C_{REF}}(t - t_0)dt = \frac{V_{DD}}{2}. \tag{A.61}$$

Solving the definite integral results in

$$\frac{1}{2}\cdot\frac{I_{REF}\sqrt{2K_T I_{BC}}}{C_{REF}C_{out}}t_d^2 = \frac{V_{DD}}{2}. \tag{A.62}$$

Accordingly, the expression for the propagation delay of the comparator with the differential pair in strong inversion, valid for both the nMOS and pMOS input pair, can be written as

$$t_d = \sqrt{\frac{V_{DD}C_{REF}C_{out}}{I_{REF}\sqrt{2K_T I_{BC}}}}. \tag{A.63}$$

A.2.2 Differential Pair in Weak Inversion

Assuming that the differential input pair of a comparator is in the weak inversion region, the drain current of the input transistors, specifically M_{N1} and M_{N2} from Fig. 2.3a, can be written as [59]

$$I_D = I_{D0} \cdot exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right), \tag{A.64}$$

where I_{D0} is

$$I_{D0} = (n-1)\mu_c C_{ox} V_T^2 \tag{A.65}$$

and V_T is the thermal voltage ($V_T = kT/q$). Therefore, considering the expressions for the gate–source voltages, (A.36) and (A.37), the drain currents can expressed as

$$I_{D,N1} = I_{D0} \cdot exp\left(\frac{V_{IN+} - V_S - V_{th}}{nV_T}\right) \tag{A.66}$$

for M_{N1}, and

$$I_{D,N2} = I_{D0} \cdot exp\left(\frac{V_{IN-} - V_S - V_{th}}{nV_T}\right) \tag{A.67}$$

for M_{N2}. Furthermore, dividing (A.66) with (A.67) results in

$$\frac{I_{D,N1}}{I_{D,N2}} = exp\left(\frac{\Delta V_{IN}}{nV_T}\right), \tag{A.68}$$

where

$$\Delta V_{IN} = V_{IN+} - V_{IN-}. \tag{A.69}$$

Also, since the sum of the two currents is always equal to the bias current I_{BC}, specifically

$$I_{BC} = I_{D,N1} + I_{D,N2}, \tag{A.70}$$

the expression for the drain currents can be written as

$$I_{D,N1/2} = \frac{I_{BC}}{1 + exp\left(\mp\frac{\Delta V_{IN}}{n \cdot V_T}\right)}. \tag{A.71}$$

The depiction of the transient waveforms within a comparison event shown in Fig. A.1 is also valid in this case. Again, for $t_0 < t < t_0 + t_d$, the expression for the output current I_{OUT} which charges and discharges the effective output capacitance C_{out} of the OTA can be written as

$$I_{OUT} = -I_{D,P4} - I_{D,N4} \approx I_{D,N2} - I_{D,N1}. \tag{A.72}$$

Considering (A.71) and (A.72), the expression for the output current is

$$I_{OUT} = -tanh\left(\frac{\Delta V_{IN}}{2nV_T}\right) I_{BC}. \tag{A.73}$$

For $t_0 < t < t_d + t_0$, the differential input voltage ΔV_{IN} can be written as a function of time in the following way:

$$\Delta V_{IN}(t) = \frac{I_{REF}}{C_{REF}}(t - t_0). \tag{A.74}$$

Consequently, considering (A.73) and (A.74), the output current I_{OUT} is defined as a function time in the time interval $t_0 < t < t_d + t_0$ in the following way:

$$I_{OUT}(t) = -tanh\left[\frac{I_{REF}(t - t_0)}{2nV_T C_{REF}}\right] I_{BC}. \tag{A.75}$$

Similar to before, according to (A.60), the following expression is valid

$$-\frac{1}{C_{out}} \int_{t_0}^{t_d + t_0} I_{OUT}(t)dt = \frac{V_{DD}}{2}, \tag{A.76}$$

used for the calculation of the time from the equilibrium point (t_0) to the switching point of the comparator, i.e., the propagation delay time (t_d). Specifically, combining (A.75) and (A.76) provides

$$\frac{1}{C_{out}} \int_{t_0}^{t_0 + t_d} I_{BC} \cdot tanh\left[\frac{I_{REF}(t - t_0)}{2nV_T C_{REF}}\right] dt = \frac{V_{DD}}{2}. \tag{A.77}$$

Solving the definite integral results in

$$\frac{2nV_T C_{REF} I_{BC}}{I_{REF} C_{out}} \cdot ln\left[cosh\left(\frac{I_{REF} \cdot t_d}{2nV_T C_{REF}}\right)\right] = \frac{V_{DD}}{2}. \tag{A.78}$$

Accordingly, the expression for the propagation delay of the comparator with the differential pair in weak inversion, valid for both the nMOS and pMOS input pair, can be expressed as

$$t_d = \frac{2nV_T C_{REF}}{I_{REF}} arccosh\left[exp\left(\frac{V_{DD} I_{REF} C_{out}}{4nV_T I_{BC} C_{REF}}\right)\right]. \tag{A.79}$$

Also, the inner function approximation using the first two terms of Taylor's series expansion is

$$arccosh\left[exp\left(x\right)\right] \approx \sqrt{2x} + \frac{x^{3/2}}{3\sqrt{2}}, \tag{A.80}$$

valid for limited values of the argument ($x < 5$). In this case, the propagation delay is

$$t_d = \sqrt{\frac{2nV_T V_{DD} C_{REF} C_{out}}{I_{REF} I_{BC}}} + \frac{\sqrt{2}}{3}\sqrt{\left(\frac{V_{DD} C_{out}}{4I_{BC}}\right)^3 \frac{I_{REF}}{nV_T C_{REF}}}. \tag{A.81}$$

Appendix B

Sensitivity Analysis

B.1 Sensitivity to Offset Voltage

B.1.1 Conventional Core

Considering the expression for the oscillation period T_{osc} of the conventional relaxation oscillator core (2.1), the differential dT_{osc} with respect to the offset voltage of the two comparators, V_{OFF1} and V_{OFF2}, is

$$dT_{osc} = \frac{C_{REF}}{I_{REF}} dV_{OFF1} + \frac{C_{REF}}{I_{REF}} dV_{OFF2}. \tag{B.1}$$

Accordingly, for relatively small changes in the offset voltages, ΔV_{OFF1} and ΔV_{OFF2}, the variation of the oscillation period is

$$\Delta T_{osc} = \frac{C_{REF}}{I_{REF}} \Delta V_{OFF1} + \frac{C_{REF}}{I_{REF}} \Delta V_{OFF2}. \tag{B.2}$$

Furthermore, dividing both sides with the approximated oscillation period,

$$T_{osc} \approx \frac{2V_{REF}C_{REF}}{I_{REF}}, \tag{B.3}$$

results in

$$\frac{\Delta T_{osc}}{T_{osc}} = \frac{\Delta V_{OFF1}}{2V_{REF}} + \frac{\Delta V_{OFF2}}{2V_{REF}}. \tag{B.4}$$

Since ΔV_{OFF1} and ΔV_{OFF2} are random variables, the variance of the relative oscillation period variation $\Delta T_{osc}/T_{osc}$ is

$$\sigma^2 \left(\frac{\Delta T_{osc}}{T_{osc}} \right) \approx \frac{1}{4V_{REF}^2} \sigma^2 \left(\Delta V_{OFF1} + \Delta V_{OFF2} \right). \tag{B.5}$$

Considering the Bienaymé's identity [66], specifically

$$\sigma^2 \left(\sum_{i=1}^{n} X_i \right) = \sum_{i,j=1}^{n} cor(X_i, X_j) \sigma(X_i) \sigma(X_j), \tag{B.6}$$

where $cor(X_i, X_j)$ is a correlation between the two random variables X_i and X_j, (B.5) can be written as

$$\sigma^2 \left(\frac{\Delta T_{osc}}{T_{osc}} \right) =$$
$$= \frac{1}{4V_{REF}^2} \left[\sigma^2(\Delta V_{OFF1}) + 2cor\left(\Delta V_{OFF1}, \Delta V_{OFF2}\right) \sigma(\Delta V_{OFF1}) \sigma(\Delta V_{OFF2}) + \sigma^2(\Delta V_{OFF2}) \right]. \tag{B.7}$$

In the case of the systematic offset voltage, ΔV_{OFF1} and ΔV_{OFF2} are dependent only on the process variations. Therefore, for two identically designed comparators, assuming the absence of mismatch, ΔV_{OFF1} and ΔV_{OFF2} are equal to the systematic offset voltage V_{OFFsys}, in

particular

$$\Delta V_{OFF1} = \Delta V_{OFF1} = V_{OFFsys}. \tag{B.8}$$

This also implies a complete correlation, specifically

$$cor\left(\Delta V_{OFF1}, \Delta V_{OFF2}\right) = 1. \tag{B.9}$$

Accordingly, considering (B.7), (B.8), and (B.9), the relative variation of the oscillation period due to the systematic offset voltage is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{V_{REF}^2}\sigma^2(V_{OFFsys}), \tag{B.10}$$

or, in terms of standard deviation,

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{V_{REF}}\sigma(V_{OFF,sys}). \tag{B.11}$$

On the other hand, since the random offset voltage is entirely mismatch–related [58], no correlation is assumed between the two comparators, specifically

$$cor\left(\Delta V_{OFF1}, \Delta V_{OFF2}\right) = 0. \tag{B.12}$$

Consequently, (B.7) reduces to

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{4V_{REF}^2}\left[\sigma^2(\Delta V_{OFF1}) + \sigma^2(\Delta V_{OFF2})\right]. \tag{B.13}$$

Assuming the identical design of both comparators, the standard deviations of ΔV_{OFF1} and ΔV_{OFF2} are equal, specifically

$$\sigma(\Delta V_{OFF1}) = \sigma(\Delta V_{OFF2}) = \sigma(V_{OFFrnd}). \tag{B.14}$$

Accordingly, the relative variation of the oscillation period due to the random offset voltage is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{2V_{REF}^2}\sigma^2(V_{OFFrnd}), \tag{B.15}$$

or, in terms of standard deviation,

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{\sqrt{2}V_{REF}}\sigma(V_{OFFrnd}). \tag{B.16}$$

B.1.2 Core with Replica Comparators (w/–RC)

Considering the expression for the oscillation period T_{osc} of the oscillator core with replica comparators (2.18), the differential dT_{osc} with respect to the offset voltage of the four comparators (V_{OFF1}, V_{OFF2}, V_{OFF3}, and V_{OFF4}) is

$$dT_{osc} = \frac{C_{REF}}{2I_{REF}} dV_{OFF1} + \frac{C_{REF}}{2I_{REF}} dV_{OFF2} - \frac{C_{REF}}{2I_{REF}} dV_{OFF3} - \frac{C_{REF}}{2I_{REF}} dV_{OFF4}. \tag{B.17}$$

Accordingly, for relatively small changes in the offset voltages, ΔV_{OFF1-4}, the variation of the oscillation period is

$$\Delta T_{osc} = \frac{C_{REF}}{2I_{REF}} \Delta V_{OFF1} + \frac{C_{REF}}{2I_{REF}} \Delta V_{OFF2} - \frac{C_{REF}}{2I_{REF}} \Delta V_{OFF3} - \frac{C_{REF}}{2I_{REF}} \Delta V_{OFF4}. \tag{B.18}$$

In continuation, dividing both sides with the oscillation period (B.3) results in

$$\frac{\Delta T_{osc}}{T_{osc}} = \frac{\Delta V_{OFF1}}{4V_{REF}} + \frac{\Delta V_{OFF2}}{4V_{REF}} - \frac{\Delta V_{OFF3}}{4V_{REF}} - \frac{\Delta V_{OFF4}}{4V_{REF}}. \tag{B.19}$$

Since ΔV_{OFF1-4} are random variables, the variance of the relative oscillation period variation $\Delta T_{osc}/T_{osc}$ is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{16V_{REF}^2} \sigma^2(\Delta V_{OFF1} + \Delta V_{OFF2} - \Delta V_{OFF3} - \Delta V_{OFF4}). \tag{B.20}$$

Considering the Bienaymé's identity (B.6), (B.20) can be expressed as

$$\begin{aligned}
&\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \\
&= \frac{1}{16V_{REF}^2}[\sigma^2(\Delta V_{OFF1}) + \sigma^2(\Delta V_{OFF2}) + \sigma^2(-\Delta V_{OFF3}) + \sigma^2(-\Delta V_{OFF4}) \\
&\quad + 2cor(\Delta V_{OFF1}, \Delta V_{OFF2})\sigma(\Delta V_{OFF1})\sigma(\Delta V_{OFF2}) \\
&\quad + 2cor(\Delta V_{OFF1}, -\Delta V_{OFF3})\sigma(\Delta V_{OFF1})\sigma(-\Delta V_{OFF3}) \\
&\quad + 2cor(\Delta V_{OFF1}, -\Delta V_{OFF4})\sigma(\Delta V_{OFF1})\sigma(-\Delta V_{OFF4}) \\
&\quad + 2cor(\Delta V_{OFF2}, -\Delta V_{OFF3})\sigma(\Delta V_{OFF2})\sigma(-\Delta V_{OFF3}) \\
&\quad + 2cor(\Delta V_{OFF2}, -\Delta V_{OFF4})\sigma(\Delta V_{OFF2})\sigma(-\Delta V_{OFF4}) \\
&\quad + 2cor(-\Delta V_{OFF3}, -\Delta V_{OFF4})\sigma(-\Delta V_{OFF3})\sigma(-\Delta V_{OFF4})].
\end{aligned} \tag{B.21}$$

In the case of the systematic offset voltage, ΔV_{OFF1-4} are exclusively related to the process variation. Therefore, for four identically designed comparators, ΔV_{OFF1-4} are equal to the

systematic offset voltage, in particular

$$\Delta V_{OFF1} = \Delta V_{OFF2} = \Delta V_{OFF3} = \Delta V_{OFF4} = V_{OFFsys}, \tag{B.22}$$

also implying the following:

$$cor(\Delta V_{OFF1}, \Delta V_{OFF2}) = 1, \tag{B.23}$$

$$cor(\Delta V_{OFF1}, -\Delta V_{OFF3}) = -1, \tag{B.24}$$

$$cor(\Delta V_{OFF1}, -\Delta V_{OFF4}) = -1, \tag{B.25}$$

$$cor(\Delta V_{OFF2}, -\Delta V_{OFF3}) = -1, \tag{B.26}$$

$$cor(\Delta V_{OFF2}, -\Delta V_{OFF4}) = -1, \tag{B.27}$$

and

$$cor(-\Delta V_{OFF3}, -\Delta V_{OFF4}) = 1. \tag{B.28}$$

Accordingly, considering (B.21)–(B.28), the relative variation of the oscillation period due to the systematic offset voltage is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = 0 \cdot \sigma^2(V_{OFFsys}). \tag{B.29}$$

On the other hand, the random offset voltages of four comparators are not correlated, which implies

$$cor(\Delta V_{OFF1}, \Delta V_{OFF2}) = 0, \tag{B.30}$$

$$cor(\Delta V_{OFF1}, -\Delta V_{OFF3}) = 0, \tag{B.31}$$

$$cor(\Delta V_{OFF1}, -\Delta V_{OFF4}) = 0, \tag{B.32}$$

$$cor(\Delta V_{OFF2}, -\Delta V_{OFF3}) = 0, \tag{B.33}$$

$$cor(\Delta V_{OFF2}, -\Delta V_{OFF4}) = 0, \tag{B.34}$$

and

$$cor(-\Delta V_{OFF3}, -\Delta V_{OFF4}) = 0. \tag{B.35}$$

Consequently, (B.21) reduces to

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{16V_{REF}^2}[\sigma^2(\Delta V_{OFF1}) + \sigma^2(\Delta V_{OFF2}) + \sigma^2(-\Delta V_{OFF3}) + \sigma^2(-\Delta V_{OFF4})]. \tag{B.36}$$

Assuming the identical design of all comparators, the standard deviations $\sigma(\Delta V_{OFF1-4})$ are

equal, specifically

$$\sigma(\Delta V_{OFF1}) = \sigma(\Delta V_{OFF2}) = \sigma(-\Delta V_{OFF3}) = \sigma(-\Delta V_{OFF4}) = \sigma(V_{OFFrnd}). \tag{B.37}$$

Accordingly, the relative variation of the oscillation period due to the random offset voltage is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{4V_{REF}^2}\sigma^2(V_{OFFrnd}), \tag{B.38}$$

or, in terms of standard deviation,

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{2V_{REF}}\sigma(V_{OFFrnd}). \tag{B.39}$$

B.1.3 Other Cores (w/–SCC, w/–RI, and w/–RCC)

Three proposed architectures with offset cancellation using chopped comparators, namely the core with self–compensating chopped comparator (w/–SCC), core with replica integrator (w/–RI), and core with replica chopped comparator (w/–RCC), are expected to have zero sensitivity with respect to the systematic and random offset voltage, specifically

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = 0 \cdot \sigma(V_{OFFrnd}) \tag{B.40}$$

and

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = 0 \cdot \sigma(V_{OFFsys}). \tag{B.41}$$

Here, the analytical expressions for the oscillation period, (3.9), (4.13), and (5.53), respectively, indicate perfect cancellation of the offset voltage. Nevertheless, limited non–zero values may arise within the implemented circuits, originating from the second–order effects of the chopper operation.

B.2 Sensitivity to Propagation Delay

B.2.1 Conventional Core

Considering the expression for the oscillation period T_{osc} of the conventional relaxation oscillator core (2.1), the differential dT_{osc} with respect to the propagation delay of the two comparators, t_{d1} and t_{d2}, is

$$dT_{osc} = dt_{d1} + dt_{d2}. \tag{B.42}$$

Accordingly, for relatively small changes in the propagation delay, Δt_{d1} and Δt_{d2}, the variation of the oscillation period is

$$\Delta T_{osc} = \Delta t_{d1} + \Delta t_{d2}, \tag{B.43}$$

otherwise written as

$$\frac{\Delta T_{osc}}{T_{osc}} = \frac{\Delta t_{d1}}{T_{osc}} + \frac{\Delta t_{d2}}{T_{osc}}. \tag{B.44}$$

Since Δt_{d1} and Δt_{d2} are random variables, the variance of the relative oscillation period variation $\Delta T_{osc}/T_{osc}$ is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{T_{osc}^2}\sigma^2(\Delta t_{d1} + \Delta t_{d2}). \tag{B.45}$$

Considering the Bienaymé's identity (B.6), (B.45) can be expressed as

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{T_{osc}^2}\left[\sigma^2(\Delta t_{d1}) + 2cor(\Delta t_{d1}, \Delta t_{d2})\sigma(\Delta t_{d1})\sigma(\Delta t_{d2}) + \sigma^2(\Delta t_{d2})\right]. \tag{B.46}$$

In Section 2.3.2 it is demonstrated that the propagation delays of two matched and identically designed comparators are similar in value and strongly correlated, specifically $cor(\Delta t_{d1}, \Delta t_{d1}) \approx 0.93$ for the given example. Therefore, the following is assumed within this analysis:

$$\Delta t_{d1} = \Delta t_{d2} = \Delta t_d, \tag{B.47}$$

also implying

$$cor(\Delta t_{d1}, \Delta t_{d2}) = 1. \tag{B.48}$$

Accordingly, considering (B.46), (B.47), and (B.48), the relative variation of the oscillation period due to the propagation delay is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{4}{T_{osc}^2}\sigma^2(\Delta t_d), \tag{B.49}$$

or, in terms of standard deviation,

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{2}{T_{osc}}\sigma(\Delta t_d). \tag{B.50}$$

B.2.2 Core with Replica Comparators (w/–RC)

Considering the expression for the oscillation period T_{osc} (2.18), the differential dT_{osc} with respect to the propagation delay of the four comparators (t_{d1}, t_{d2}, t_{d3}, and t_{d4}) is

$$dT_{osc} = \frac{1}{2}dt_{d1} + \frac{1}{2}dt_{d2} - \frac{1}{2}dt_{d3} - \frac{1}{2}dt_{d4}. \tag{B.51}$$

Accordingly, for relatively small changes in the propagation delay, Δt_{d1-4}, the variation of the oscillation period is

$$\Delta T_{osc} = \frac{1}{2}\Delta t_{d1} + \frac{1}{2}\Delta t_{d2} - \frac{1}{2}\Delta t_{d3} - \frac{1}{2}\Delta t_{d4}. \tag{B.52}$$

or otherwise written as

$$\frac{\Delta T_{osc}}{T_{osc}} = \frac{\Delta t_{d1}}{2T_{osc}} + \frac{\Delta t_{d2}}{2T_{osc}} - \frac{\Delta t_{d3}}{2T_{osc}} - \frac{\Delta t_{d4}}{2T_{osc}}. \tag{B.53}$$

Since Δt_{d1-4} are random variables, the variance of the relative oscillation period variation $\Delta T_{osc}/T_{osc}$ is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \frac{1}{4T_{osc}^2}\sigma^2(\Delta t_{d1} + \Delta t_{d2} - \Delta t_{d3} - \Delta t_{d4}). \tag{B.54}$$

Considering the Bienaymé's identity (B.6), (B.54), can be expressed as

$$\begin{aligned}
&\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = \\
&= \frac{1}{4T_{osc}^2}[\sigma^2(\Delta t_{d1}) + \sigma^2(\Delta t_{d2}) + \sigma^2(-\Delta t_{d3}) + \sigma^2(-\Delta t_{d4}) \\
&\quad + 2cor(\Delta t_{d1}, \Delta t_{d2})\sigma(\Delta t_{d1})\sigma(\Delta t_{d2}) \\
&\quad + 2cor(\Delta t_{d1}, -\Delta t_{d3})\sigma(\Delta t_{d1})\sigma(-\Delta t_{d3}) \\
&\quad + 2cor(\Delta t_{d1}, -\Delta t_{d4})\sigma(\Delta t_{d1})\sigma(-\Delta t_{d4}) \\
&\quad + 2cor(\Delta t_{d2}, -\Delta t_{d3})\sigma(\Delta t_{d2})\sigma(-\Delta t_{d3}) \\
&\quad + 2cor(\Delta t_{d2}, -\Delta t_{d4})\sigma(\Delta t_{d2})\sigma(-\Delta t_{d4}) \\
&\quad + 2cor(-\Delta t_{d3}, -\Delta t_{d4})\sigma(-\Delta t_{d3})\sigma(-\Delta t_{d4})].
\end{aligned} \tag{B.55}$$

According to the conclusions from Section 2.3.2, the following is assumed

$$\Delta t_{d1} = \Delta t_{d2} = \Delta t_{d3} = \Delta t_{d4} = \Delta t_d, \tag{B.56}$$

also implying

$$cor(\Delta t_{d1}, \Delta t_{d2}) = 1, \tag{B.57}$$

$$cor(\Delta t_{d1}, -\Delta t_{d3}) = -1, \tag{B.58}$$

$$cor(\Delta t_{d1}, -\Delta t_{d4}) = -1, \tag{B.59}$$

$$cor(\Delta t_{d2}, -\Delta t_{d3}) = -1, \tag{B.60}$$

$$cor(\Delta t_{d2}, -\Delta t_{d4}) = -1, \tag{B.61}$$

and

$$cor(-\Delta t_{d3}, -\Delta t_{d4}) = 1. \tag{B.62}$$

Accordingly, considering (B.55)–(B.62), the relative variation of the oscillation period due to the propagation delay is

$$\sigma^2\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = 0 \cdot \sigma^2(\Delta t_d). \tag{B.63}$$

In practice, limited non–zero values are expected because of a minor mismatch of propagation delays in different comparators.

B.2.3 Other Cores (w/–SCC, w/–RI, and w/–RCC)

The core with self–compensating chopped comparator (w/–SCC) cancels the influence of the propagation delay entirely, as shown in (3.9). On the other hand, the cancellation of the delay in the core with replica integrator (w/–RI) and core with replica chopped comparator (w/–RCC) is based on matching the delays of two comparators, as shown in analytical expressions for the oscillation period, (4.13) and (5.53), respectively. Therefore, similar as demonstrated in Section B.2.2, w/–RI and w/–RCC cores are also expected to have near–zero sensitivity with respect to the propagation delay, specifically

$$\sigma\left(\frac{\Delta T_{osc}}{T_{osc}}\right) = 0 \cdot \sigma(\Delta t_d). \tag{B.64}$$

In all cases, limited non–zero values may arise within the implemented circuits, originating from the second–order effects of the chopping scheme. Also, w/–RI and w/–RCC cores will have an additional error due to a minor mismatch in delay values of different comparators.

Appendix C

Analysis of Temperature Calibration Method

C.1 Temperature Dependency of the Output Frequency

The temperature dependency of the oscillator frequency $f(T)$ normalized at the nominal temperature $T = T_0$, $f(T) = f_{osc}(T)/f_{osc}(T_0)$, can be expressed as the n–th order polynomial

$$f(T) = c_n(T-T_0)^n + ... + c_3(T-T_0)^3 + c_2(T-T_0)^2 + c_1(T-T_0) + 1, \tag{C.1}$$

where c_n to c_1 are the polynomial coefficients, unique for each oscillator sample. Within this analysis, the second–order polynomial is assumed for the frequency characteristic, specifically

$$f(T) = c_2(T-T_0)^2 + c_1(T-T_0) + 1, \tag{C.2}$$

since the third and higher order coefficients are typically present with negligible influence.

Chapter 5 describes the oscillator prototype having the tuning capability of the first–order temperature coefficient of the output frequency ($TC1_f$), illustrated in Fig. 5.13. Here, the first–order temperature coefficient of the frequency is changed with fixed steps by changing the temperature coefficient trim code TCT. This specifically implies the alteration of the polynomial coefficient c_1, transforming (C.2) into

$$f(T) = c_2(T-T_0)^2 + c_1'(T-T_0) + 1, \tag{C.3}$$

where c_1' is the post–trim value of the first–order coefficient of the polynomial. For each sample, as depicted in Fig. 5.14, the optimal post–trim value of the first–order polynomial coefficient c_1^* (with $c_1' \mapsto c_1^*$) can be calculated starting from the condition $f(T_{MIN}) = f(T_{MAX})$, specifically

$$c_2(T_{MIN}-T_0)^2 + c_1^*(T_{MIN}-T_0) + 1 = c_2(T_{MAX}-T_0)^2 + c_1^*(T_{MAX}-T_0) + 1, \tag{C.4}$$

where T_{MIN} and T_{MAX} are the minimum and maximum temperature, respectively. The equality of both sides from (C.4) is fulfilled in case c_1^* is equal to

$$c_1^* = c_2(2T_0 - T_{MAX} - T_{MIN}). \tag{C.5}$$

Conclusively, the difference between the two coefficients c_1^* and c_1 of each sample represents the optimal first–order temperature coefficient trim value $\Delta TC1_f^*$ of a sample, specifically

$$\Delta TC1_f^* = c_1^* - c1, \tag{C.6}$$

or taking (C.5) into account

$$\Delta TC1_f^* = c_2(2T_0 - T_{MAX} - T_{MIN}) - c_1. \tag{C.7}$$

C.2 Three–Point Temperature Calibration

In case the frequency is measured at three different temperatures, as depicted in Fig. 5.14, specifically at the nominal temperature $T = T_0$

$$f(T_0) = c_2(T_0 - T_0)^2 + c_1(T_0 - T_0) + 1 = 1, \tag{C.8}$$

at a specific low temperature $T = T_L$ ($T_L < T_0$)

$$f(T_L) = c_2(T_L - T_0)^2 + c_1(T_L - T_0) + 1, \tag{C.9}$$

and at a specific high temperature $T = T_H$ ($T_H < T_0$)

$$f(T_H) = c_2(T_H - T_0)^2 + c_1(T_H - T_0) + 1, \tag{C.10}$$

the exact values of the polynomial coefficients c_1 and c_2 for each sample can be calculated with

$$c_1 = -\frac{(T_L - T_0)(f(T_H) - f(T_0))}{(T_H - T_0)(T_H - T_L)} + \frac{(T_H - T_0)(f(T_L) - f(T_0))}{(T_L - T_0)(T_H - T_L)} \tag{C.11}$$

and

$$c_2 = \frac{f(T_H) - f(T_0)}{(T_H - T_0)(T_H - T_L)} - \frac{f(T_L) - f(T_0)}{(T_L - T_0)(T_H - T_L)}. \tag{C.12}$$

Therefore, the three–point measurement of the output frequency provides sufficient information for the evaluation of the optimal trim value of the first–order temperature coefficient. In particular, considering (C.7), (C.11), and (C.12), the optimal trim value is calculated with

$$\Delta TC1_f^* = \frac{\frac{T_0 - T_{MAX} - T_{MIN} + T_L}{T_H - T_0}[f(T_H) - f(T_0)] - \frac{T_0 - T_{MAX} - T_{MIN} + T_H}{T_L - T_0}[f(T_L) - f(T_0)]}{T_H - T_L}. \tag{C.13}$$

Moreover, in a specific case where

$$T_{MAX} - T_H = T_L - T_{MIN}, \tag{C.14}$$

i.e., when the high and low measurement temperatures T_H and T_L are equally distant from their respective border temperatures T_{MAX} and T_{MIN}, (C.13) reduces to

$$\Delta TC1_f^* = -\frac{f(T_H) - f(T_L)}{T_H - T_L}. \tag{C.15}$$

Although not present in (C.15), the frequency measurement at $T = T_0$ is also necessary, specifically for the normalization of the frequency values at T_L and T_H.

C.3 Two–Point Temperature Calibration

Here, as depicted in Fig. 5.15, frequency measurement at two different temperatures is assumed, specifically the frequency $f(T_0)$ at the nominal temperature $T = T_0$ (C.8) and the frequency $f(T_H)$ at the high measurement temperature (C.10). Normally, having the information on only two evaluated points is insufficient for the calculation of the second–order polynomial coefficients from (C.2), and hence for obtaining the optimal first–order temperature coefficient trim value $\Delta TC1_f^*$. Nevertheless, the optimal trim value can be calculated, or at least well estimated, from a two–point measurement of the output frequency if certain conditions are fulfilled, as will be described in continuation.

First, the expression for the calculation of the optimal trim value from (C.15) is considered, valid under the condition from (C.14). If the low measurement temperature T_L and the respective frequency value $f(T_L)$ are substituted with the nominal temperature T_0 and the nominal frequency $f(T_0)$ in both equations, (C.15) transforms to

$$\Delta TC1_f^* = -\frac{f(T_H) - f(T_0)}{T_H - T_0}, \tag{C.16}$$

valid under the condition

$$T_{MAX} - T_H = T_0 - T_{MIN}. \tag{C.17}$$

This indicates that the optimal trim value $\Delta TC1_f^*$ can be obtained having only two measured frequencies if the nominal temperature T_0 and the second measurement temperature T_H are equidistant from the border temperatures (T_{MIN} and T_{MAX}). Accordingly, T_0 and T_H are then also equidistant from the middle of the temperature range:

$$\frac{T_0 + T_H}{2} = \frac{T_{MAX} + T_{MIN}}{2}. \tag{C.18}$$

Similarly, considering (C.8) and (C.10), the following is valid:

$$-\frac{f(T_H) - f(T_0)}{T_H - T_0} = -c_2(T_H - T_0) - c_1. \tag{C.19}$$

Furthermore, taking (C.18) into account ($T_H \mapsto T_{MAX} + T_{MIN} - T_0$), (C.19) transforms to

$$-\frac{f(T_H) - f(T_0)}{T_H - T_0} = -\frac{f(T_{MAX} + T_{MIN} - T_0) - f(T_0)}{T_{MAX} + T_{MIN} - 2T_0} = c_2(2T_0 - T_{MAX} - T_{MIN}) - c_1, \tag{C.20}$$

where the right side is equal to the predicted optimal trim value $\Delta TC1_f^*$ in (C.7).

In a general case, particularly when the condition from (C.18) is not fulfilled, the optimal temperature trim value $\Delta TC1_f^*$ is estimated in the following way. First, there always exist a temperature point T_0^* which fulfills the requirement from (C.18):

$$\frac{T_H + T_0^*}{2} = \frac{T_{MAX} + T_{MIN}}{2}, \tag{C.21}$$

or otherwise

$$T_0^* = T_{MAX} + T_{MIN} - T_H. \tag{C.22}$$

In this case, correspondent with (C.16) and (C.18), the following is valid:

$$\Delta TC1_f^* = -\frac{f(T_H) - f(T_0^*)}{T_H - T_0^*}. \tag{C.23}$$

Since the frequency measurement is in fact performed at the temperature T_0 rather than T_0^*, the proposed method relies on the estimation of $f(T_0^*)$, specifically the value of the frequency at $T = T_0^*$.

Initially, considering (C.2), the frequency $f(T_0^*)$ in relation to the nominal frequency $f(T_0)$ can be expressed as

$$f(T_0^*) = f(T_0) + c_2(T_0^* - T_0)^2 + c_1(T_0^* - T_0), \tag{C.24}$$

which inserted into (C.23) results in

$$\Delta TC1_f^* = -\frac{f(T_H) - f(T_0) - c_2(T_0^* - T_0)^2 - c_1(T_0^* - T_0)}{T_H - T_0^*}, \tag{C.25}$$

otherwise written as

$$\Delta TC1_f^* = -\frac{f(T_H) - f(T_0)}{T_H - T_0^*} + \frac{c_2(T_0^* - T_0)^2 + c_1(T_0^* - T_0)}{T_H - T_0^*}. \tag{C.26}$$

Furthermore, multiplying both sides with $(T_H - T_0^*)/(T_H - T_0)$ leads to

$$\frac{T_H - T_0^*}{T_H - T_0}\Delta TC1_f^* = -\frac{f(T_H) - f(T_0)}{T_H - T_0} + \frac{T_0^* - T_0}{T_H - T_0}\left[c_2(T_0^* - T_0) + c_1\right]. \tag{C.27}$$

Having the two–point measurement variable $\Delta TC1'_f$ defined as

$$\Delta TC1'_f = -\frac{f(T_H) - f(T_0)}{T_H - T_0} \tag{C.28}$$

provides the relation with the optimal temperature coefficient trim value $\Delta TC1_f^*$:

$$\frac{T_H - T_0^*}{T_H - T_0}\Delta TC1_f^* = \Delta TC1'_f + \frac{T_0^* - T_0}{T_H - T_0}\left[c_2(T_0^* - T_0) + c_1\right]. \tag{C.29}$$

Since relaxation oscillators are non–linear elements, both the first–order and the second–order polynomial coefficients of the oscillator frequency temperature characteristic (C.2) may originate from the same process–related non–idealities. Therefore, it is necessary to consider an eventual correlation between the two polynomial coefficients, assuming the following

$$c_2 \approx \alpha \cdot c_1 + \beta, \tag{C.30}$$

where α and β are the linear regression coefficients. The validity of this assumption is confirmed by the Monte Carlo simulations on a test–case oscillator, shown in Fig. C.1, where the calculated R^2 value is close to 0.9.

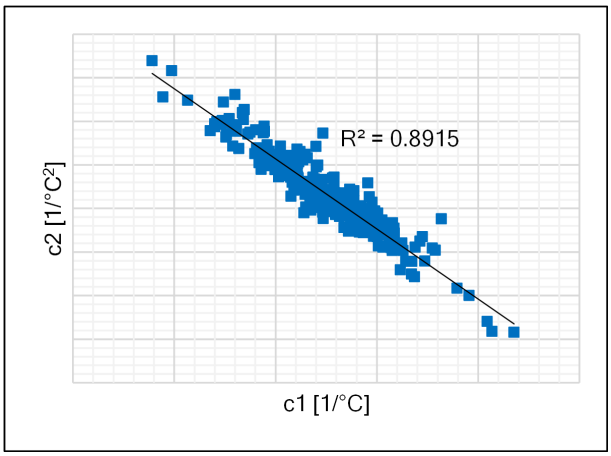


Figure C.1: The scatter plot of the polynomial coefficients c_1 and c_2, calculated from 250 Monte Carlo simulations of a test–case oscillator. The values on the x and y axis are omitted on purpose.

Using the approximation from (C.30), (C.29) transforms to

$$\frac{T_H - T_0^*}{T_H - T_0} \Delta TC1_f^* \approx \Delta TC1'_f + \frac{T_0^* - T_0}{T_H - T_0} \left[c_1 \left(\alpha (T_0^* - T_0) + 1 \right) + \beta (T_0^* - T_0) \right]. \tag{C.31}$$

Similarly, (C.7) provides the relation between $\Delta TC1_f^*$ and the polynomial coefficients c_1 and c_2, which, considering (C.30), can be rewritten as

$$\Delta TC1_f^* \approx c_1 \left[\alpha (2T_0 - T_{MAX} - T_{MIN}) - 1 \right] + \beta (2T_0 - T_{MAX} - T_{MIN}). \tag{C.32}$$

From here, the coefficient c_1 can be expressed as

$$c_1 \approx \frac{\Delta TC1_f^* - \beta (2T_0 - T_{MAX} - T_{MIN})}{\alpha (2T_0 - T_{MAX} - T_{MIN}) - 1}, \tag{C.33}$$

which combined with (C.31) results in

$$\begin{aligned}\left[\frac{T_H - T_0^*}{T_H - T_0} - \frac{T_0^* - T_0}{T_H - T_0} \cdot \frac{\alpha(T_0^* - T_0) + 1}{\alpha(2T_0 - T_{MAX} - T_{MIN}) - 1}\right] \Delta TC1_f^* \approx \\ \approx \Delta TC1'_f + \beta \frac{T_0^* - T_0}{T_H - T_0} \left[(T_0^* - T_0) - \frac{(2T_0 - T_{MAX} - T_{MIN})\left(\alpha(T_0^* - T_0) + 1\right)}{\alpha(2T_0 - T_{MAX} - T_{MIN}) - 1}\right].\end{aligned} \tag{C.34}$$

Eventually, (C.34) indicates that the optimal trim value $\Delta TC1_f^*$ can be estimated by the linear transformation of the $\Delta TC1'_f$ variable calculated with two–point measurement, specifically

$$\Delta TC1_f^* \approx a \cdot \Delta TC1'_f + b, \tag{C.35}$$

where

$$a = \frac{1}{\frac{T_H - T_0^*}{T_H - T_0} - \frac{T_0^* - T_0}{T_H - T_0} \cdot \frac{\alpha(T_0^* - T_0) + 1}{\alpha(2T_0 - T_{MAX} - T_{MIN}) - 1}} \tag{C.36}$$

and

$$b = \frac{\beta \frac{T_0^* - T_0}{T_H - T_0} \left[(T_0^* - T_0) - \frac{(2T_0 - T_{MAX} - T_{MIN})\left(\alpha(T_0^* - T_0) + 1\right)}{\alpha(2T_0 - T_{MAX} - T_{MIN}) - 1}\right]}{\frac{T_H - T_0^*}{T_H - T_0} - \frac{T_0^* - T_0}{T_H - T_0} \cdot \frac{\alpha(T_0^* - T_0) + 1}{\alpha(2T_0 - T_{MAX} - T_{MIN}) - 1}} \tag{C.37}$$

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List of Symbols

A	area
A_c	amplitude of the control signal
A_{KT}	mismatch proportionality constant for current factor
A_{Vth}	mismatch proportionality constant for threshold voltage
a	linear transformation coefficient (slope)
b	linear transformation coefficient (offset)
C	capacitor/capacitance
C_C	reference capacitor
C_M	Miller capacitor
C_{out}	output capacitance
C_{ox}	oxide capacitance per unit area
C_{REF}	reference capacitance
c	polynomial coefficient
E	energy
FQT	frequency trim code
FQT^*	optimal frequency trim code
FoM	figure–of–merit
f	normalized output frequency
f_m	offset frequency
f_{osc}	output frequency
Δf_{osc}	output frequency offset/variation
f_{osc0}	nominal frequency
f^*_{osc0}	optimal nominal frequency
Δf_{oscT}	output frequency drift versus temperature
Δf_{oscV}	output frequency drift versus supply voltage
g_m	transconductance
$g_{m,dp}$	differential pair transconductance
HD_2	second–order distortion parameter

HD_3	third–order distortion parameter
I	current
I_{BC}	comparator bias current
I_{BV2I}	voltage–to–current converter bias current
I_{CTAT}	current complementary to absolute temperature
I_D	device current
ΔI_D	device current difference
I_{DD}	supply current
I_{OUT}	output current
ΔI_{OUT}	output current imbalance
I_{PTAT}	current proportional to absolute temperature
I_{REF}	reference current
ΔI_{REF}	reference current difference
I_{REF0}	nominal reference current
K_T	current factor
ΔK_T	current factor mismatch
k	Boltzmann constant
L	device length
L_{min}	minimum length
LS	line sensitivity
$\mathscr{L}$	phase noise spectrum
M_N	nMOS transistor
M_P	pMOS transistor
n	subthreshold slope factor
P	power
q	electron charge
R	resistor/resistance
R_M	Miller compensation resistor
R_N	resistor with negative first–order temperature coefficient
R_P	resistor with positive first–order temeprature coefficient
R_{REF}	reference resistance/resistor
R_{REF0}	nominal reference resistance
R_S	segment resistance
R^2	coefficient of determination
r_{ds}	dynamic resistance
S	switch
S_{chop}	chopper switch

S_{int}	integrator switch
S_{td}	propagation delay sensitivity
$S_{VOFFrnd}$	random offset voltage sensitivity
$S_{VOFFsys}$	systematic offset voltage sensitivity
T	temperature
ΔT	temperature difference
T_0	nominal temperature
T_0^*	temperature equidistant to midpoint
T_H	high measurement temperature
T_L	low measurement temperature
T_{MAX}	maximum temperature
T_{MIN}	minimum temperature
T_{osc}	oscillation period
ΔT_{osc}	oscillation period variation
TC	temperature coefficient
TCT	temperature coefficient trim code
TCT^*	optimal temperature coefficient trim code
$TC1$	first–order temperature coefficient
$TC1_C$	reference capacitor first–order temperature coefficient
$TC1_f$	output frequency first–order temperature coefficient
$\Delta TC1_f$	first–order temperature coefficient trim value
$\Delta TC1_f^*$	optimal first–order temperature coefficient trim value
$\Delta TC1_f'$	two–point measurement variable
$\delta TC1_f$	first–order temperature coefficient tuning step of the output frequency
$TC1_N$	negative first–order temperature coefficient
$TC1_P$	positive first–order temperature coefficient
$TC1_R$	reference resistor first–order temperature coefficient
$TC1_R^*$	optimal first–order temperature coefficient of the reference resistor
$\delta TC1_R$	first–order temperature coefficient tuning step of the reference resistor
$TC1_{R0}$	nominal first–order temperature coefficient of the reference resistor
$TC1_T$	oscillation period first–order temperature coefficient
$TC1_{tc}$	oscillator core first–order temperature coefficient
$TC2$	second–order temperature coefficient
$TC2_C$	reference capacitor second–order temperature coefficient
$TC2_f$	output frequency second–order temperature coefficient
$TC2_R$	reference resistor second–order temperature coefficient
$TC2_T$	oscillation period second–order temperature coefficient

$TC2_{tc}$	oscillator core second–order temperature coefficient
t	time
Δt	time difference
t_c	oscillator core timing influence
t_D	measurement signal pulse duration
t_d	propagation delay
Δt_d	propagation delay variation
δt_d	residual propagation delay
$t_{startup}$	startup time
V	voltage
VC	integrating voltage
ΔVC	integrating voltage difference
V_{DD}	supply voltage
V_{DS}	drain–source voltage
V_{GS}	gate–source voltage
V_{GS0}	nominal gate–source voltage
ΔV_{IN}	differential input voltage
V_{IN+}	non–inverting terminal voltage
V_{IN-}	inverting terminal voltage
V_{OFF}	offset voltage
ΔV_{OFF}	offset voltage variation
δV_{OFF}	residual offset voltage
V_{OFFrnd}	random offset voltage
V_{OFFsys}	systematic offset voltage
V_{OUT}	output voltage
V_{REF}	reference voltage
V_{REF0}	reference generator output voltage
V_S	source voltage
V_{SS}	ground voltage
V_T	thermal voltage equivalent
V_{THR}	digital threshold voltage
V_{th}	transistor threshold voltage
ΔV_{th}	threshold voltage mismatch
W	device width
X	random variable
x	independent variable
y	dependent variable

α	linear regression slope coefficient
β	linear regression offset coefficient
Δ	difference
λ	output impedance constant
μ	mean value
μ_c	mobility of carrier charges
σ	standard deviation
σ^2	variance
σ_f	frequency uncertainty
σ_{Tosc}	period jitter
$\sigma_y(\tau)$	Allan deviation
σ_y	Allan deviation floor
τ	time window
ϕ	phase

List of Abbreviations

CLK	Clock
CMIR	Current Mirror
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary to Absolute Temperature
CAP	Capacitance
CMP	Comparator
CONV	Conventional
CYC	Cycle
DAC	Digital to Analog Converter
DCL	Digital Compensation Loop
FLL	Frequency–Locked Loop
FoM	Figure–of–Merit
GBW	Gain–Bandwith
IEF	Integrated Error Feedback
IoT	Internet of Things
LC	Inductor–Capacitor
LS	Line Sensitivity
LSB	Least Significant Bit
MC	Monte Carlo
MEMS	Micro–Electronic Mechanical System
MIM	Metal–Insulator–Metal
MOS	Metal Oxide Semiconductor
nMOS	N–Type Metal Oxide Semiconductor
OSC	Oscillator
OTA	Operational Transconductance Amplifier
pMOS	P–Type Metal Oxide Semiconductor
PIP	Polysilicon–Insulator–Polysilicon
PLL	Phase–Locked Loop

PSA	Programmable Switch Array
PTAT	Proportional to Absolute Temperature
PVT	Process–Voltage–Temperature
RC	Resistor–Capacitor
RFID	Radio Frequency Identification
RMS	Root Mean Square
RREF	Reference Resistor
RES	Resistance
SI	Strong Inversion
SoC	System–on–Chip
SR	Set–Reset
SW	switch
TC	Temperature Coefficient
TYP	Typical
VREF GEN	Voltage Reference Generator
V2I	Voltage–to–Current Converter
WI	Weak Inversion
WSN	Wireless Sensor Networks
w–/RC	Core with Replica Comparators
w–/RCC	Core with Replica Chopped Comparator
w–/RI	Core with Replica Integrator
w–/SCC	Core with Self–Compensating Chopped Comparator
2PTC	Two–Point Temperature Calibration
3PTC	Three–Point Temperature Calibration

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Biography

Josip Mikulić was born on December 2nd, 1991, in Imotski, Croatia. He received his B.Sc. degree in electrical engineering in 2013 from the University of Zagreb, Zagreb, Croatia. During his master studies in electronics, he attended a one–year student exchange program at KU Leuven, Belgium, eventually receiving his M.Sc. degree in electrical engineering and information technology in 2015 from the University of Zagreb, Zagreb, Croatia. He is currently employed at ams–OSRAM, where he has been working as an analog design engineer since 2016. His main scientific interests are the research and development of on–chip clock generator circuits. Also, he is engaged in the development of analog and mixed–signal IP blocks (voltage references, V2I converters, ADC/DAC circuits), DFM process rules, analog fault simulation, and AI–aided circuit optimization. Throughout his research career, he authored two journal articles, more than ten conference papers, and five patent submissions in the field of electronics and chip design. He was awarded with "Željka Matutinović – Sunčica" award for the best student work in the field of electronics in 2015 and "Best Paper Award" for the paper at MIPRO 2021 conference (Opatija, Croatia) in the field of Microelectronics, Electronics and Electronic Technology.

List of Publications

Journal Papers

1.J. Mikuli ć, G. Schatzberger and A. Barić, "A 1-MHz Relaxation Oscillator Core Employing a Self-Compensating Chopped Comparator Pair," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 5, pp. 1728-1736, May 2019.

2.J. Mikuli ć, G. Schatzberger and A. Barić, "Post-Manufacturing Process and Temperature Calibration of a 2-MHz On-Chip Relaxation Oscillator," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 10, pp. 4076-4089, Oct. 2021.

Conference Papers

1.J. Mikuli ć, G. Schatzberger and A. Barić, "A 1-MHz Relaxation Oscillator Core Employing a Self-Compensating Chopped Comparator Pair," 2018 IEEE International Sympo-

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Patents

1. J. Mikuli ć, G. Schatzberger, "Oscillator Circuit with Comparator Delay Cancelation", Patent number: (US) 10833654, Type: Grant, Filed: April 9, 2018, Date of Patent: November 10, 2020.
2. J. Mikuli ć, G. Schatzberger, "Oscillator Circuit and Method for Generating a Clock Signal", Patent number: (US) 10742200, Type: Grant, Filed: October 19, 2017, Date of Patent: August 11, 2020.
3. J. Mikuli ć, G. Schatzberger, “Relaxation Oscillator with Comparator Delay and Offset-Voltage Cancellation using Chopped Comparator”, Type: Application, Filed: (WOCN, WODE, WOUS) August 25, 2021.
4. J. Mikuli ć, G. Schatzberger, “Rotating Capacitor Relaxation Oscillator with Offset Voltage Compensation using Chopped Comparator”, Type: Application, Filed: (WO) December 14, 2021.
5. J. Mikuli ć, G. Schatzberger, “Delay and Offset-Voltage Compensated Relaxation Oscillator Core with Replica Integrator”, Type: Application, Filed: (DE) March 17, 2022.

Životopis

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