# Design characterization of multiport electro-optical circuits for broadband voltage measurements in an electromagnetically polluted environment

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FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA

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# PROJEKTIRANJE I KARAKTERIZACIJA VIŠEPROLAZNIH ELEKTROOPTIČKIH SKLOPOVA ZA ŠIROKOPOJASNO MJERENJE NAPONA U ELEKTROMAGNETSKI ZAGAĐENOJ OKOLINI

DOKTORSKI RAD

Mentor: prof. dr. sc. Adrijan Barić

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# About the Supervisor

Adrijan Barić was born in Zagreb in 1958. He received Dipl. Ing. and M.Sc. degrees in electrical engineering from the University of Zagreb (UniZag), Faculty of Electrical Engineering and Computing (FER), Zagreb, Croatia, in 1982 and 1985. He received the PhD degree from the Dublin City University, Ireland, in 1995. Since 1984 he is employed by FER. He was on a two-month research visit at the Rutherford Appleton Laboratory, England, and on a six-month postdoc research visit at the Ghent University, Belgium. He was promoted to Full professor in 2013. He was a principal investigator of two projects funded by the Ministry of Science, Education and Sports of Croatia, one BICRO project, he coordinated the FER research team in one EU FP6 and one FP7 project, as well as several bilateral and multilateral projects with EU companies and universities. He presently coordinates the project "MUNJA" funded by the company ON Semiconductor (Belgium), the project "Sensor Fusion" funded by ams AG (Austria), and the project "Fast switching converters based on GaN devices and resonant architectures" funded by the Croatian Science Foundation HRZZ. He was the President of the Committee for Research, Development and Technology of the UniZag from 2008 to 2011. From 2013 to 2017 he was the President of the Council of Technical Faculties of the UniZag. He was a General Chair or Co-Chair of two IEEE conferences, Finance Chair of one IEEE conference, and Technical Programme Chair of EMC Compo 2011. He is a member of the societies IEEE, HD MIPRO, KoREMA and AMAC-FER. He received Gold Medal "Josip Lončar" for outstanding performance from FER in 2015.

# O mentoru

Adrijan Barić rođen je u Zagrebu 1958. Diplomirao je 1982. i magistrirao 1985. na Fakultetu elektrotehnike i računarstva (FER) Sveučilišta u Zagrebu (SuZ). Doktorirao je na Dublin City University, Irska, 1995. Na FER-u radi od 1984. Bio je gostujući istraživač 2 mjeseca na Rutherford Appleton Laboratory, Engleska, te 6 mjeseci na Ghent University, Belgija, 2000. U redovitog profesora u trajnom zvanju izabran je 2013. Bio je glavni istraživač na dva projekta MZOS-a, jednom BICRO projektu, te je vodio je FER-ov tim u jednom EU FP6 i jednom EU FP7 projektu, te više bilateralnih i multilateralnih projekata s EU tvrtkama i sveučilištima. Trenutno vodi projekt "Sensor Fusion" s ams AG, Austrija, HRZZ projekt "Brzi prekidački pretvornici zasnovani na GaN elementima i rezonantnim arhitekturama", te projekt "MUNJA" s tvrtkom ON Semi, Belgija. Objavio je više od 80 radova u časopisima i zbornicima konferencija iz područja elektroničkih sklopova i elektromagnetske kompatibilnosti. Bio je predsjednik Odbora za istraživanje, razvoj i tehnologiju SuZ-a od 2008. do 2011. Od 2013. do 2017. bio je predsjednik Vijeća tehničkog područja SuZ-a. Bio je predsjedatelj ili supredsjedatelj dvije IEEE konferencije, financijski voditelj jedne IEEE konferencije, te Technical Programe Chair konferencije EMC Compo 2011. Član je udruga IEEE, HD MIPRO, KoREMA i AMAC-FER. Godine 2015. primio je FER-ovu Zlatnu plaketu "Josip Lončar" za svoj rad.

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# Abstract

Broadband electro-optical differential probes for voltage measurements in an electromagnetically polluted environment are designed and characterized. The differential circuit topology is used because of its good immunity to noise. By separating the signal acquisition and signal processing part of the system, a fully isolated measurement system is implemented, where both the measured RF signal and the bias signal are transmitted using an optical connection. Methods for characterization and modelling of multiport circuits at high frequencies are compared. The differential circuits are evaluated by measuring the mixed-mode S-parameters. The differential-mode signal transmission, the common-mode signal transmission, and the common-mode rejection ratio are evaluated.

The probe circuit consists of three main parts: the attenuator, the laser and the bias circuit. Each part of the probe circuit is characterized by performing measurements, electromagnetic and circuit simulations, and circuit modelling. The design of each part of the probe circuit is optimized in order to improve the common-mode rejection ratio of the system. The optimized attenuator circuit, laser and bias circuit layout are implemented in the probe circuit design. Probe circuit characterization structures with different attenuation ratios are characterized. The repeatability of the characteristics between probes with the same probe circuit design is evaluated. The probe circuit layout is optimized and implemented on a connectorized probe with a well-defined ground connection and a fully floating wafer probe. The probes are characterized in the frequency range from 1 MHz to 8 GHz. The impact of ground connection and power supply isolation on the performance of the probes is evaluated. The input impedance of the two probes is characterized and modelled. The simple and low cost measurement system can be implemented as a standalone probe or as a part of an integrated circuit characterization and test environment. The system is designed for characterization of electrostatic discharge waveforms, and can also be used for electromagnetic compatibility measurements.



**Keywords**: attenuator, circuit modelling, common-mode rejection ratio (CMRR), common-mode signal, differential voltage measurement, differential-mode signal, electro-optical system, electromagnetic compatibility (EMC), electrostatic discharge (ESD), noise immunity, power-over-fiber (PoF), vertical-cavity surface-emitting laser (VCSEL)

# Prošireni sažetak

Elektrostatski izboji (engl. *electrostatic discharge* – ESD) su brzi pulsevi s tipično visokom razinom napona. Ovi brzi pulsevi imaju širok frekvencijski opseg koji je tipično u gigaherc-nom području te mogu stvoriti elektromagnetske smetnje u mjernom sustavu. S kontinuiranim razvojem elektroničkih uređaja postoji stalna potreba za unaprjeđenjem tehnika zaštite od elektrostatskih izboja. Mogućnost jednostavnog i praktičnog mjerenja naponskih valnih oblika elektrostatskih izboja pruža korisne informacije dizajnerima integriranih sklopova. Unapređuje se razumijevanje mehanizama propagacije elektrostatskih izboja te se omogućava poboljšanje tehnika potiskivanja i zaštite od elektrostatskih izboja u elektroničkim sklopovima.

Projektiraju se i karakteriziraju širokopojasne elektrooptičke sonde za diferencijsko mjerenje napona u elektromagnetski zagađenoj okolini. Koristi se sklop s diferencijskom topologijom zbog dobre otpornosti na smetnje. Odvajanjem dijela sustava za mjerenje i obradu signala ostvaruje se potpuno izolirani mjerni sustav, gdje se i mjereni radiofrekvencijski signal i signal napajanja prenose optičkom vezom. Svaki dio elektrooptičkog sustava karakterizira se zasebno te se optimizira njegov dizajn sa ciljem poboljšanja faktora potiskivanja zajedničkog signala diferencijskog mjernog sustava. Koristi se iterativni pristup istraživanju pri čemu se rezultati mjerenja, elektromagnetskih i sklopovskih simulacija kombiniraju sa ciljem poboljšanja karakteristika svakog dijela sklopa sonde kroz više faza razvoja dizajna. Uspoređuju se metode za karakterizaciju i modeliranje višeprolaznih sklopova na visokim frekvencijama. Diferencijski sklopovi karakteriziraju se mjerenjem mješovitih raspršnih parametara (engl. *scattering parameters* – S-parameters). Karakterizira se prijenos diferencijskog signala, zajedničkog signala te faktor potiskivanja zajedničkog signala (engl. *common-mode rejection ratio* – CMRR).

Sklop sonde sastoji se od tri osnovna dijela: atenuatora, lasera i sklopa za napajanje. Svaki dio sonde karakterizira se mjerenjem, provođenjem elektromagnetskih i sklopovskih simulacija te modeliranjem. Dizajn svakog dijela sklopa sonde optimizira se sa ciljem poboljšanja faktora potiskivanja zajedničkog signala sustava. Jednostavan mjerni sustav niske cijene može se implementirati u obliku samostalne sonde ili kao dio mjernog okruženja za karakterizaciju i ispitivanje integriranih sklopova. Sustav je projektiran za karakterizaciju valnih oblika elektrostatskih izboja te se može koristiti i za mjerenje elektromagnetske kompatibilnosti (engl. *electromagnetic compatibility* – EMC).

Predstavljene su metode za karakterizaciju višeprolaznih sklopova na visokim frekvencijama mjerenjem raspršnih parametara. Mješoviti S-parametri prikladniji su za karakterizaciju diferencijskih (simetričnih) sklopova nego tradicionalni asimetrični (engl. *single-ended*) S-parametri. Tradicionalni vektorski analizatori mreža projektirani su za mjerenje asimetričnih S-parametara. Čistomodni vektorski analizator mreža (engl. *pure-mode vector network analyzer*) predstavlja koncept za izravno mjerenje mješovitih S-parametara. Iako ne postoje komer-

cijalno dostupni uređaji tog tipa, umjesto toga mogu se koristiti vektorski analizatori mreža s dva generatora. Provodi se usporedba različitih mjernih metoda analizom tipičnih sklopova koji se karakteriziraju u sklopu istraživanja. Usporedbom mjerenja provedenih koristeći tradicionalni četveroprolazni vektorski analizator mreža, četveroprolazni vektorski analizator mreža s dva generatora te tradicionalni dvoprolazni vektorski analizator mreža, demonstrirana je dobra ponovljivost rezultata mjerenja karakteristika diferencijskog i zajedničkog signala. Većina mjerenja u sklopu istraživanja provedena je koristeći dvoprolazni vektorski analizator mreža.

Prezentirana je serijska i paralelna (engl. *shunt*) metoda karakterizacije sklopova. Glavna prednost serijske metode karakterizacije je mogućnost ekstrahiranja parazita prema masi, dok je paralelna metoda prikladnija za karakterizaciju sklopova niske impedancije. Ekstrahirani su nadomjesni modeli otpornika i kondenzatora za površinsku montažu (engl. *surface-mount technology* – SMT) korištenih u atenuatorskom sklopu. Demonstrirano je da otpornici s višim nominalnim otporom imaju veći pad impedancije pri frekvencijama u gigahercnom području, kao posljedica utjecaja parazita. Višeslojni keramički kondenzator namijenjen za upotrebu u RF sustavima modeliran je koristeći dvoprolaznu paralelnu metodu karakterizacije. Ekstrahirani model precizno opisuje utjecaj skin-efekta u frekvencijskom pojasu do 2 GHz.

Atenuatorski sklop se koristi za prigušenje ulaznog RF signala. Izborom vrijednosti otpornika korištenih u atenuatorskom sklopu namješta se faktor atenuacije elektrooptičkog sklopa sonde. Izlazni napon atenuatora ograničen je maksimalnom dopuštenom razinom signala na laserskoj diodi uz koji laser još uvijek radi u linearnom području. Provode se elektromagnetske simulacije i mjerenja S-parametara više iteracija dizajna atenuatorskog sklopa. Unapređuje se stabilnost prigušenja diferencijskog i zajedničkog signala te se smanjuje pretvorba modova. Različite iteracije atenuatorskog sklopa uspoređuju se mjerenjem sklopova sonde s implementiranim različitim verzijama dizajna atenuatora. Optimizacijom dizajna atenuatorskog sklopa faktor potiskivanja zajedničkog signala uvećan je za 10 dB do 20 dB.

Laserska dioda koristi se za pretvorbu izmjerenog RF signala u optički signal. Na taj način poboljašava se otpornost elektrooptičkog mjernog sustava na elektromagnetske smetnje. Koristi se laser s vertikalnom rezonantnom šupljinom (engl. *vertical-cavity surface-emitting laser* – VCSEL) zbog širokog frekvencijskog pojasa, malih dimenzija i mase te niske cijene. Diferencijski RF signal dovodi se na ulaz lasera između anode i katode. Radna točka lasera postavlja se u središte linearnog područja kako bi laser mogao raditi s maksimalnim amplitudama ulaznog signala. Izolirani modul za napajanje (engl. *power-over-fiber* – PoF) i neizolirani modul za napajanje koji je izravno spojen na izvor napajanja karakteriziraju se mjerenjem diferencijske ulazne impedancije. Korištenjem izoliranog napajanja postiže se potpuna galvanska izolacija elektrooptičkog mjernog sustava te se potiskuju smetnje koje dolaze iz izvora napajanja.

Projektira se diferencijski sklop za napajanje koji se koristi za postavljanje statičke radne točke laserske diode. Projektira se više iteracija dizajna sklopa za napajanje koje se karakter-

iziraju provođenjem elektromagnetskih simulacija i mjerenjem diferencijske ulazne impedancije. Najbolje performanse postižu se korištenjem serijske kombinacije ferita i otpornika na ulazu u sklop za napajanje. Na ovaj način koriste se prednosti oba tipa pasivnih komponenata kako bi se postigla visoka ulazna impedancija u širokom pojasu frekvencija. Paraziti se dodatno smanjuju dodavanjem proreza u masi ispod pasivnih komponenata i smanjenjem dimenzija lemnih mjesta (engl. *pad*).

Karakteriziraju se laseri različitih proizvođača i u različitim tipovima pakiranja. Mjeri se prijenos diferencijskog i zajedničkog signala te faktor potiskivanja zajedničkog signala. Korištenjem prospojnog (engl. *through-hole*) pakiranja lasera ostvaruje se najbolja kombinacija faktora potiskivanja zajedničkog signala, mehaničke robusnosti i ponovljivosti karakteristika lasera. Izolacija napajanja nema značajan utjecaj na performanse karakteriziranog lasera. Ekstrahiran je diferencijski nadomjesni model lasera koji se koristi za modeliranje prijenosa diferencijskog i zajedničkog signala te faktora potiskivanja zajedničkog signala. Demonstriran je utjecaj asimetrije parazita prema masi na faktor potiskivanja zajedničkog signala karakteriziranog lasera. Optimizirana je topologija laserskog sklopa te je poboljšan faktor potiskivanja zajedničkog signala. Ostvaren je faktor potiskivanja zajedničkog signala od 30 dB u frekvencijskom pojasu do 3.9 GHz. Karakterizirani laser koristi se u elektrooptičkom sklopu sonde. Odnos signal-šum (engl. *signal-to-noise ratio* – SNR) lasera ovisi o odnosu signal-šum fotodetektora korištenog za mjerenje te ograničava odnos-signal šum elektrooptičkog sklopa sonde.

Početna verzija dizajna sklopa sonde implementirana je na plivajućoj sondi za mjerenje wafera. Ispitane su različite verzije sklopa sonde te su poboljšanja dizajna atenuatorskog sklopa, topologije laserske diode i sklopa za napajanje implementirana u dizajn sklopa sonde. Karakterizirani su sklopovi sonde s različitim stupnjevima atenuacije. Općenito vrijedi, što je niži stupanj atenuacije sonde, to viši faktor potiskivanja zajedničkog signala može biti postignut. Ovo je posljedica činjenice da zajednički signal ne može biti prigušen u istoj mjeri kao i diferencijski signal, zato što postoji doprinos zajedničkom signalu koji nije ovisan o stupnju atenuacije. Korištenje otpornika s nižim nominalnim otporom također rezultira stabilnijim prijenosom diferencijskog signala u širokom pojasu frekvencija i širim 3 dB frekvencijskim opsegom sondi s nižim stupnjem atenuacije. Prisutne su razlike do 5 dB u iznosu faktora potiskivanja zajedničkog signala između sklopova sonde s identičnim topologijama. To je posljedica tolerancija između pasivnih komponenata korištenih u sklopu sonde, laserskih dioda i parazita unesenih procesom lemljenja. Bolju ponovljivost karakteristika između uzoraka sondi moguće je ostvariti korištenjem profesionalnog postupka lemljenja i sastavljanja. Ovo pokazuje utjecaj postupka lemljenja i sastavljanja tiskanih pločica na ponovljivost karakteristika sklopa sonde.

Topologija sklopa sonde optimizirana je sa ciljem poboljšanja faktora potiskivanja zajedničkog signala. Optimizirana topologija sklopa sonde implementirana je na diferencijskoj sondi s pristupnom strukturom s konektorima i spojenom masom te potpuno plivajućoj diferencijskoj

sondi za mjerenje wafera. Unatoč razlikama u pristupnim strukturama i priključcima mase, obje sonde realizirane su u diferencijskoj konfiguraciji gdje se signal diferencijski dovodi na laser. Sonde su projektirane za diferencijska mjerenja valnih oblika elektrostatskih izboja s amplitudama do 100 V (200 $V_{PP}$). Iako se pri radu s elektrostatskim izbojima ne očekuje značajna disipacija snage, maksimalna dopuštena razina efektivnog napona iznosi 14.1 V. Faktor potiskivanja zajedničkog signala sonde za mjerenje wafera s optimiziranim dizajnom sklopa sonde je 10 dB viši u usporedbi s početnim dizajnom sklopa sonde. Spoj sonde prema masi nema značajan utjecaj na prijenos diferencijskog signala, dok je utjecaj na prigušenje zajedničkog signala vrlo značajan. Znatno viši faktor potiskivanja zajedničkog signala postiže se kad je prisutna dobro definirana referenca mase. Sonda sa spojenom masom i plivajuća sonda imaju sličan 3 dB frekvencijski pojas od 3.5 GHz. Međutim, sonda sa spojenom masom ima faktor potiskivanja zajedničkog signala iznad 30 dB u frekvencijskom pojasu do 4.4 GHz, dok plivajuća sonda ima faktor potiskivanja zajedničkog signala iznad 20 dB u frekvencijskom pojasu do 1 GHz.

Ispitan je utjecaj izoliranog napajanja na performanse sondi u obliku smetnji u prijenosu diferencijskog i zajedničkog signala. Utjecaj smetnji koje dolaze iz neizoliranog izvora napajanja i sprege smetnji na električne vodove je relativno malen za sonde sa spojenom masom. Međutim, izolacija napajanja je kritična za u potpunosti plivajuće diferencijske sonde, s obzirom da značajno smanjuje razinu smetnji u prijenosu diferencijskog, a posebno u prijenosu zajedničkog signala. Osim znatno višeg faktora potiskivanja zajedničkog signala u širokom pojasu frekvencija, sonda sa spojenom masom ima i višu i stabilniju diferencijsku i zajedničku ulaznu impedanciju na visokim frekvencijama, uz vrlo nizak parazitni kapacitet. Nominalna diferencijska ulazna impedancija sonde sa spojenom masom iznosi 2095 Ω s parazitnim kapacitetom od 0.13 pF, dok nominalna zajednička ulazna impedancija iznosi 525 Ω s parazitnim kapacitetom od 0.48 pF. Prezentirani jednostavan dizajn sklopa sonde niske cijene moguće je minijaturizirati i implementirati na sondama s različitim tipovima pristupnih struktura i primjenama u sustavima za mjerenje elektrostatskih izboja i elektromagnetske kompatibilnosti.

Brzi pad faktora potiskivanja zajedničkog signala na visokim frekvencijama prisutan je kod svih karakteriziranih sklopova sonde, neovisno o topologiji sklopa sonde i stupnju atenuacije signala. Ovo pokazuje fundamentalno ograničenje dizajna sklopa sonde. Takav pad u faktoru potiskivanja zajedničkog signala nije prisutan u karakteristikama atenuatora i lasera karakteriziranih zasebno. Pad u faktoru potiskivanja zajedničkog signala na visokim frekvencijama rezultat je interakcije između propagacije diferencijskog i zajedničkog signala kroz atenuator i laser, u kombinaciji s prilagođenjem diferencijske i zajedničke impedancije između ta dva sklopa. Faktor potiskivanja zajedničkog signala elektrooptičke sonde moguće je poboljšati optimizacijom izlazne impedancije atenuatora i ulazne impedancije lasera. Kontroliranjem impedancija moguće je sniziti razinu zajedničkog signala na ulazu u laser, u odnosu na razinu diferencijskog signala, na taj način povećavajući faktor potiskivanja zajedničkog signala.

Razvijen je diferencijski elektrooptički sustav za mjerenje napona koji ima dobre karakteristike u frekvencijskom području do nekoliko gigaherca. Sustav koristi jednostavan dizajn sklopa sonde niske cijene. Optička veza koristi se i za radiofrekvencijski signal i za signal napajanja, sa ciljem galvanske izolacije sustava, dopuštajući mu rad u elektromagnetski zagađenoj okolini. Prikazana su ograničenja sustava u smislu stabilnosti prijenosa diferencijskog signala i pada u faktoru potiskivanja zajedničkog signala na visokim frekvencijama. Predložene su izmjene za daljnja unaprjeđenja dizajna svakog dijela sklopa sonde. Umjesto fokusiranja na niske frekvencije pod cijenu performansi na visokim frekvencijama, ostvaren je stabilniji frekvencijski profil faktora potiskivanja zajedničkog signala. Navedene karakteristike postižu se pojednostavljenjem dizajna sklopa, koristeći samo neophodne komponente, što umanjuje fizičke dimenzije sustava, poboljšava performanse i snižava cijenu. Uz karakterizaciju valnih oblika elektrostatskih izboja, razvijeni dizajn sklopa sonde može se prilagoditi i za primjene ispitivanja elektromagnetske kompatibilnosti. Predloženi dizajn omogućava eksperimentiranje s različitim tipovima pristupnih struktura kako bi se smanjile dimenzije sonde, koju bi bilo moguće integrirati u okolinu za ispitivanje integriranih sklopova.

Znanstveni doprinos doktorskog rada:

1. Metodologija za modeliranje elektrooptičkih sklopova i karakterizaciju odziva na diferencijske i zajedničke signale kombinacijom admitancijskih parametara i mješovitih raspršnih parametara.
2. Diferencijski elektrooptički nadomjesni model lasera s vertikalnom rezonantnom šupljinom za procjenu faktora potiskivanja zajedničkog signala.
3. Projektiranje i karakterizacija višeprolaznih širokopojasnih elektrooptičkih diferencijskih sondi za mjerenje napona u elektromagnetski zagađenoj okolini.
4. Usporedna analiza diferencijskih elektrooptičkih naponskih sondi s plivajućom masom i sa spojenom masom za rad u gigahercnom frekvencijskom području.

**Ključne riječi**: atenuator, modeliranje sklopova, faktor potiskivanja zajedničkog signala (CMRR), zajednički signal, diferencijsko mjerenje napona, diferencijski signal, elektrooptički sustav, elektromagnetska kompatibilnost (EMC), elektrostatski izboj (ESD), otpornost na smetnje, power-over-fiber (PoF), laser s vertikalnom rezonantnom šupljinom (VCSEL)

# Contents

# Chapter 1

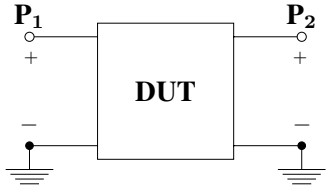
# Introduction

## 1.1 Introduction and overview of the conducted research

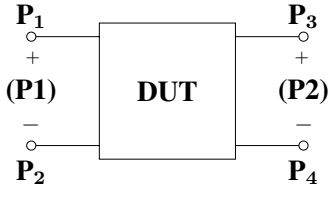
Electrostatic discharges (ESD) are fast pulses with a typically high maximum voltage. These fast pulses have a wide bandwidth that is usually in the gigahertz range, and can create electromagnetic interference in the measurement system [1]. In particular, system-level ESD pulses contain information in the frequency band up to 5 GHz [2]. Given the short duration of ESD pulses, their average power is not a concern. With the continuous development of electronic devices there is a constant need for improvement of ESD protection. The ability to measure ESD voltage waveforms in a simple and practical way provides useful information to integrated circuit designers. It furthers the understanding of the mechanisms of ESD propagation, and allows for improvement of ESD suppression and protection techniques in electronic devices.

Standard electrical probes are susceptible to coupling of electromagnetic noise on the measurement system. Differential circuits have a more robust topology compared to single-ended circuits. Their main advantage is lower sensitivity to system noise and reduced generation of transient noise [3]. A general schematic of a single-ended device is presented in Fig. 1.1a. The device has two physical ports: $P_1$ and $P_2$. In a single-ended system, the signal at each port is referenced to the ground. Single-ended systems are sensitive to interference, because the unwanted signal is directly superposed to the wanted signal, and the two signals are indistinguishable. Additionally, any interference in the ground reference is superposed to signals at all ports sharing the same ground reference.

In a differential system, a pair of physical ports forms a logical differential (balanced) port. The signal at the logical differential port is defined as the difference between the signals at the two physical ports. The idea behind differential signaling is that if two traces are physically close to each other, the same interference is picked up by both signals. Given that the interference is common to both signals, it is cancelled out by making a difference of the two signals. A general schematic of a differential device is presented in Fig. 1.1b. The device shown has four physical ports. The physical ports $P_1$ and $P_2$ form the logical differential port (P1), while the physical ports $P_3$ and $P_4$ form the logical differential port (P2). Differential-mode or common-mode stimulus can be applied to a balanced port. A differential-mode signal is created by two counter-phase signals with the same magnitude, applied to the two physical ports that




(a) Single-ended device under test.




(b) Differential device under test.

**Figure 1.1:** Schematic of a single-ended and a differential device under test.

form the balanced port. A common-mode signal is created by two in-phase signals with the same magnitude, applied to the two physical ports that form the balanced port. The differential-mode signal typically presents the wanted signal, while the common-mode signal typically presents the unwanted signal in the differential system. The ratio between the transmission of the wanted differential-mode signal and the unwanted common-mode signal is called the common-mode rejection ratio (CMRR).

An effective way of making a measurement system more resistant to electromagnetic interference is using electro-optical probes. A general concept of an electro-optical voltage measurement system is presented in Fig. 1.2. In an electro-optical measurement system, the signal acquisition and signal processing stage of the system are separated, achieving galvanic isolation of the measurement system. In this way, the electromagnetic interference present in the measurement environment does not impact the signal processing stage of the system, where the signal obtained using the electro-optical probe is typically digitized using a high speed oscilloscope, or a similar instrument.

The electro-optical measurement system consists of three key parts: the attenuator, the laser and the bias circuit. The attenuator is used to lower the input signal level in order not to overdrive the laser. The laser converts the measured radio frequency (RF) signal into an optical signal, which is transmitted to the photodetector in the signal processing part of the system. The bias circuit is used to set the operating point of the laser. Fully isolated electro-optical probes also use an optical connection for the power-over-fiber (PoF) power supply.

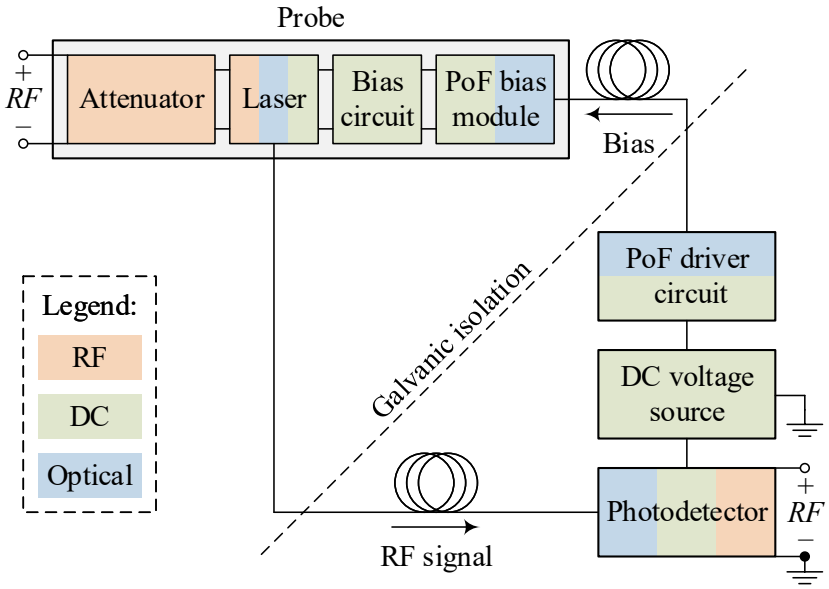



**Figure 1.2:** Differential electro-optical voltage measurement system schematic.

The general concept of electro-optical ESD probes is presented in [4]. Electro-optical probes are most commonly implemented as contactless probes for electric and magnetic field sensing [5–12]. Such probes can be used for measuring radiated emissions for electromagnetic

compatibility (EMC) analysis. The spectrum required by EMC standards for measurements of electromagnetic emissions of integrated circuits is up to 1 GHz, and is expected to be extended in the future [13]. Precise measurements of ESD voltage waveforms require contact measurements to be performed. Given the interference that can be generated by ESD pulses, ESD probes need to be designed to operate in an electromagnetically polluted environment. Using the benefits of a differential circuit topology and an electro-optical measurement system provides the highest level of noise immunity. A circuit design of a differential electro-optical ESD voltage probe is proposed in [2].

This thesis presents the development of a broadband electro-optical differential voltage measurement system. The goal is to develop a simple and low-cost differential system with a stable common-mode rejection ratio up to several gigahertz. While most of the practice in ESD focuses on the quasi-static behaviour, when the ESD pulse has stabilized, the presented system is developed with the goal of being able to investigate the transients and the related risk of overshoots in more detail. The measurement system can be adjusted for different fixture types and is suitable for on-chip ESD waveform characterization, as well as for characterization of waveforms in certain EMC applications.

The probe circuit is realized on a three-layer printed circuit board (PCB), shown in Fig. 1.3. The PCB stack-up uses a combination of an RF Rogers RO4003C substrate and a thicker FR4 substrate. The Rogers RF substrate is used for routing the RF transmission lines, and for placing all the components of the attenuator and the bias circuit. The FR4 substrate is used for mechanical stability of the PCB, and for placing the laser diode and the bias module. The PCB stack-up and dimensions are based on the |Z| Probe® PCB layout. The |Z| Probe® is a type of a broadband wafer probe designed for high-accuracy measurements, with low contact resistance and good impedance control [14]. The same PCB stack-up is used for all the characterization structures designed to evaluate the performance of the parts of the electro-optical probe circuit.

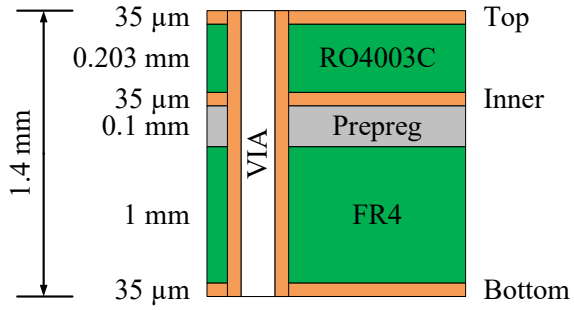



**Figure 1.3:** Characterization PCB stack-up schematic. The copper layers are marked in orange and the dielectric layers are marked in green color (dimensions are not in scale).

The research is conducted by characterizing each individual part of the electro-optical measurement system separately. The design of each part of the electro-optical system is optimized in order to improve the performance of the probe circuit. Circuit simulations, electromagnetic

simulations, and measurements are used to analyze the performance of the individual parts of the probe circuit design. Equivalent circuit models of the components used in the probe circuit are developed. The response of the probe circuit to differential-mode and common-mode input signals is evaluated, as well as the common-mode rejection ratio. The improvements made to the individual parts of the measurement system are implemented into the probe circuit design. Multiple layouts of the probe circuit are characterized and the probe circuit layout is optimized. The optimized probe circuit layout is implemented on a connectorized probe with a well-defined ground connection, as well as a fully floating wafer probe. The performance of the probes is analyzed, as well as the impact of the ground connection and power supply isolation, on the probe performance. Potential areas for performance improvement of the elements of the electro-optical measurement system are suggested.

## 1.2 Scientific contribution of the thesis

The scientific contribution of the thesis is:

1. Methodology combining admittance parameters and mixed-mode scattering parameters for modelling electro-optical devices and for characterizing differential-mode and common-mode response.
2. Differential electro-optical equivalent circuit model of a vertical-cavity surface-emitting laser for common-mode rejection ratio estimation.
3. Design and characterization of multiport broadband electro-optical differential probes for voltage measurements in an electromagnetically polluted environment.
4. Comparative analysis of the floating-ground and connected-ground differential electro-optical voltage probes operating in GHz-range.

## 1.3 Outline of the thesis

The thesis is organized in five chapters.

Chapter 2 presents the different measurement methodologies used to characterize and model multiport circuits. The passive components used in the attenuator circuit are characterized, and their circuit models are extracted. Different attenuator circuit topologies are designed and characterized. The attenuator circuit design is optimized in order to improve the attenuation of the wanted differential-mode signal and the suppression of the unwanted common-mode signal.

Chapter 3 presents the design and characterization of the laser bias circuit, as well as the bias modules used to set the operating point of the laser diode. Laser diodes from different manufac-

turers and in different package types are characterized. The equivalent circuit model of the laser diode used is extracted. Based on the analysis of the circuit model, the laser layout is optimized in order to improve the common-mode rejection ratio. The optimized laser layout is characterized and the signal-to-noise ratio of the electro-optical measurement system is evaluated.

Chapter 4 presents the development of the probe circuit design, from the initial design implemented on the wafer probe, to the implementation of the improvements made to the circuit elements on the probe circuit characterization structure. The probe circuit layout is optimized and implemented on two probes with different fixtures and ground connection types. The probes are characterized by measuring the differential-mode and common-mode signal transmission, as well as the common-mode rejection ratio. The input impedance characteristics of the two probes are analyzed and modelled. The impact of impedance matching between the elements of the probe circuit and the circuit symmetry on the common-mode rejection ratio is analyzed. Time domain measurements are performed using the developed electro-optical probe.

Chapter 5 concludes the thesis.

# Chapter 2

# Multiport measurement methodology and design of attenuator structures

This chapter explores the different measurement methodologies used for circuit characterization at high frequencies. The optimum method is selected based on the characterized circuits and components, and the available measurement equipment. Series and shunt characterization methods are described, which are used to extract equivalent circuit models. Equivalent circuit models of the resistors and capacitors used in the attenuator circuit are presented. The circuit models of the characterized components are used to perform electromagnetic and circuit simulations, and evaluate the proposed circuit designs. The attenuator circuit, located at the input of the probe circuit, must ensure that the laser diode is not overdriven by high input signal levels. Different attenuator circuit designs are simulated and measured. The best attenuator circuit design is selected based on the stability of the differential-mode signal attenuation, and suppression of the unwanted common-mode signal and the mode conversion.

This chapter is structured as follows. Section 2.1 presents the different measurement methodologies used to characterize and model multiport circuits. Section 2.2 explores the passive components used in the attenuator circuit and presents their equivalent circuit models. Section 2.3 discusses the design and characterization of different attenuator circuit topologies. The summary is given in Section 2.4.

This chapter is based on the following papers:

[15] Blecic, R., Stimac, H., Gillon, R., Nauwelaers, B., Baric, A., “Improved Estimation of Radiated Fields of Unintentional Radiators by Correction of the Impedance Mismatch Between a Transverse Electromagnetic Cell and a Hybrid Coupler”, IEEE Transactions on Electromagnetic Compatibility, Vol. 60, No. 6, Dec 2018, pp. 1717-1725.

[16] Štimac, H., Blečić, R., Gillon, R., Barić, A., “Frequency-Domain Characterization and Modelling of a Multi-Layer Ceramic Capacitor for RF Applications”, in 2019 Joint International Symposium on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC), June 2019, pp. 285-288.

[17] Bačmaga, J., Štimac, H., Gillon, R., Barić, A., “High-Frequency Characterization and Parametrized Modelling of DC-Biased Surface-Mount Ferrite Beads for EMI Suppression Applications”, IEEE Transactions on Electromagnetic Compatibility, Vol. 62, No. 6, Dec 2020, pp. 2793-2803.

[18] Bačmaga, J., Štimac, H., Barić, A., “Combined Series and Shunt Characterization for Accurate Resonant Frequency Extraction and Circuit Modelling of Surface-Mount Inductors”, in 2020 IEEE 24th Workshop on Signal and Power Integrity (SPI), May 2020, pp. 1-4.

[19] Bačmaga, J., Štimac, H., Barić, A., “Methodology for Characterization and Modelling of DC-Biased Surface-Mount Ferrite Power Inductors”, in 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Nov 2020, pp. 1-7.

## 2.1 Measurement methodology

High frequency characterization of circuits presents a challenge, given that the standard characterization methods like measuring voltages and currents are not suitable at frequencies in the gigahertz range. Within this thesis a number of different multiport circuits and components are characterized. This includes two-port, three-port and four-port, both active and passive circuits and components. Given that working with differential-mode and common-mode signals is a central topic of the research presented in this thesis, most circuits are characterized as differential (balanced) circuits. However, single-ended circuits are characterized as well.

A number of measurement methods used for characterization and modelling of multiport circuits at high frequencies are explored. An introduction into the concept of single-ended and mixed-mode scattering parameters (S-parameters) is given. When differential-mode and common-mode stimulus is applied to circuits, mixed-mode S-parameters are often more useful than standard single-ended S-parameters. The series and shunt characterization methods are explored, as well as the application of these methods to extract equivalent circuit models.

The differences between a traditional vector network analyzer and a pure-mode vector network analyzer are explained. The pure-mode vector network analyzer is designed for measuring mixed-mode S-parameters directly. Methods for measuring multiport circuits using a more affordable two-port vector network analyzer are explored. Procedures for combining the results and error reduction are discussed. Methods for measuring mixed-mode S-parameters using a traditional vector network analyzer and external components like hybrid couplers, baluns and power dividers are described. The repeatability of measurement results using the same measurement method, as well as using different measurement methods is evaluated on practical examples of circuits characterized within the research presented in this thesis. The best characterization method is selected based on the measurement accuracy, the time required to perform the measurements, and the available measurement equipment.

### 2.1.1 S-parameters

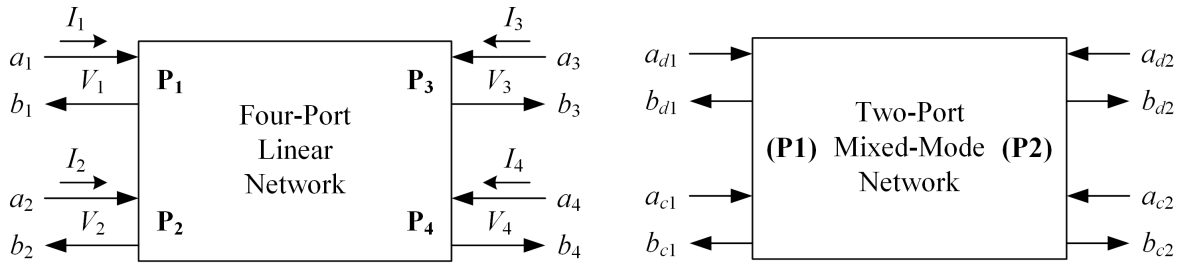
At high frequencies it is very difficult to measure voltages and currents directly. For that reason, scattering parameters are introduced. Standard S-parameters are useful when working with single-ended devices. For applications where differential (balanced) devices are used, the concept of mixed-mode scattering parameters is often more practical [20]. S-parameters are used for measuring linear networks. If active devices are characterized, they need to be measured in small-signal mode of operation.

### Single-ended S-parameters

A device with four physical ports shown in Fig. 2.1 can be viewed as a single-ended device (Fig. 2.1a), or a mixed-mode device (Fig. 2.1b). When characterizing a device as a multiport single-ended device, the physical ports are stimulated one by one, while the other ports are terminated with a matched load. The reflected and transmitted traveling waves are measured. The concept of power waves is introduced in [21]. While traveling waves are physical, measurable and present the solution of Maxwell's equations, power waves are a theoretical concept used in the definition of S-parameters, and are a useful tool for achieving power matching [22]. For a device with $N$ ports shown in Fig. 2.1a, the incident power wave $a_i$ and the reflected power wave $b_i$ at a certain port $i$, are defined using the voltage at the port $V_i$, the current flowing into the port $I_i$, and the reference impedance of the port $Z_i$ as follows [21]:

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{|\mathrm{Re}\{Z_i\}|}}, \quad b_i = \frac{V_i - Z_i^* I_i}{2\sqrt{|\mathrm{Re}\{Z_i\}|}}, \tag{2.1}$$

where $Z_i^*$ represents the complex conjugate of the impedance $Z_i$. In general, the port impedance $Z_i$ can be complex. The power wave definitions can be simplified if all ports share the same complex reference impedance $Z_R$. In practice, $Z_R = Z_0$ is typically used, where $Z_0$ represents the real characteristic impedance, which is typically set to 50 Ω [23].




(a) Four-port single-ended network.

(b) Two-port mixed-mode network.

**Figure 2.1:** Linear network with four physical ports represented in a single-ended configuration (left) and in a mixed-mode configuration with two logical ports (right).

The concept of S-parameters was first introduced in [24]. S-parameters are defined as the ratio between the reflected power wave at the port $i$ and the incident power wave at the port $j$ in an $N$-port linear network as follows [21, 25, 26]:

$$S_{ij} = \left.\frac{b_i}{a_j}\right|_{a_k=0,\ k\neq j}. \tag{2.2}$$

The power wave reflection coefficient looking into the port $i$ is defined as the ratio between the

reflected and the incident power wave at the port $i$ as follows [21]:

$$\Gamma = \frac{b_i}{a_i}. \tag{2.3}$$

The power wave reflection coefficient looking into the port $i$ can also be expressed using the impedance of the port $Z_i$ and the impedance of the termination load $Z_L$ as follows [21]:

$$\Gamma = \frac{Z_L - Z_i^*}{Z_L + Z_i}. \tag{2.4}$$

In the general case, the relationship between the incident and reflected power waves, and the S-parameters can be expressed in the form of a matrix equation as follows [25]:

$$[\boldsymbol{b}] = [\boldsymbol{S}]\,[\boldsymbol{a}]. \tag{2.5}$$

For an $N$-port linear network the S-parameter matrix is expressed as follows [25]:

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & \ddots & & \vdots \\ \vdots & & \ddots & \vdots \\ S_{N1} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_N \end{bmatrix}. \tag{2.6}$$

For a four-port linear network, as shown in Fig. 2.1a, the S-parameter matrix is expressed as follows [27]:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}. \tag{2.7}$$

**Mixed-mode S-parameters**

Mixed-mode S-parameters are developed for combined differential-mode and common-mode normalized power waves [20, 25, 26, 28–37]. The two physical single-ended ports that form a logical balanced port can be viewed as a single differential port with a mixed-mode stimulus, as shown in Fig. 2.1b. The stimulus can be either common-mode, where in-phase signals with the same magnitude are applied to the two physical ports, or differential-mode, where counter-phase signals with the same magnitude are applied to the two physical ports. The mixed-mode S-parameters can be calculated from the standard single-ended S-parameters and vice versa [20, 25–27, 29, 30, 34, 35, 38–40].

For the two-port mixed-mode network shown in Fig. 2.1b, differential-mode and common-mode voltages and currents are defined at each port, using the single-ended voltages and currents shown in Fig. 2.1a. The differential-mode voltages and currents at the balanced ports

are defined using the difference between the voltages and currents at the two physical ports that form the balanced port. The common-mode voltages and currents at the balanced ports are defined using the sum of the voltages and currents at the two physical ports that form the balanced port. The differential-mode and common-mode voltages and currents are defined as follows [20, 25, 28]:

$$V_{d1} = V_1 - V_2, \tag{2.8}$$

$$I_{d1} = \frac{1}{2}(I_1 - I_2), \tag{2.9}$$

$$V_{d2} = V_3 - V_4, \tag{2.10}$$

$$I_{d2} = \frac{1}{2}(I_3 - I_4), \tag{2.11}$$

$$V_{c1} = \frac{1}{2}(V_1 + V_2), \tag{2.12}$$

$$I_{c1} = I_1 + I_2, \tag{2.13}$$

$$V_{c2} = \frac{1}{2}(V_3 + V_4), \tag{2.14}$$

$$I_{c2} = I_3 + I_4. \tag{2.15}$$

Using this concept, differential-mode and common-mode normalized power waves are introduced. They are analogous to the concept of power waves for standard single-ended S-parameters, calculated using (2.1). The differential-mode and common-mode normalized power waves can be expressed using the standard single-ended power waves. Similar to the voltage and currents, the differential-mode power waves are calculated using the difference between the single-ended power waves, while the common-mode power waves are calculated using the sum of the single-ended power waves, as follows [20, 25, 27–29].

$$a_{d1} = \frac{1}{\sqrt{2}}(a_1 - a_2), \tag{2.16}$$

$$a_{c1} = \frac{1}{\sqrt{2}}(a_1 + a_2), \tag{2.17}$$

$$b_{d1} = \frac{1}{\sqrt{2}}(b_1 - b_2), \tag{2.18}$$

$$b_{c1} = \frac{1}{\sqrt{2}}(b_1 + b_2), \tag{2.19}$$

$$a_{d2} = \frac{1}{\sqrt{2}}(a_3 - a_4), \tag{2.20}$$

$$a_{c2} = \frac{1}{\sqrt{2}}(a_3 + a_4), \tag{2.21}$$

$$b_{d2} = \frac{1}{\sqrt{2}}(b_3 - b_4), \tag{2.22}$$

$$b_{c2} = \frac{1}{\sqrt{2}}(b_3 + b_4). \tag{2.23}$$

This relationship between the mixed-mode incident power wave matrix $[\boldsymbol{A}_{mm}]$ and the standard single-ended incident power wave matrix $[\boldsymbol{A}_{std}]$ is expressed as follows [20, 25, 29]:

$$\begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = [\boldsymbol{M}] \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}, \tag{2.24}$$

$$[\boldsymbol{A}_{mm}] = [\boldsymbol{M}]\,[\boldsymbol{A}_{std}]. \tag{2.25}$$

In a similar way, the relationship between the mixed-mode reflected power wave matrix $[\boldsymbol{B}_{mm}]$ and the standard single-ended reflected power wave matrix $[\boldsymbol{B}_{std}]$ is expressed as follows [20, 25, 29]:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = [\boldsymbol{M}] \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}, \tag{2.26}$$

$$[\boldsymbol{B}_{mm}] = [\boldsymbol{M}]\,[\boldsymbol{B}_{std}], \tag{2.27}$$

where the transformation matrix $[\boldsymbol{M}]$ is defined as follows [20, 25, 29]:

$$[\boldsymbol{M}] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}. \tag{2.28}$$

Mixed-mode S-parameters are defined using the differential-mode and common-mode normalized power waves as follows [20, 25, 27–29]:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix}. \tag{2.29}$$

Using (2.25) and (2.27), the relationship between the mixed-mode S-parameter matrix $[\boldsymbol{S}_{mm}]$ and the standard single-ended S-parameter matrix $[\boldsymbol{S}_{std}]$ is expressed as follows [20, 25, 29]:

$$[\boldsymbol{S}_{mm}] = [\boldsymbol{M}]\,[\boldsymbol{S}_{std}]\,[\boldsymbol{M}]^{-1}. \tag{2.30}$$

### Converting single-ended to mixed-mode S-parameters

Mixed-mode S-parameters can be calculated from the measured single-ended S-parameters. A linear network with four physical ports is shown in Fig. 2.1. The network can be represented as a mixed-mode network with two balanced logical ports. Two physical single-ended ports $P_1$ and $P_2$ form the logical balanced port (P1), while the other two physical single-ended ports $P_3$ and $P_4$ form the logical balanced port (P2), for the mixed-mode S-parameter analysis. The mixed-mode S-parameters are calculated from the measured standard single-ended S-parameters as follows [27, 41]:

$$S_{dd11} = \frac{1}{2}\left(S_{11} - S_{21} - S_{12} + S_{22}\right), \tag{2.31}$$

$$S_{dd12} = \frac{1}{2}\left(S_{13} - S_{23} - S_{14} + S_{24}\right), \tag{2.32}$$

$$S_{dd21} = \frac{1}{2}\left(S_{31} - S_{41} - S_{32} + S_{42}\right), \tag{2.33}$$

$$S_{dd22} = \frac{1}{2}\left(S_{33} - S_{43} - S_{34} + S_{44}\right), \tag{2.34}$$

$$S_{cd11} = \frac{1}{2}\left(S_{11} + S_{21} - S_{12} - S_{22}\right), \tag{2.35}$$

$$S_{cd12} = \frac{1}{2}\left(S_{13} + S_{23} - S_{14} - S_{24}\right), \tag{2.36}$$

$$S_{cd21} = \frac{1}{2}\left(S_{31} + S_{41} - S_{32} - S_{42}\right), \tag{2.37}$$

$$S_{cd22} = \frac{1}{2}\left(S_{33} + S_{43} - S_{34} - S_{44}\right), \tag{2.38}$$

$$S_{dc11} = \frac{1}{2}\left(S_{11} - S_{21} + S_{12} - S_{22}\right), \tag{2.39}$$

$$S_{dc12} = \frac{1}{2}\left(S_{13} - S_{23} + S_{14} - S_{24}\right), \tag{2.40}$$

$$S_{dc21} = \frac{1}{2}\left(S_{31} - S_{41} + S_{32} - S_{42}\right), \tag{2.41}$$

$$S_{dc22} = \frac{1}{2}\left(S_{33} - S_{43} + S_{34} - S_{44}\right), \tag{2.42}$$

$$S_{cc11} = \frac{1}{2}\left(S_{11} + S_{21} + S_{12} + S_{22}\right), \tag{2.43}$$

$$S_{cc12} = \frac{1}{2}\left(S_{13} + S_{23} + S_{14} + S_{24}\right), \tag{2.44}$$

$$S_{cc21} = \frac{1}{2}\left(S_{31} + S_{41} + S_{32} + S_{42}\right), \tag{2.45}$$

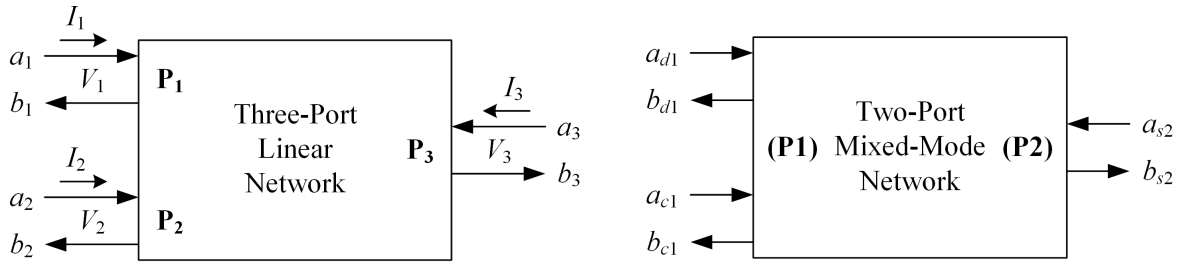
$$S_{cc22} = \frac{1}{2}\left(S_{33} + S_{43} + S_{34} + S_{44}\right). \tag{2.46}$$

A key parameter for characterizing the performance of differential circuits is the common-mode rejection ratio. The CMRR is defined as the ratio between the wanted differential-mode signal transmission and the unwanted common-mode signal transmission. In this thesis the CMRR of four-port circuits with a balanced input and a balanced output, shown in Fig. 2.1, is defined as the ratio between the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-differential mode conversion transmission coefficient $S_{dc21}$, given that a differential load is always connected to the output of such circuits. Alternative definitions of the CMRR for four-port networks are sometimes used, depending on the application, as described in [38, 42]. The CMRR is calculated as follows:

$$\text{CMRR} = \frac{S_{dd21}}{S_{dc21}}. \tag{2.47}$$

A linear network with three physical ports is shown in Fig. 2.2a. The network can be represented as a mixed-mode network with one balanced logical port and one single-ended logical port, as shown in Fig. 2.2b. The two physical single-ended ports $P_1$ and $P_2$ form the logical balanced port (P1). The physical single-ended port $P_3$ forms the logical single-ended port (P2), for the mixed-mode S-parameter analysis. The mixed-mode S-parameters of this three-port network are expressed as follows [27, 36, 41]:

$$\begin{bmatrix} b_{d1} \\ b_{s2} \\ b_{c1} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{ds12} & S_{dc11} \\ S_{sd21} & S_{ss22} & S_{sc21} \\ S_{cd11} & S_{cs12} & S_{cc11} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{s2} \\ a_{c1} \end{bmatrix}. \tag{2.48}$$




(a) Three-port single-ended network.

(b) Two-port mixed-mode network.

**Figure 2.2:** Linear network with three physical ports represented in a single-ended configuration (left) and in a mixed-mode configuration with two logical ports (right).

The mixed-mode S-parameters of the three-port network are calculated from the measured standard single-ended S-parameters as follows [27, 41]:

$$S_{ss22} = S_{33}, \tag{2.49}$$

$$S_{sd21} = \frac{1}{\sqrt{2}}\left(S_{31} - S_{32}\right), \tag{2.50}$$

$$S_{sc21} = \frac{1}{\sqrt{2}}(S_{31} + S_{32}), \tag{2.51}$$

$$S_{ds12} = \frac{1}{\sqrt{2}}(S_{13} - S_{23}), \tag{2.52}$$

$$S_{cs12} = \frac{1}{\sqrt{2}}(S_{13} + S_{23}), \tag{2.53}$$

$$S_{dd11} = \frac{1}{2}(S_{11} - S_{12} - S_{21} + S_{22}), \tag{2.54}$$

$$S_{dc11} = \frac{1}{2}(S_{11} + S_{12} - S_{21} - S_{22}), \tag{2.55}$$

$$S_{cd11} = \frac{1}{2}(S_{11} - S_{12} + S_{21} - S_{22}), \tag{2.56}$$

$$S_{cc11} = \frac{1}{2}(S_{11} + S_{12} + S_{21} + S_{22}). \tag{2.57}$$

The common-mode rejection ratio of three-port circuits with a balanced input and a single-ended output, as shown in Fig. 2.2, is defined as the ratio between the wanted differential-mode signal transmission coefficient $S_{sd21}$ and the unwanted common-mode signal transmission coefficient $S_{sc21}$. The CMRR is calculated as follows [42]:

$$\text{CMRR} = \frac{S_{sd21}}{S_{sc21}}. \tag{2.58}$$

### 2.1.2 S-parameter measurements

#### Traditional vector network analyzer

A device for measuring S-parameters is called a vector network analyzer (VNA) [43, 44]. A VNA can measure both the magnitude and phase of S-parameters. A VNA needs to be calibrated before performing measurements, by measuring a set of well-defined calibration standards [45–49]. A traditional VNA performs measurements by stimulating each port individually, while the remaining ports are terminated with a matched load [29]. The reflected and transmitted traveling waves are measured in order to calculate the standard single-ended S-parameters. Vector network analyzers with two or four physical ports are most commonly used. Due to the higher price of four-port vector network analyzers, more affordable two-port vector network analyzers are often used. When a two-port VNA is used to measure a multiport circuit, more than one measurement needs to be performed. The measurement is performed as a series of two-port measurements [30, 50]. The remaining ports are terminated with a matched load, as shown in Fig 2.3.

For example, in order to measure a four-port circuit with physical ports $P_1$–$P_4$, as shown in Fig. 2.1a, a four-by-four S-parameter matrix (2.7) is generated, containing 16 elements. When a measurement of a four-port circuit is performed using a two-port VNA, six two-port measurements need to be performed, each for a combination of two ports: $P_1$ and $P_2$, $P_1$ and $P_3$, $P_1$

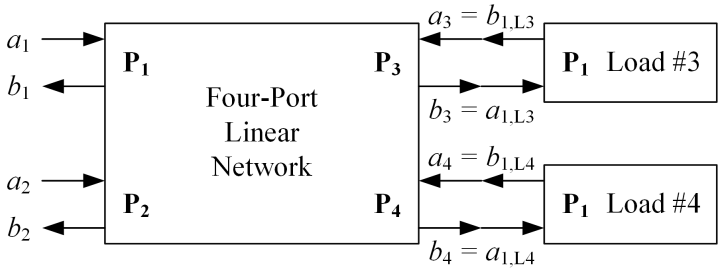



**Figure 2.3:** Two-port measurement of a four-port linear network.

and $P_4$, $P_2$ and $P_3$, $P_2$ and $P_4$, $P_3$ and $P_4$. Six two-by-two S-parameter matrices are generated. These matrices need to be combined to form a four-by-four S-parameter matrix of the measured circuit. The downside of using a two-port VNA compared to a four-port VNA is a more complicated and prolonged measurement procedure, where a series of measurements needs to be performed, instead of a single measurement. Given that the ports of the VNA are disconnected and reconnected to the device under test multiple times, this has a negative effect on the measurement accuracy and repeatability.

When performing two-port measurements of a four-port device, the return loss $S_{ii}$ at each port $i$ is measured three times. In an ideal case, all three measurement results would be the same, however that is usually not the case in practice. When combining the results, one option is to take only one of the measurements into account. An alternative approach is to reduce these inconsistencies by making an average of the three measurements, and use that result in the combined matrix [50]. For example, the return loss at port $P_1$ is calculated as the average of measurements performed at ports $P_1$ and $P_2$, $P_1$ and $P_3$, and $P_1$ and $P_4$ as follows:

$$S_{11,avg} = \frac{S_{11,\mathrm{M12}} + S_{11,\mathrm{M13}} + S_{11,\mathrm{M14}}}{3}. \tag{2.59}$$

For symmetrical devices, an average of the return loss values on all ports can be calculated [50].

Another thing to note when combining the measurement results is the impedance of the loads used to terminate the unused ports during the two-port measurements. These ports should be terminated with a matched load. However, in practice the loads are not ideal and there is some mismatch between the characteristic impedance and the load impedance. An approach for renormalizing the scattering parameter matrix is described in [50, 51]. Aside from normalizing non-ideal terminations, this procedure can also be used in cases where highly reflective terminations are used, in order to raise the value of the reflected signals above the noise level [51].

### Pure-mode vector network analyzer

In order to thoroughly characterize differential (balanced) circuits, the differential-mode, common-mode and mode conversion responses need to be measured. These responses are repre-

sented using mixed-mode S-parameters [28]. While a traditional VNA performs measurements of single-ended S-parameters directly, a concept called the pure-mode vector network analyzer (PMVNA) measures mixed-mode S-parameters directly [29, 39, 52–55]. This is achieved by stimulating each mode individually, instead of stimulating each physical port individually, which is the case with a traditional VNA [29]. The schematic of the PMVNA concept is shown in Fig. 2.4. The calibration procedure for a PMVNA is described in [53].

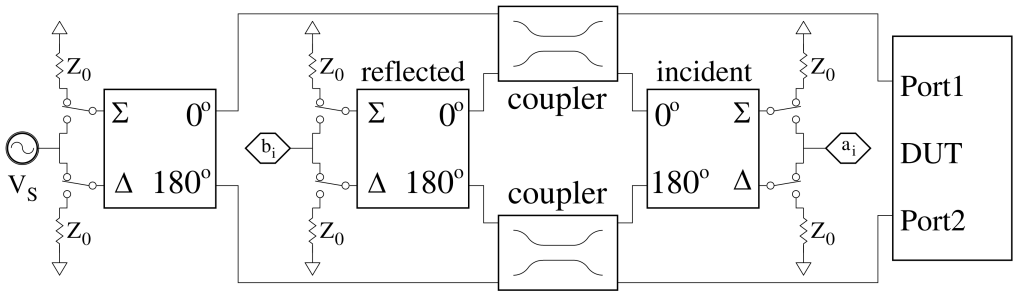



**Figure 2.4:** Pure-mode vector network analyzer concept schematic, image sourced from [55].

Measurements of a differential circuit using a PMVNA display a significantly lower level of uncertainty, compared to a traditional VNA. This is particularly notable for mode conversion mixed-mode S-parameters, $S_{cd}$ and $S_{dc}$ [39, 56, 57]. A full implementation of the PMVNA concept is not yet commercially available [55]. However, there are commercially available dual-source VNAs that can produce either pure-differential-mode or pure-common-mode drive in both the forward and reverse direction [54, 58]. These network analyzers can be used to measure balanced devices more accurately.

### Hybrid couplers

In order to characterize a differential circuit using a traditional single-ended vector network analyzer, external hybrid couplers, power dividers or baluns can be used [29, 31, 41, 52, 59–63]. A hybrid coupler has two input and two output ports. A hybrid coupler with a 180 degree phase shift can generate either in-phase signals or counter-phase signals at the two output ports, from a single input port. Alternatively, the hybrid can be used to either make a sum or a difference of the two input signals, at the output port [15]. When a hybrid coupler with a 180 degree phase shift is used with a traditional single-ended four-port VNA, the system can generate both differential-mode and common-mode stimulus [59]. Both input ports of the hybrid coupler can be used simultaneously to generate both a differential-mode and a common-mode signal component at the output ports, as shown in Fig. 2.5. With known S-parameters of the hybrid coupler, the impact of the coupler can be de-embedded from the measurement results [49].

The same procedure can be used with a two-port VNA, if a two-port differential device is measured [61, 63], as shown in Fig. 2.6. If a four-port differential device is measured, two sets of measurements need to be performed, one with a differential-mode stimulus, and the second

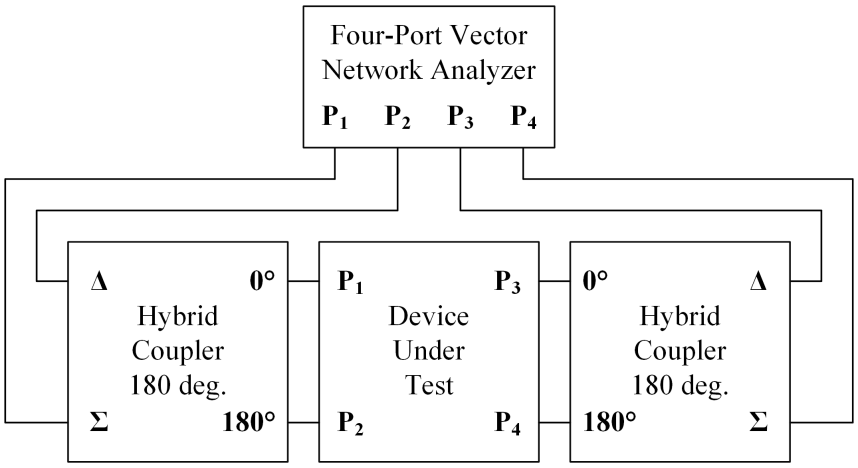



**Figure 2.5:** Mixed-mode S-parameter measurement setup using a four-port vector network analyzer and two hybrid couplers with a 180 degree phase shift.

with a common-mode stimulus, generated from a single input port of the hybrid coupler. The other input port of the hybrid coupler is terminated with a matched load. In a similar way, the differential-mode and common-mode response of the characterized device need to be measured separately, using a second hybrid coupler.

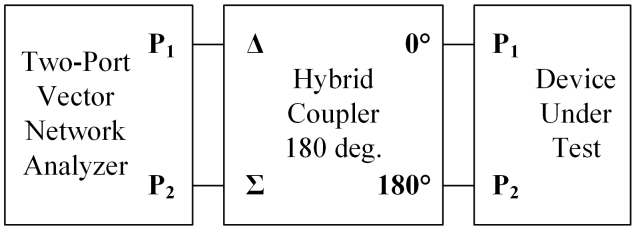



**Figure 2.6:** Mixed-mode S-parameter measurement setup using a two-port vector network analyzer and a hybrid coupler with a 180 degree phase shift.

Instead of using a hybrid coupler, baluns and power dividers can be used [31, 41, 60–62]. A balun can be used to generate a differential-mode stimulus, while a power divider can be used to generate a common-mode stimulus. Using these circuits, two sets of measurements can be performed. For some applications, it is only necessary to measure either the differential-mode or the common-mode response of the differential device under test, in which case only one of the aforementioned circuits is used. In some cases, baluns and power dividers can be a part of measurement probes, which means that their S-parameters cannot be measured separately [31]. In such cases, other calibration approaches are used [41].

Hybrid couplers, baluns and power dividers that are used in practice are not ideal. Instead of generating perfect differential-mode and common-mode signals, there is a certain amplitude and phase imbalance between the two signals. This means that in a differential-mode measurement, aside from the differential-mode signal, an unwanted common-mode signal is generated, and vice versa. This unwanted amplitude and phase imbalance of the generated signals affects the

measurement accuracy and introduces measurement uncertainty [64, 65]. Additional components used in the measurements setup, like cables and adapters, introduce further amplitude and phase imbalance. The same problem also occurs in pure-mode vector network analyzers [54].

### 2.1.3 Measurement methodology verification

The S-parameter measurement methods using different vector analyzer concepts that have been described Section 2.1.2 are compared on three practical examples. The goal is to verify the results of the different measurement methods for the devices characterized within the scope of this thesis. The three devices that are characterized are a four-port attenuator circuit, a three-port laser diode and a hybrid coupler with a 180 degree phase shift.

#### Attenuator circuit

The schematic of the characterized four-port differential attenuator circuit is shown in Fig. 2.7. The device has four physical ports which form two mixed-mode logical ports, as shown in Fig. 2.1. The attenuator circuit is characterized using three different measurement methods. The first measurement is performed using a traditional four-port vector network analyzer [66]. Based on the measured single-ended S-parameters, mixed-mode S-parameters are calculated using (2.31)–(2.46). The second measurement is performed using a dual-source four-port vector network analyzer [67]. This concept for measuring mixed-mode S-parameters using a dual-source four-port VNA is called the true differential measurement mode (TDMM) [58]. Mixed-mode S-parameters are measured directly. The third measurement is performed using a traditional two-port vector network analyzer [68]. A set of six two-port measurements is performed, each for a combination of two physical ports. The measurement results are combined into a four-by-four S-parameter matrix using the technique described in [30, 50]. The mixed-mode S-parameters are calculated in the same way as for the measurement using the traditional four-port VNA.

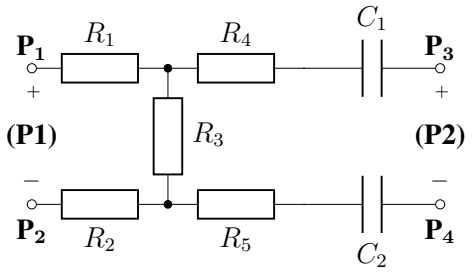
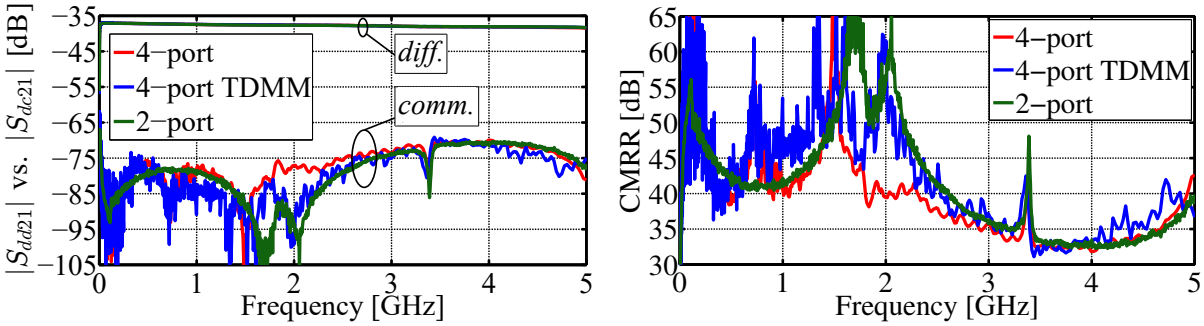



**Figure 2.7:** Four-port differential attenuator circuit schematic.

The comparison of the measurement results is shown in Fig. 2.8. Two characteristic mixed-mode S-parameters are compared. The first value is the differential-to-differential transmission

coefficient $S_{dd21}$, which determines the attenuation level of the attenuator. The second value is the common-to-differential transmission coefficient $S_{dc21}$, which quantifies the unwanted mode conversion from the common-mode signal at the input to a differential-mode signal at the output. The measurement results for the differential-to-differential signal transmission $S_{dd21}$ show very good repeatability. No significant difference can be observed between the three measurement methods. The general trend of the common-to-differential mode conversion $S_{dc21}$ measurements is similar using all three methods. Some differences are observed between the measurements in terms on noise in the characteristic, as well as the resonances. This is expected, given the low level of the measured signal, which is close to the noise floor of the measurement system, making it more susceptible to measurement uncertainty, as explained in Section 2.1.2.




(a) Differential-to-differential and common-to-differential signal transmission.

(b) Common-mode rejection ratio.

**Figure 2.8:** Characteristics of the attenuator circuit measured using a traditional four-port VNA, a dual-source four-port VNA using the TDMM, and a traditional two-port VNA. The magnitude of the differential-to-differential transmission coefficient $S_{dd21}$, the common-to-differential transmission coefficient $S_{dc21}$, and the common-mode rejection ratio (CMRR) are compared.

The general trend of the common-mode rejection ratio is similar using all three measurement methods. Given that the CMRR is defined as the ratio between the two transmission coefficients using (2.47), the impact of the common-to-differential mode conversion has a dominant effect on the CMRR characteristic. At frequencies where the CMRR value is lower, the fitting between the measurement methods is very good. At frequencies where the CMRR value is above 45 dB, there is more discrepancy between the characteristics, because precise CMRR measurements require very low magnitude and phase uncertainty of the measurement system. The magnitude and phase uncertainty are dependent on the VNA model used to perform the measurements, the output power, frequency range, calibration method and the measurement setup [66–68].

### Laser diode

A sample laser diode is characterized using the same three methods used to characterize the attenuator circuit. A schematic of the laser measurement setup is shown in Fig. 2.9. The physical port $P_1$ is connected to the laser anode, the physical port $P_2$ is connected to the laser cath-

ode, and the physical port $P_3$ is connected to the output of the photodetector. The physical ports $P_1$ and $P_2$ form the logical balanced port (P1), and the physical port $P_3$ forms the logical single-ended port (P2), as shown in Fig. 2.2. Using a traditional four-port vector network analyzer [66], three-port single-ended S-parameters are measured, and the mixed-mode S-parameters are calculated using (2.49)–(2.57). The dual-source four-port VNA [67] is used to measure the mixed-mode S-parameters directly. Using a traditional two-port vector network analyzer [68], a set of three two-port measurements is performed, each for a combination of two physical ports. The measurement results are combined into a three-by-three S-parameter matrix using the technique described in [30, 50]. The mixed-mode S-parameters are calculated in the same way as for the measurement using the traditional four-port VNA.

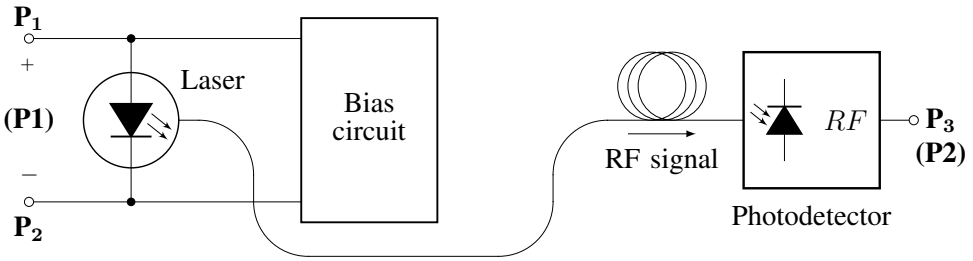
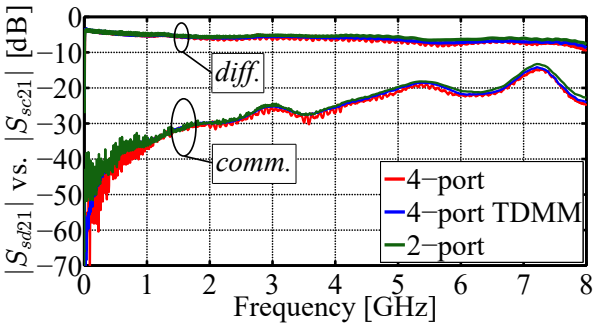


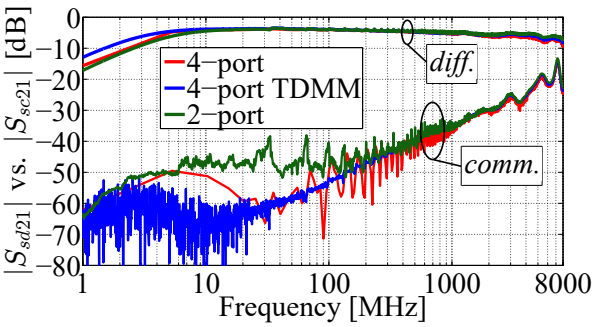

**Figure 2.9:** Three-port laser diode measurement setup schematic.

The mixed-mode S-parameter measurement results are compared in Fig. 2.10. There is very good repeatability between the three measurement methods for the differential-mode transmission coefficient $S_{sd21}$. Only the four-port TDMM measurement shows a slightly lower lower cutoff frequency. The measurement repeatability is also very good for the common-mode transmission coefficient $S_{sc21}$ at higher frequencies. There are more significant differences between the measurement methods for frequencies below 100 MHz. Due to the sensitive nature of the laser characterization setup there is always some difference between the measurements, because the common-mode signal is very sensitive to the twisting and bending of the cables in the measurement setup. Additionally, the low level of the common-mode signal makes it difficult to measure accurately, particularly at low frequencies where the measurement accuracy of the VNA is the worst [66–68]. By comparing the CMRR results it is observed that all three measurement methods show very good repeatability for frequencies above 1 GHz. At frequencies below 100 MHz the differences are more pronounced, because such high CMRR values are very difficult to measure, as they require the measurement system to have extremely low magnitude and phase measurement uncertainty. The magnitude and phase uncertainty are typically the worst at low frequencies, close the the minimum frequency of the VNA [66–68]. This is also the frequency range where the CMRR is typically the highest.

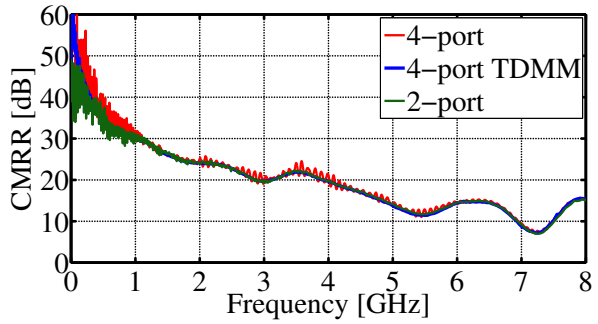
As for the attenuator circuit, it is demonstrated that measuring the low level common-mode signal, and in turn the high CMRR, is very difficult. The CMRR can be measured accurately and with good repeatability for lower CMRR values. In general, that is the most important



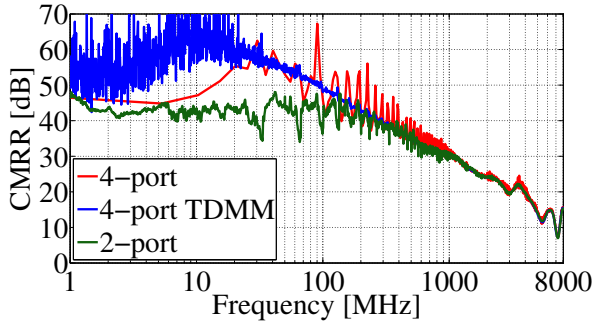

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).



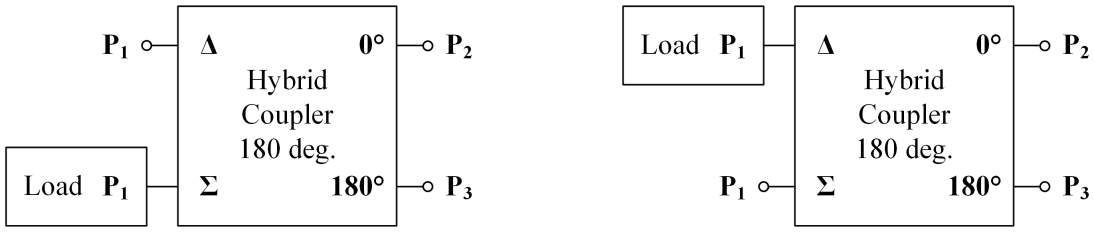

(d) Common-mode rejection ratio (log. frequency).

**Figure 2.10:** Characteristics of the laser diode measured using a traditional four-port VNA, a dual-source four-port VNA using the TDMM, and a traditional two-port VNA. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

range of values, as it represents the frequency range where the design should be improved and the CMRR increased. At low frequencies where the CMRR is very high, particularly above 40 dB, the actual value of the CMRR is not critical for the performance of the electro-optical measurement system. Given this reason, as well as the lower cutoff frequency of 2 MHz of the photodetector model used [69], the analysis of the measurements presented in this thesis is typically focused at frequencies above 100 MHz.

### Hybrid coupler

A hybrid coupler with a 180 degree phase shift is characterized. The specified frequency bandwidth of the hybrid coupler is from 1 GHz to 12.4 GHz. The hybrid coupler can be used to generate either two counter-phase signals, creating a differential-mode stimulus at a balanced port (Fig. 2.11a), or it can be used to generate two in-phase signals, creating a common-mode stimulus at a balanced port (Fig. 2.11b). The differential-mode and the common-mode hybrid coupler measurement setup are characterized using two measurement methods. Using a traditional four-port vector network analyzer [66], three-port single-ended S-parameters are measured. Using a traditional two-port vector network analyzer [68], a set of three two-port measurements is performed, each for a combination of two physical ports. The measurement

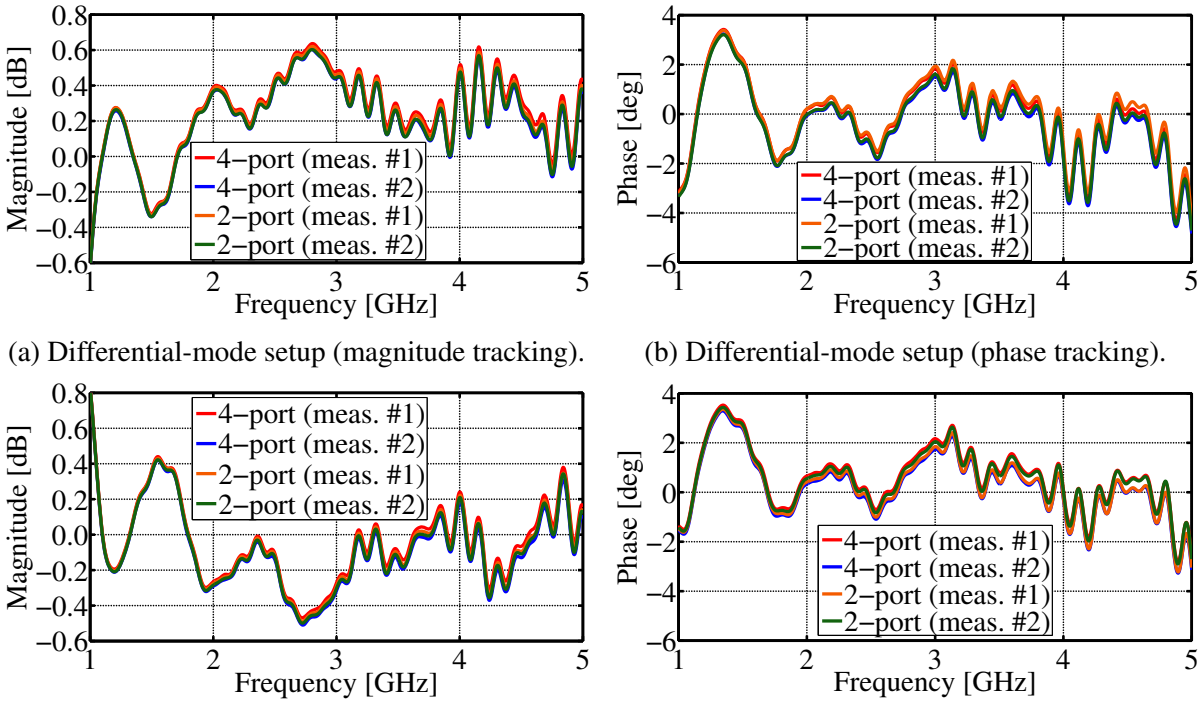



(a) Differential-mode measurement setup. (b) Common-mode measurement setup.

**Figure 2.11:** Hybrid coupler with a 180 degree phase shift differential-mode and common-mode measurement setup schematic.

results are combined into a three-by-three S-parameter matrix using the technique described in [30, 50]. Two sets of measurements are performed using each measurement method, in order to determine the repeatability of the measurement results. The magnitude and phase imbalance characteristics of the hybrid coupler differential-mode and common-mode measurement setup are calculated from the single-ended S-parameter measurements.

The magnitude and phase tracking measurement results of the hybrid coupler differential-mode and common-mode measurement setup are shown in Fig. 2.12. The magnitude tracking of the differential-mode measurement setup is within ±0.6 dB, while the phase tracking is within ±5 deg. The magnitude tracking for the common-mode measurement setup is within ±0.8 dB, while the phase tracking is within ±4 deg. The repeatability of the results with the two




(a) Differential-mode setup (magnitude tracking). (b) Differential-mode setup (phase tracking).

(c) Common-mode setup (magnitude tracking). (d) Common-mode setup (phase tracking).

**Figure 2.12:** Characteristics of the hybrid coupler differential-mode and common-mode measurement setup measured using a traditional four-port VNA and a traditional two-port VNA. Two sets of the magnitude tracking and phase tracking measurement results are compared.

different measurement methods is consistent with the repeatability between the measurements performed using the same method. Small differences between the measurements performed using the same method are expected when reconnecting the components, as explained in Section 2.1.2.

It is demonstrated that the three compared measurement methods show good repeatability for all the characterized structures. Despite the two-port measurement method being the most sensitive, as it requires multiple reconnections to be made in order to perform the required set of measurements, it shows good repeatability for all types of characterized structures. Given that only a traditional two-port VNA is available in the laboratory where the research is conducted, it will be used for most of the S-parameter measurements presented in this thesis. Where available, measurements using a dual-source four-port VNA with the TDMM option will be presented. Using a combination of single-ended S-parameter measurements is chosen over performing measurements using hybrid couplers.

Although hybrid couplers allow differential-mode and common-mode stimulus to be generated directly, broadband hybrid couplers that would cover the entire measurement frequency range are not available. Instead, using multiple hybrid couplers to cover the entire measurement frequency range would be required. This greatly complicates the measurements, as it requires a large number of reconnections and individual measurements to be performed. Additionally, the nature of measurements using hybrid couplers, as well as the fact that they require the usage of additional cables and adapters, introduces additional measurement uncertainty and makes the de-embedding procedure very complicated. On the other hand, single-ended S-parameter measurements can be de-embedded in a simple way and the mixed-mode S-parameters can be calculated directly.

### 2.1.4 Modelling methodology

Two main methodologies for circuit modelling explored in this thesis are the series characterization method (Fig. 2.13) and the shunt characterization method (Fig. 2.14). The main benefit of the series characterization method is that the port-to-ground parasitics can be extracted. The main downside of the series characterization method is that the impedance of the fixture can mask the impedance of the device under test (DUT), when characterizing low impedance devices. The series method requires accurate de-embedding of the fixture to be performed.

The shunt characterization method can be performed as a one-port or as a two-port measurement. Given that the measurement uncertainty is worse for reflection coefficient measurements than for transmission coefficient measurements, the one-port shunt characterization method is typically not used [70]. The main benefit of the shunt characterization method is the ability to accurately measure low impedance DUTs. The main downside of the shunt characterization method is that one solder pad of the DUT is shorted to the ground and the related port-to-ground

parasitics cannot be extracted. The parasitics related to the other solder pad are effectively connected in parallel to the DUT, which can mask the impedance of the DUT under certain conditions. This makes the shunt characterization method unsuitable for extracting the port-to-ground parasitics. In order to extract the most accurate circuit models, it is best to combine both the series and the shunt characterization method, as described in [17–19]. For circuits that are differentially driven, using the shunt characterization method is not suitable, as it converts the differential circuit configuration into a single-ended configuration.

### Series characterization method

The measurement setup used for the series characterization method is shown in Fig. 2.13a. The port $P_1$ of the DUT is connected to the port $P_1'$ of the VNA, while the port $P_2$ of the DUT is connected to the port $P_2'$ of the VNA. Two-port S-parameters of the DUT are measured. The S-parameters are converted to admittance parameters (Y-parameters) [23]. The characterized DUT is modelled using the admittance Π-model, shown in Fig. 2.13b. The Π-model elements are calculated using the Y-parameters as follows:

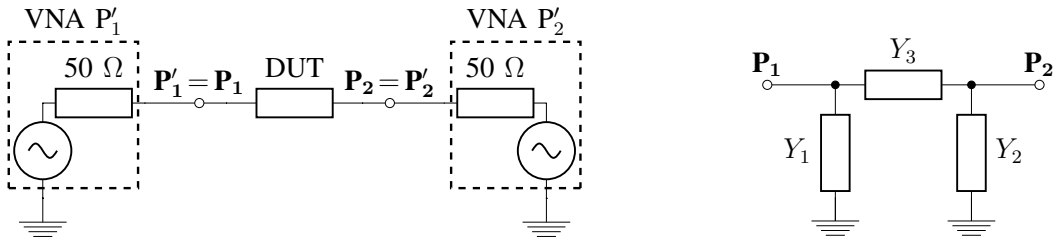
$$y_{12,avg} = \frac{y_{12} + y_{21}}{2}, \tag{2.60}$$

$$Y_1 = y_{11} + y_{12,avg}, \tag{2.61}$$

$$Y_2 = y_{22} + y_{12,avg}, \tag{2.62}$$

$$Y_3 = -y_{12,avg}. \tag{2.63}$$

The Π-model is used to create an equivalent electrical circuit model of the DUT. The Π-model shunt elements $Y_1$ and $Y_2$ model the port-to-ground paths, which are typically related to solder pad parasitics. The Π-model series element $Y_3$ models the port-to-port path, which is typically related to internal structure of the DUT.




(a) Series characterization method.

(b) Admittance Π-model.

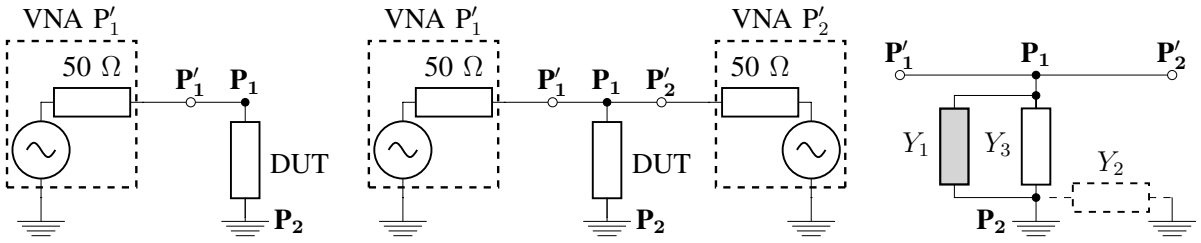
**Figure 2.13:** Series characterization method measurement setup and the extracted circuit model.

### Shunt characterization method

The measurement setup used to perform the one-port shunt characterization method is shown in Fig. 2.14a, while the two-port shunt characterization method measurement setup is shown in Fig. 2.14b. The port $P_1$ of the DUT is connected between the ports $P'_1$ and $P'_2$ of the VNA. The port $P_2$ of the DUT is connected to the ground. Two-port S-parameters are measured and converted to impedance parameters (Z-parameters) [23]. The impedance of the DUT is calculated using the Z-parameters as follows:

$$z_{12,avg} = \frac{z_{12} + z_{21}}{2}, \tag{2.64}$$

$$Z_{DUT} = z_{12,avg}. \tag{2.65}$$




(a) 1-port shunt method. (b) 2-port shunt characterization method. (c) Extracted shunt circuit.

**Figure 2.14:** Shunt characterization method measurement setup and the extracted circuit connection.

For a DUT represented using the admittance Π-model, the connection of the Π-model elements when performing the two-port shunt characterization method is shown in Fig. 2.14c. The port-to-ground Π-model element $Y_2$ is shorted to the ground and is masked when performing the shunt characterization method. The impedance of the DUT is primarily determined by the port-to-port Π-model element $Y_3$. However, when using the shunt characterization method, the port-to-ground Π-model element $Y_1$ is effectively connected in parallel to the element $Y_3$. The impedance of the DUT extracted using the shunt characterization method can be calculated using the Π-model elements as follows:

$$Z_1 = \frac{1}{Y_1}, \tag{2.66}$$

$$Z_2 = \frac{1}{Y_2}, \tag{2.67}$$

$$Z_3 = \frac{1}{Y_3}, \tag{2.68}$$

$$Z_{DUT} = Z_3 \parallel Z_1. \tag{2.69}$$

If the shunt impedance $Z_1$ in the Π-model is comparable to the series impedance $Z_3$, the internal impedance of the DUT can be masked, otherwise $Z_{DUT} \approx Z_3$. By combining both the

series and the shunt characterization method, the series characterization method can be used to extract the value of the shunt impedances $Z_1$ and $Z_2$. If the impact of the shunt impedance $Z_1$ on the impedance of the DUT extracted using the shunt characterization method $Z_{DUT}$ is significant, it can be corrected, in order to extract the value of the series impedance $Z_3$, as described in [17–19]. The shunt characterization method is typically used in order to extract the impedance T-model of the DUT [23].

### Input impedance characterization

The input impedance of the DUT is analyzed based on the S-parameter measurements. The differential-mode input impedance $Z_{d1}$ at the balanced logical port (P1) is the total impedance seen between the physical ports $P_1$ and $P_2$, as illustrated in Fig. 2.15a. The common-mode input impedance $Z_{c1}$ at the logical port (P1) is the effective shunt impedance seen from the physical ports $P_1$ and $P_2$ towards the ground, as illustrated in Fig. 2.15b.


(a) Differential-mode input impedance.

(b) Common-mode input impedance.

**Figure 2.15:** Differential-mode input impedance $Z_{d1}$ and common-mode input impedance $Z_{c1}$ schematic.

The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ are calculated using the mixed-mode S-parameter matrix at the logical port (P1) obtained using (2.54)–(2.57). Taking into account the configuration of the circuits that are characterized in this thesis under differential-mode and common-mode drive conditions, as well as the mode conversion, the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the DUT are defined as follows [55]:

$$Z_{d1} = 2Z_0 \frac{S_{dd11} - S_{cc11} + 1 - \Delta}{1 + \Delta - S_{dd11} - S_{cc11}}, \tag{2.70}$$

$$Z_{c1} = \frac{Z_0}{2} \frac{S_{dd11} + S_{cc11} + 1 + \Delta}{1 - \Delta + S_{dd11} - S_{cc11}}, \tag{2.71}$$

where $Z_0 = 50\ \Omega$ is the characteristic impedance, and $\Delta$ is the determinant of the mixed-mode S-parameter matrix at the logical port (P1):

$$\Delta = S_{dd11}S_{cc11} - S_{dc11}S_{cd11}. \tag{2.72}$$

The differential-mode input impedance $Z_{d1}$ can also be calculated directly using the two-port standard single-ended S-parameter measurement results. Similar to the concept of the power

wave reflection coefficient for standard single-ended S-parameters defined using (2.4), the reflection coefficient can be defined for mixed-mode power waves [55]. The differential-mode reflection coefficient at the balanced logical port (P1) is calculated as follows [71]:

$$\Gamma_{d1} = \frac{(2 \cdot S_{11} - S_{21})(1 - S_{22} - S_{12}) + (1 - S_{11} - S_{21})(1 + S_{22} - 2 \cdot S_{12})}{(2 - S_{21})(1 - S_{22} - S_{12}) + (1 - S_{11} - S_{21})(1 + S_{22})}. \tag{2.73}$$

Using the differential-mode reflection coefficient, the differential-mode input impedance $Z_{d1}$ at the logical port (P1) is calculated as follows [72]:

$$Z_{d1} = Z_0 \cdot \frac{1 + \Gamma_{d1}}{1 - \Gamma_{d1}}, \tag{2.74}$$

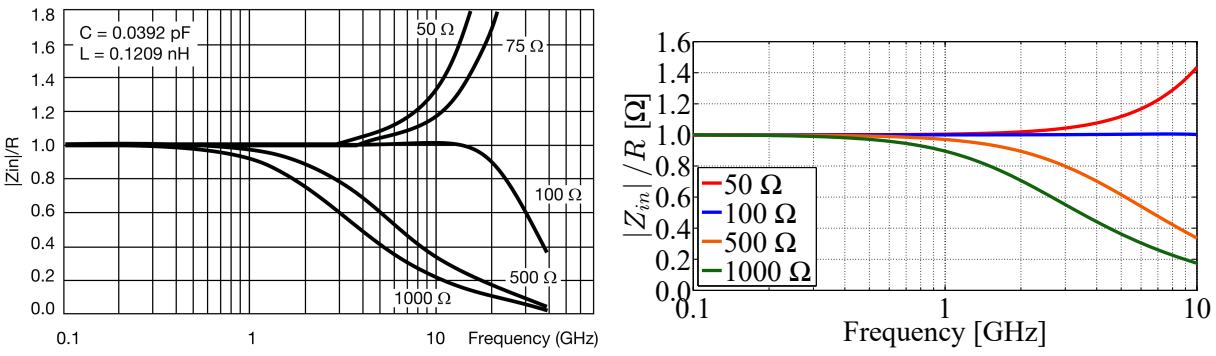
where $Z_0 = 50\ \Omega$ is the characteristic impedance.

## 2.2 Passive component modelling

Passive components are used in the probe circuit of the electro-optical voltage measurement system. Having an equivalent circuit model of the passive components used allows for simulations of the different circuits and structures explored in this thesis to be performed. The representation of passive components using circuit models, which have a physical interpretation, allows them to be used both for frequency domain and time domain simulations. In contrast to S-parameter measurement results, the circuit models can be used outside of the frequency range covered by the measurement results, which is limited by the VNA used to perform the measurements. The circuit models can be fitted for different physical parameters, like the thickness and dielectric constant of the substrate on which the components are mounted. Equivalent circuit models of the surface-mount resistors and capacitors used are presented. Components in the 0402 imperial surface-mount technology (SMT) package are used, because of the small size of the package, which allows the probe circuit design to be minimized while reducing the parasitics introduced by the components.

### 2.2.1 RF resistor modelling

Resistors used in broadband RF circuits need to have a stable frequency impedance profile. At high frequencies, the parasitics of the internal resistor structure, as well as the external parasitics related to soldering and the layout of the PCB on which the resistors are mounted, have a significant impact on the impedance of the resistors [73]. For resistors with a nominal resistance of 100 Ω or higher, the impedance drops at higher frequencies, as shown in Fig. 2.16a. The higher the nominal impedance, the more significant the drop in the effective impedance is. For the 500 Ω resistors, the impedance at 5 GHz drops to 60% of the nominal value, while it drops to 40% of the nominal value for the 1000 Ω resistors. This is primarily the effect of the




(a) Resistor datasheet specifications [73].

(b) Resistor circuit model simulations.

**Figure 2.16:** Comparison of the datasheet specifications and the equivalent circuit model (Fig. 2.17) simulations of the modelled RF resistors. The ratio of the magnitude of the effective impedance $Z_{in}$ and the nominal resistance $R$ of the resistors is shown.

parasitic capacitance which bypasses the internal resistance. For the 50 Ω resistors, the parasitic inductance has a dominant effect, which increases the effective impedance at frequencies above 3 GHz. The impedance of the 100 Ω resistors is very stable in the frequency range up to 8 GHz, which is critical for the probe circuit design.

The equivalent circuit model of the RF resistor, proposed by the manufacturer [73], is shown in Fig. 2.17. The nominal resistance $R$ of the resistor, the internal inductance $L$, and the internal shunt capacitance $C$, model the internal structure of the resistor. $L_c$ is the inductance of the external connection, while $C_g$ is the external capacitance towards the ground. The model parameters $L$, $C$ and $L_c$ are fitted by graphical tuning, according to the characteristics provided in the datasheet [73]. The resistance $R$ corresponds to the nominal resistance of each resistor. The external parasitic capacitance $C_g$ is dependent on the solder pad dimensions, the properties of the substrate and the layout of the PCB on which the resistor is mounted, as well as the soldering process used. For this reason, the capacitance towards the ground $C_g$ needs to be extracted based on the specific usage scenario. It is typically in the 0.05 pF to 0.30 pF range. The fitted parameters of the resistor equivalent circuit model are listed in Table 2.1.

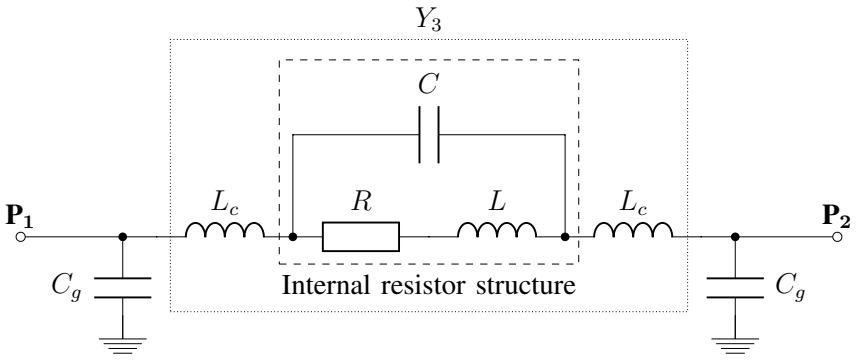



**Figure 2.17:** Equivalent circuit model of the RF resistor [73].

**Table 2.1:** Extracted RF resistor equivalent circuit model parameters.

| $L$ | $C$ | $L_c$ |
|---|---|---|
| 0.4308 nH | 0.0796 pF | 0.184 nH |

The proposed RF resistor equivalent circuit model is in the form of the admittance Π-model, shown in Fig. 2.13b. The external parasitic capacitances $C_g$ represent the port-to-ground elements $Y_1$ and $Y_2$ in the Π-model. The port-to-port element $Y_3$ of the Π-model is marked in Fig. 2.17. The values of the Π-model elements are calculated using (2.60)–(2.63), as described in Section 2.1.4. The capacitance $C_g$ is not included in the simulations of the fitted circuit model, which are shown in Fig. 2.16b. The effective impedance of the resistors is calculated

as $Z_{in} = 1/Y_3$. The simulated characteristics of the RF resistor circuit model in the frequency range of interest up to 8 GHz, show good fitting to the resistor datasheet specifications.

### 2.2.2 RF capacitor modelling

Capacitors are used in RF circuits as coupling or decoupling elements, for filtering, impedance matching, and a variety of other applications. It is useful to have an accurate lumped element model of a capacitor available when designing RF circuits, in order to estimate the parasitics and simulate the behaviour of the circuit [74]. The main advantage of the shunt characterization method, compared to the series method, is the precise characterization of small impedances [70, 75]. An additional benefit is that the feed line characteristics have a significantly smaller impact on the results, compared to the series measurement method.

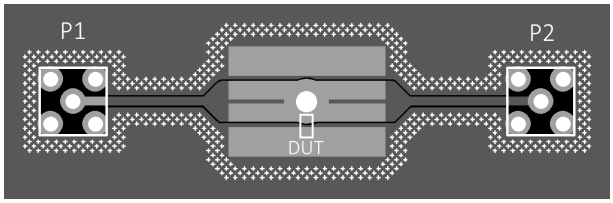
Application of the shunt technique for characterization of capacitors with low inductance values, and a corresponding capacitor equivalent circuit model are presented in [76]. A complex fourth-order equivalent circuit model of a high-capacitance multi-layer ceramic capacitor (MLCC) is presented in [77]. An MLCC characterization for frequencies up to 6 GHz is explored in [78]. However, these investigations have a limited focus on skin effect modelling and the explored capacitance values are relatively high. The lumped element models of a surface-mount resistor and power inductor, which include the skin effect modelling, are presented in [79] and [75], respectively.

An equivalent circuit model of a multi-layer ceramic capacitor is extracted. An MLCC in a surface-mount 0402 imperial package is characterized using the two-port shunt method, described in Section 2.1.4. The nominal capacitance is 100 pF with a tolerance of 5% [80]. The high quality factor (Q-factor) and a low equivalent series resistance (ESR) make these capacitors suitable for RF applications. Three samples of the capacitor are measured, in order to control the repeatability of the capacitor characteristics. The presented lumped element model is more focused on skin effect modelling than comparable models [76, 77]. A capacitor with a lower nominal capacitance and a higher self resonant frequency (SRF) than in [76, 77] is characterized. All the elements in the model are frequency independent, and there is a clear physical interpretation of each element in the model.

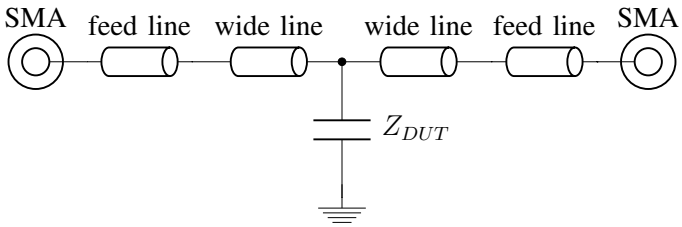
#### Characterization setup

The capacitor characterization structure consists of two feed lines realized using conductor-backed coplanar waveguide (CBCPW) transmission lines [81]. Each feed line consists of a 50-Ohm transmission line segment, and a wider line, which forms the solder space for the device under test. This layout allows for testing of components with different package sizes. The DUT is connected as a shunt capacitor. One port of the DUT is connected to the feed lines, while

the other port is connected to the ground. SubMiniature version A (SMA) connectors are used at the input of each feed line, forming two ports. Two-port S-parameters of the DUT are measured using a vector network analyzer [68]. The layout and model of the capacitor characterization structure are shown in Fig. 2.18. When there is no DUT soldered to the board, the characterization structure is used as a Thru calibration structure, with a direct connection between the two ports. Three calibration structures are measured in order to control the repeatability of the structures and the measurement results.




(a) Layout.




(b) Model.

**Figure 2.18:** Layout and model of the capacitor characterization and calibration structure.

The SMA connector and feed line at each port of the structure form a test fixture, which needs to be de-embedded. The calibration structures are used to extract the parameters of the SMA connector circuit model, as well as to extract the feed line model, shown in Fig. 2.18b. The capacitor characterization structure model parameters are listed in Table 2.2. The parameters $l_{feed}$ and $w_{feed}$ are the length and width of the 50-Ohm feed line segment, $l_{wide}$ and $w_{wide}$ are the length and width of the wider feed line segment, $g$ is the CBCPW transmission line gap, $h$ is the FR4 substrate thickness, $\varepsilon_r$ is the dielectric constant, $\tan\delta$ is the dielectric loss tangent, $\sigma$ is the conductor conductivity, and $t$ is the conductor thickness.

**Table 2.2:** Extracted capacitor characterization structure model parameters.

| $l_{feed}$ | $w_{feed}$ | $l_{wide}$ | $w_{wide}$ | $g$ |
|---|---|---|---|---|
| 11.85 mm | 1.016 mm | 10.835 mm | 4.65 mm | 0.18 mm |
| $h$ | $\varepsilon_r$ | $\tan\delta$ | $\sigma$ | $t$ |
| 1.6 mm | 4.2 | 0.02 | $4.1 \cdot 10^7$ S/m | 35 µm |

The SMA connector circuit model used here is described in [82]. The connector circuit model parameters are optimized and fitted to the calibration structure measurement results. The circuit model is shown in Fig. 2.19, and the optimized model parameters are listed in Table 2.3.

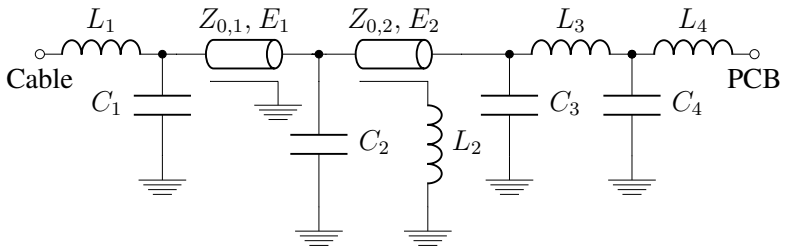
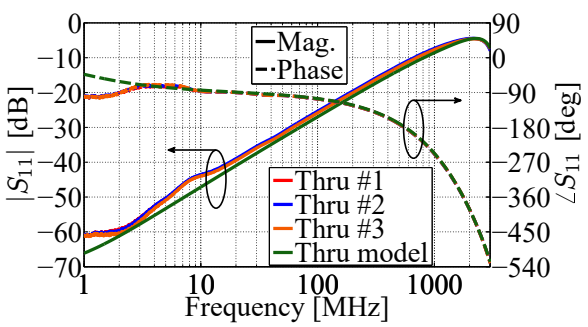



**Figure 2.19:** SMA connector circuit model [82].

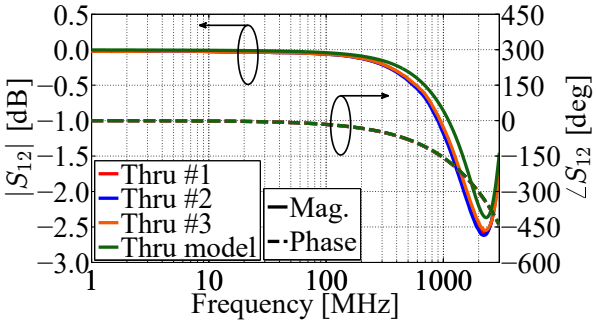
**Table 2.3:** Optimized SMA connector model parameters.

| $L_1$ | $C_1$ | $Z_{0,1}$ | $E_1$ | $C_2$ | $Z_{0,2}$ |
|---|---|---|---|---|---|
| 0.036 nH | 0.8 fF | 47 Ω | 178 deg | 84 fF | 60 Ω |
| $E_2$ | $L_2$ | $C_3$ | $L_3$ | $C_4$ | $L_4$ |
| 58 deg | 0.13 nH | 80 fF | 1 nH | 160 fF | 0.016 nH |

The comparison of the Thru calibration structure model to the measurement results is shown in Fig. 2.20. There is a good repeatability between the measurements, and the calibration structure model is well fitted to the measurement results. Based on these results, the presented test fixture model can be used for de-embedding of the capacitor measurements.




(a) $S_{11}$-parameter magnitude and phase.




(b) $S_{12}$-parameter magnitude and phase.

**Figure 2.20:** Comparison of the Thru calibration structure model to the measurement results.

### Capacitor measurement results

Two-port S-parameter measurements of the three capacitor samples are performed. Four different methods are used to extract the impedance of the device under test:

1. $Z_{DUT} = 25 \cdot S_{12}$ (embedded): method of extracting the DUT impedance based on the S-parameter measurements, before de-embedding is performed [70].
2. $Z_{DUT} = 25 \cdot S_{12}$ (de-embedded): method of extracting the DUT impedance based on the S-parameter measurements, after de-embedding is performed.
3. $Z_{DUT} = Z_{12}$ (embedded): method of extracting the DUT impedance based on the Z-parameters, which are calculated from the measured S-parameters as described in Section 2.1.4, before de-embedding is performed [23].
4. $Z_{DUT} = Z_{12}$ (de-embedded): method of extracting the DUT impedance based on the Z-parameters, after de-embedding is performed.

The comparison of these four methods, based on the capacitor #1 measurement results, is shown in Fig. 2.21. As it can be seen from the figure, methods 1) and 2) are limited to a maximum impedance of 25 Ω, and become inaccurate for frequencies that are approximately 10 times higher or lower than the SRF of the capacitor (490 MHz). This is a result of the DUT impedance exceeding the impedance of the two 50-Ohm ports, connected in parallel to the DUT. Additionally, it is necessary to de-embed the impact of the test fixtures on the measurement results. When de-embedding is not performed, transmission line effects become significant at frequencies above 500 MHz. Based on this discussion, it can be concluded that method 4) is the most accurate. This method is used for all the results presented in the rest of this paper.

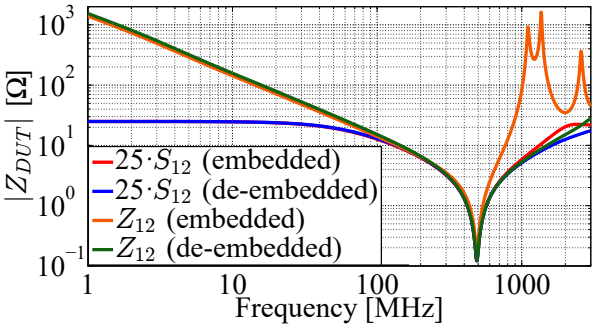
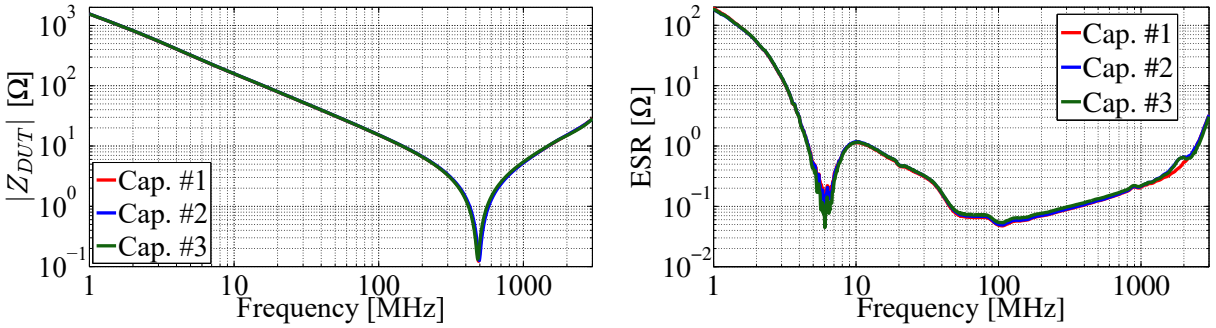



**Figure 2.21:** Capacitor #1 impedance magnitude. Comparison of the four methods used to extract the impedance of the device under test.

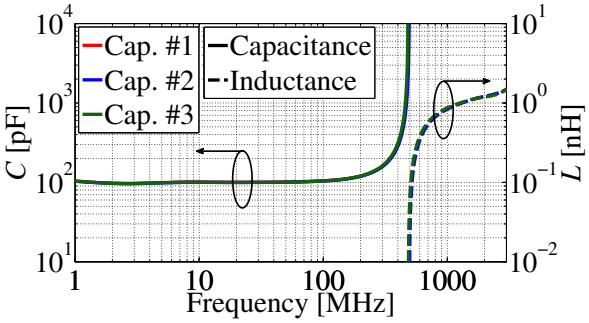
Comparison of the impedance magnitude of the three measured capacitors is shown in Fig. 2.22a. There is a good match between the three measured samples, despite the nominal tolerance of the components. Comparison of the equivalent series resistance of the three measured capacitors is shown in Fig. 2.22b. The ESR is calculated as ESR $= \mathrm{Re}\{Z_{DUT}\}$. The ESR is frequency dependent and it increases with frequency above the SRF, following the general trend described in [83]. The drop-off in the measured ESR value around 6 MHz is likely




(a) Impedance magnitude.




(b) Equivalent series resistance (ESR).




(c) Apparent capacitance ($C$) and apparent inductance ($L$).

**Figure 2.22:** Comparison of the impedance characteristics extracted from the three measured capacitor samples.

a result of the VNA calibration uncertainty at low frequencies. Comparison of the apparent capacitance ($C$) and the apparent inductance ($L$) of the three measured capacitors is shown in Fig. 2.22c. The apparent capacitance is calculated as $C = -1/(Z_{DUT} \cdot 2\pi f)$. The apparent capacitance is frequency independent for frequencies that are more than 5 times lower than the SRF of the capacitor. At these lower frequencies, the apparent capacitance can be considered to represent the capacitance of the device under test. The apparent inductance is calculated as $L = Z_{DUT}/(2\pi f)$. The equivalent series inductance (ESL) can be considered equivalent to the apparent inductance at higher frequencies, where the apparent inductance value becomes constant.

### Capacitor model

The de-embedded two-port S-parameter measurement results of the capacitors are converted to Z-parameters. The impedance of the DUT is calculated from the Z-parameters as $Z_{DUT} = Z_{12}$. The capacitor shunt circuit model is fitted to the measurements. The lumped element model parameters are extracted and optimized for the capacitor #1. The proposed capacitor equivalent circuit model is shown in Fig. 2.23, and the optimized model parameters are listed in Table 2.4. The capacitance $C_{nom}$ represents the nominal capacitance of the modelled capacitor. The inductance $L_{mount}$ is the mounting inductance, related to the equivalent series inductance and the return path inductance. The resistance $R_{LFloss}$ is the low frequency loss resistance. The other

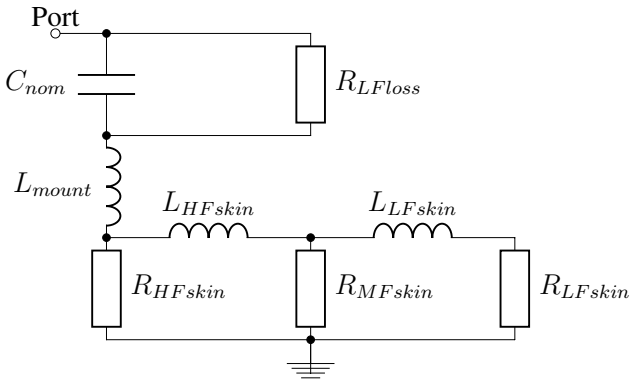


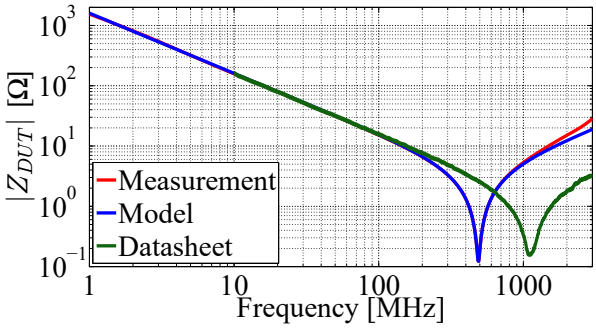

**Figure 2.23:** Proposed capacitor equivalent circuit model.

**Table 2.4:** Optimized capacitor equivalent circuit model parameters.

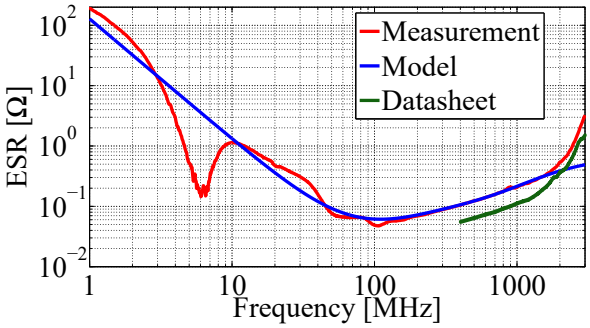
| $C_{nom}$ | $L_{mount}$ | $L_{HFskin}$ | $L_{LFskin}$ |
|---|---|---|---|
| 99.16 pF | 1018 pH | 63.51 pH | 103.5 pH |
| $R_{HFskin}$ | $R_{MFskin}$ | $R_{LFskin}$ | $R_{LFloss}$ |
| 0.6388 Ω | 0.0946 Ω | 0.0710 Ω | $2 \cdot 10^4$ Ω |

resistances and inductances are related to skin effect modelling. $L_{HFskin}$ and $L_{LFskin}$ are the skin effect inductances at high and low frequencies. $R_{HFskin}$, $R_{MFskin}$ and $R_{LFskin}$ are the skin effect resistances at high, medium and low frequencies, respectively.

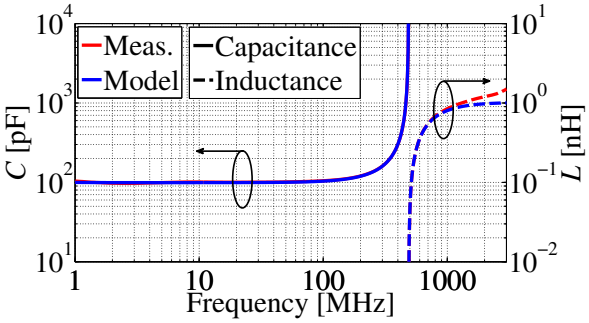
The capacitor equivalent circuit model is compared to the measurement results and the impedance characteristics specified in the datasheet [80], as shown in Fig. 2.24. The fitting between the capacitor equivalent circuit model and the measurement results is very good in the frequency range from 10 MHz up to 2 GHz. The downside of using the shunt method to characterize the capacitor, is the fact that the parasitics of the solder pad connected to the ground are not included in the model. Compared to the datasheet, the measurements and circuit model take into account the behaviour of a capacitor soldered to a printed circuit board, including the additional parasitics. It is possible to extend the range of the model, and fit the ESR value at higher frequencies, by adding additional LR elements for skin effect modelling. It is demonstrated that the proposed capacitor equivalent circuit model is very good in the frequency range from 10 MHz up to 2 GHz, and that there is good repeatability for all the three measured capacitor samples and calibration structures [16].




(a) Impedance magnitude.




(b) Equivalent series resistance (ESR).




(c) Apparent capacitance ($C$) and apparent inductance ($L$).

**Figure 2.24:** Comparison of the impedance characteristics extracted from the capacitor equivalent circuit model, the measurement results and the datasheet [80].

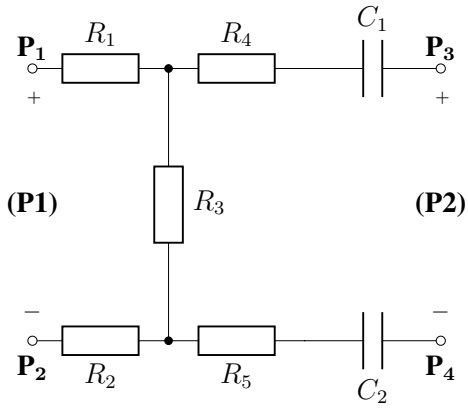
## 2.3 Attenuator circuit

The attenuator circuit is the input stage of the electro-optical probe circuit. The attenuator circuit is used to lower the level of the measured input RF signal in order not to overdrive the laser diode. The attenuator circuit consists of a resistor network. By selecting the values of the resistors in the attenuator circuit, the attenuation ratio is set. Good symmetry of the attenuator circuit is required in order to achieve a high CMRR of the probe circuit. The goal is to attenuate the input differential-mode signal, while minimizing the mode conversion of the unwanted common-mode signal to a differential signal. A stable frequency profile of the differential-mode and common-mode signal attenuation is desired. The attenuator circuit needs to have a high input impedance in order not to impact the performance of the device under test. The input impedance of the attenuator circuit determines the input impedance of the probe circuit. Although ESD waveforms have high voltages, their average power is almost negligible, meaning that the power dissipation on the resistors in the attenuator circuit is not an issue. This allows for compact surface-mount technology resistors to be used [2]. Different attenuator circuit topologies are designed, characterized and compared.

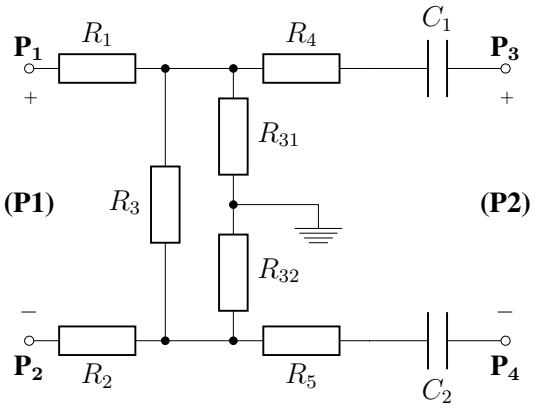
### 2.3.1 Initial attenuator circuit design

The schematic of the initial attenuator circuit design (attenuator #1) is presented in Fig. 2.25a. The attenuator circuit is realized as a resistor network with two voltage dividers and a current divider. The input resistors $R_1$ and $R_2$ take over most of the input voltage, and act as a voltage divider for the next stage. The power dissipation on these two resistors limits the maximum input differential root-mean-square (RMS) voltage for the probe circuit. The parallel branch with the resistor $R_3$ is used to balance between the two input branches, in order to limit the asymmetry introduced by the resistance tolerances and the parasitics related to soldering of the surface-mount components. Resistor $R_3$ also attenuates the input signal by acting as a current divider, and limiting the current going into the output stage of the attenuator circuit, and the laser. Resistors $R_4$ and $R_5$ further attenuate the input signal by dividing the voltage in the output stage between the two resistors and the dynamic resistance of the laser connected in series with the resistors.

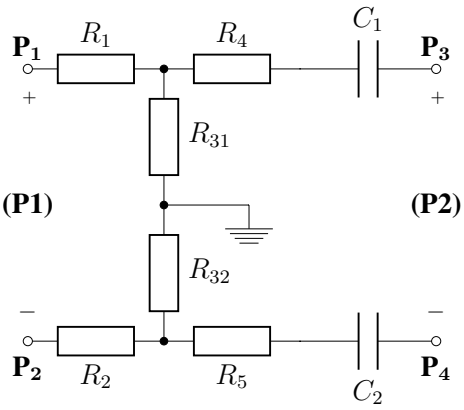
Surface-mount technology resistors in a 0402 imperial package are used. These small components limit the parasitics introduced into the circuit and allow for minimization of the attenuator circuit design. The list of components used in the attenuator circuit and the nominal performance parameters are listed in Table 2.5. The voltage attenuation is the ratio of the input voltage and the output voltage when the attenuator circuit is terminated with a matched 100 Ω differential load. On the other hand, the definition of the differential-to-differential transmission coefficient $S_{dd21}$ takes into account the impedance matching between the generator and the attenuator circuit and uses different port terminations.




(a) Attenuator #1 circuit design.




(b) Attenuator #2 circuit design.




(c) Attenuator #3 circuit design.

**Figure 2.25:** Comparison of the attenuator circuit design schematics.

**Table 2.5:** Attenuator circuit design configurations.

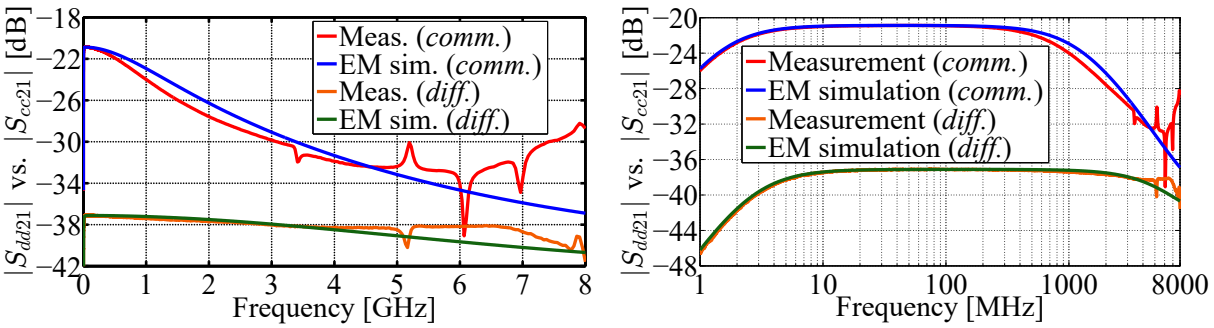
| Design | $R_1, R_2, R_4, R_5$ | $R_3$ | $R_{31}, R_{32}$ | $C_1, C_2$ | Attenuation | $S_{dd21}$ |
|---|---|---|---|---|---|---|
| Attenuator #1 | 500 Ω | 100 Ω | – | 100 pF | 131 (42.3 dB) | –37 dB |
| Attenuator #2 | 500 Ω | 200 Ω | 100 Ω | 100 pF | 131 (42.3 dB) | –37 dB |
| Attenuator #3 | 500 Ω | – | 50 Ω | 100 pF | 131 (42.3 dB) | –37 dB |

### Verification of EM simulation results

A characterization structure is designed in order to characterize the attenuator #1 circuit layout. The attenuator circuit characterization structure is realized on the PCB stack-up shown in Fig. 1.3. The attenuator circuit SMT components are located on the Top layer of the PCB, on the top side of the Rogers substrate, while the Inner layer of the PCB, on the bottom side of the Rogers substrate is used as the ground plane. An additional ground plane is placed on the Bottom layer of the PCB, on the bottom side of the FR4 substrate. Four-port S-parameters of the structure are measured using a dual-source four-port VNA [67]. The measurements are per-

formed in the frequency range from 1 MHz to 8 GHz. Mixed-mode S-parameters are calculated from the standard single-ended S-parameters using (2.31)–(2.46), and are used to characterize the performance of the attenuator circuit. In addition to measurements, electromagnetic (EM) simulations of the attenuator structure are performed using a commercially available EM solver based on the finite element method (FEM) [84], in order to analyze the performance of the structure. The measurements and the EM simulation results are compared in Fig. 2.26, in order to verify the validity of the EM simulations.

There is good matching between the measurement and EM simulation results for both the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$, in the frequency range from 1 MHz to 5 GHz, which is critical for the performance of the probe circuit. The mode conversion parameters like $S_{dc21}$ are not compared, given that it is not possible to simulate the high level of the mode conversion parameters which are obtained through measurements. The high mode conversion is caused by asymmetrical ground parasitics that are introduced through placing and soldering of the components on the characterization PCB, which are not taken into account in the EM simulations. It can be concluded that the EM simulations provide reliable results, and they can be used to verify the modifications and improvements that are made to the attenuator circuit design.




(a) Linear frequency scale.

(b) Logarithmic frequency scale.

**Figure 2.26:** Comparison of the measurement and the EM simulation of the attenuator #1 circuit design. The magnitude of the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ are compared.

The differential-to-differential transmission coefficient $S_{dd21}$ level of the attenuator #1 design at low frequencies between 10 MHz and 1 GHz matches the nominal value of –37 dB. The differential-mode signal attenuation is relatively stable in the entire measurement range and remains within ±3 dB even above 5 GHz. On the other hand, the level of the common-to-common transmission coefficient $S_{cc21}$ at low frequencies is approximately 16 dB higher than for the differential-to-differential transmission coefficient. At higher frequencies it drops by approximately 16 dB, but remains at least 4 dB higher than the differential-to-differential transmission level in the entire frequency range. While the frequency profile of the differential-to-differential transmission coefficient is very stable, the common-to-common transmission coefficient is

significantly higher than desired, and needs to be more stable in terms of frequency.

### 2.3.2 Attenuator circuit design optimization

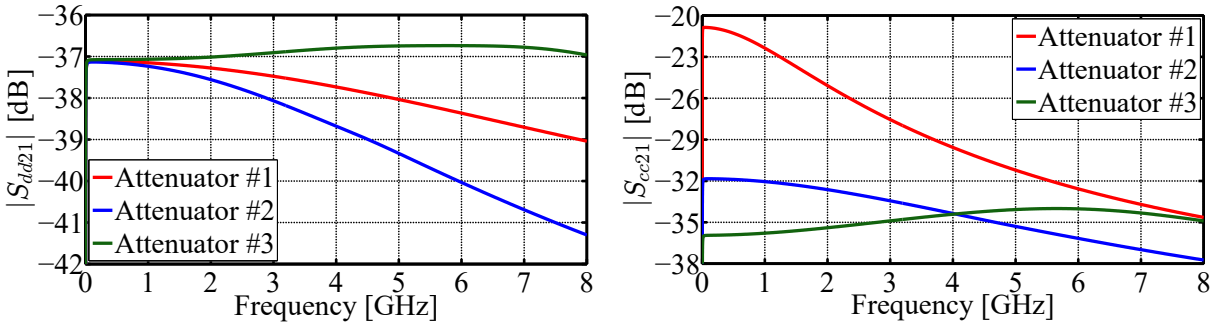
The attenuator circuit design is modified in order to improve the suppression of the common-mode signal. This is achieved by adding a parallel resistor branch with the center of the branch connected to the ground. The ground connection is used to balance the signal level in both branches and reduce the impact of the asymmetry introduced in the input stage of the attenuator circuit, where the voltage drop is the highest. Two new attenuator circuit designs are introduced: attenuator #2 (Fig. 2.25b) and attenuator #3 (Fig. 2.25c). Attenuator #2 uses an additional parallel branch with the ground connection realized using the resistors $R_{31}$ and $R_{32}$ added in parallel to the existing parallel branch with the resistor $R_3$. This combines the benefits of both a differential parallel branch, and a parallel branch with a ground reference. Attenuator #3 replaces the existing differential parallel branch $R_3$ with a parallel branch with a ground reference realized using the resistors $R_{31}$ and $R_{32}$. Such a solution minimizes the size of the attenuator circuit and utilizes the full benefits of the parallel branch with a ground reference. The list of components used in the attenuator circuits and the nominal performance parameters are listed in Table 2.5.

#### Attenuator circuit EM simulations

EM simulations of all three attenuator circuit designs presented in Fig. 2.25 are performed. The EM simulation results are compared in Fig. 2.27. When analyzing the behaviour of the attenuator structures, the low frequency drop in both the differential-mode an common-mode signal as a result of the high impedance of the series blocking capacitors $C_1$ and $C_2$ is not taken into account. The nominal value of the differential-to-differential transmission coefficient $S_{dd21}$ for all three attenuator circuit designs is the same. The attenuator #3 differential-to-differential transmission coefficient is the most stable in terms of frequency and remains within $\pm$0.3 dB of the nominal value in the entire frequency range. Compared to the attenuator #3, the differential-to-differential transmission coefficient value drops more for the initial attenuator #1 circuit design, by 1.9 dB at 8 GHz, and the most for the attenuator #2, by 4.2 dB at 8 GHz.

The common-to-common transmission coefficient $S_{cc21}$ of the attenuator #1 circuit design drops approximately from –21 dB at low frequencies to –35 dB at 8 GHz. The common-to-common transmission coefficient of the attenuator #2 circuit design drops approximately from a nominal value of –32 dB to –38 dB at 8 GHz. The common-to-common transmission coefficient of the attenuator #3 circuit design remains within $\pm$2 dB of the nominal value of –36 dB in the entire frequency range. Based on the EM simulations of the three attenuator circuit designs, it is observed that the attenuator #3 circuit design has the best performance for both the

differential-to-differential and the common-to-common transmission coefficient, with both the lowest nominal value and the most stable frequency profile.




(a) Differential-to-differential signal transmission.

(b) Common-to-common signal transmission.

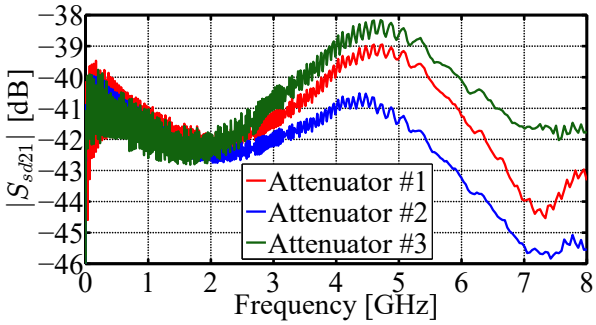
**Figure 2.27:** Comparison of the EM simulations of the three characterized attenuator circuit designs. The magnitude of the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ are compared.

### Probe circuit measurements

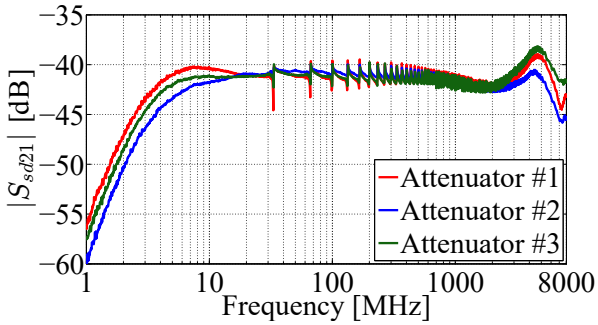
The results of the comparison of the EM simulations of the three attenuator circuit designs are verified by performing measurements. In order to perform an accurate evaluation of the behaviour of the different attenuator circuit designs, each attenuator circuit is implemented as a part of a probe circuit, as shown in Fig. 4.1. A laser biased using the isolated power supply PoF bias module (Fig. 3.3a) is connected to the output of the attenuator circuit. The laser represents a matched differential load. The laser has a limited common-mode rejection ratio and converts some of the unwanted common-mode signal to differential-mode, which is transmitted to the photodetector. The probe circuit has two physical input ports $P_1$ and $P_2$, which form the logical balanced mixed-mode port (P1). The photodetector output port $P_3$ presents the output port of the probe circuit, which forms the logical single-ended port (P2) for the mixed-mode analysis. S-parameters of the three probe circuits, each with a different attenuator circuit design and the same laser layout are measured using a two-port VNA [68]. The measured three-port standard S-parameters are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58).

The differential-mode and common-mode signal transmission, as well as the CMRR of the probe circuits with the different attenuator designs are compared in Fig. 2.28. The differential-mode transmission coefficient $S_{sd21}$ measurements show a similar trend for all three attenuator circuit designs. The difference between the attenuators increases slightly with frequency, but all results remain within a few dB even at 8 GHz. The low frequency cutoff in the differential-mode signal transmission coefficient $S_{sd21}$ is a result of the lower cutoff frequency of 2 MHz of the photodetector model used to perform the measurements [69]. It is not taken

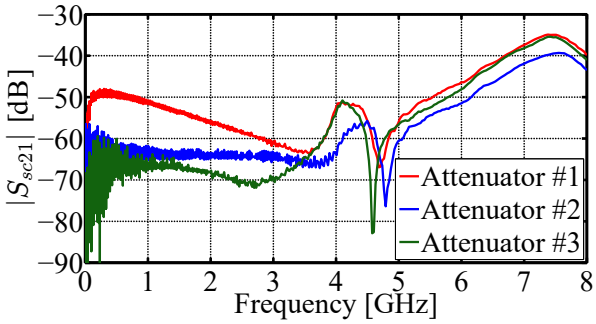
into account when comparing the attenuator circuit designs, given that all three designs display similar behaviour with very small differences in the lower cutoff frequency. The attenuator #3 circuit design has the most stable differential-mode frequency characteristic, which remains within $\pm 3$ dB of the nominal value within the entire measurement frequency range. The common-mode transmission coefficient $S_{sc21}$ is the lowest for the attenuator #3 up to 3.4 GHz. The attenuator #2 has a 2–8 dB higher common-mode signal level in this frequency range, with the attenuator #1 being the worst. The attenuator #1 common-mode characteristic starts with a signal level which is approximately 20 dB higher than for the attenuator #3, and decreases gradually with frequency. After the bump at 4.1 GHz and the resonance around 4.6 GHz, the general trend is very similar for all three attenuator characteristics, although the common-mode signal level is slightly lower for the attenuator #2.



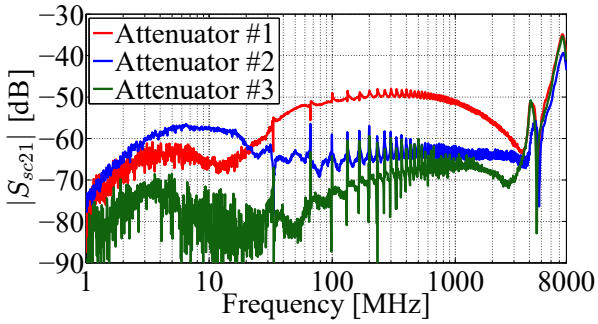

(a) Differential-mode signal (linear frequency).



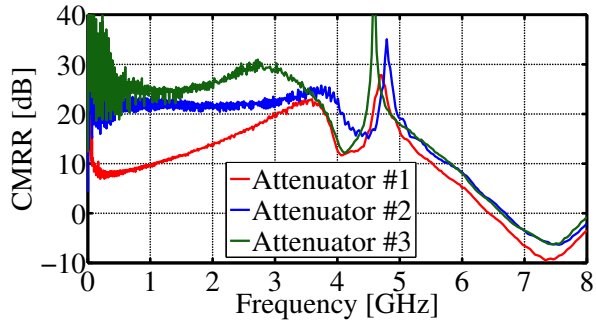

(b) Differential-mode signal (log. frequency).



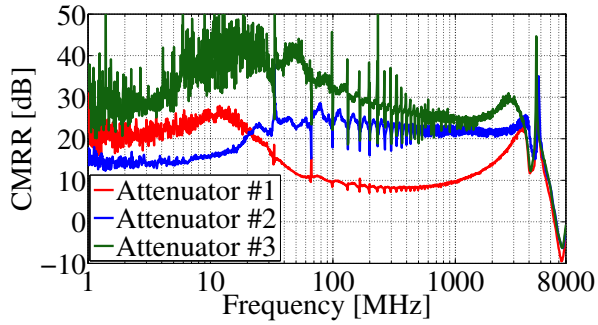

(c) Common-mode signal (linear frequency).




(d) Common-mode signal (logarithmic frequency).




(e) Common-mode rejection ratio (lin. frequency).



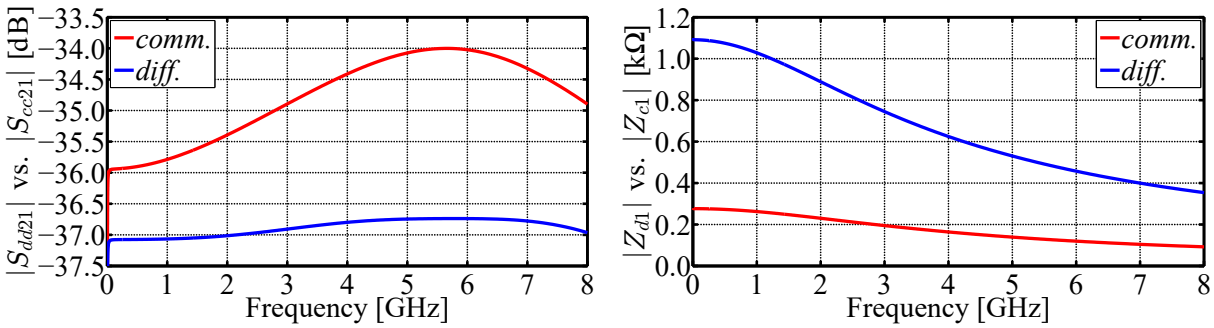

(f) Common-mode rejection ratio (log. frequency).

**Figure 2.28:** Comparison of the measurements of the three probe circuits with the different attenuator circuit designs. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

Given the very similar differential-mode characteristics and the differences in the common-mode characteristics, the CMRR is the highest for the attenuator #3 in the frequency range up to 3.5 GHz. The CMRR of the attenuator #2 is 3–9 dB lower in this frequency range. The attenuator #1 circuit design has the worst CMRR, which is mostly below 20 dB, because of the high value of the common-mode signal for frequencies up to 3.6 GHz. At frequencies above 5 GHz, all three attenuator circuits follow the same trend, with a fast decrease in the CMRR along a stable slope, regardless of the differences between the circuit designs. The CMRR level is almost the same for the attenuator #2 and attenuator #3. The measurement comparison of the probe circuits with the three different attenuator circuit designs confirms the results of the attenuator EM simulations. It is demonstrated that the attenuator #3 circuit design has the best overall performance and it should be used as a part of the probe circuit design. By optimizing the attenuator circuit design, the CMRR is increased in the frequency range up to 3.5 GHz, with the increase being mostly between 10 dB and 20 dB.

### Optimized attenuator circuit design

EM simulation results of the attenuator #3 circuit design are shown in Fig. 2.29. The differential-to-differential transmission coefficient $S_{dd21}$ is very stable and remains within $\pm 0.3$ dB of the nominal value in the entire frequency range. The common-to-common transmission coefficient $S_{cc21}$ has an approximately 1 dB higher nominal value and is slightly less stable. The common-mode signal remains within $\pm 2$ dB of the nominal value in the entire frequency range. The differential-mode and common-mode signal attenuation have comparable levels and both are stable in terms of frequency, providing good attenuation of the input signal. The nominal differential-mode input impedance $Z_{d1}$ is 1092 Ω, while the nominal common-mode input impedance $Z_{c1}$ is 275 Ω. Both impedances follow a similar frequency profile, dropping to ap-




(a) Differential-to-differential and common-to-common signal transmission.

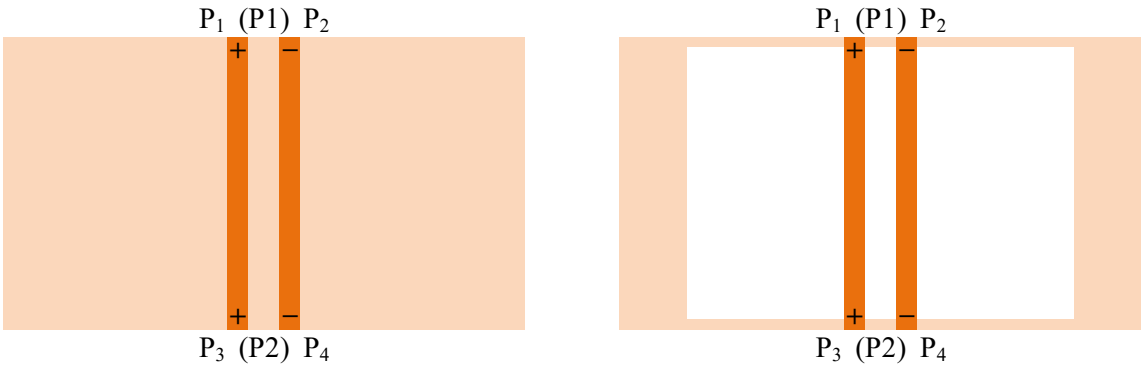
(b) Differential-mode and common-mode input impedance.

**Figure 2.29:** EM simulations of the attenuator #3 circuit design. Comparison of the magnitude of the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ (left). Comparison of the magnitude of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ (right).

proximately 1/3 of the nominal value at 8 GHz. This is a result of the parasitics between the attenuator circuit components and the PCB, as well as transmission line effects in the attenuator structure, which come into play at higher frequencies.

### Impact of the ground plane

Further modifications of the attenuator structure layout can be made in order to decrease the impact of the parasitic effects at high frequencies. One method is to reduce the parasitics by creating a slot in the ground plane under the attenuator. This modification is examined by analyzing the behaviour of two differential 50-Ohm transmission lines realized on the RF substrate, which corresponds to the Rogers substrate layer of the probe PCB stack-up shown in Fig. 1.3. Two EM simulations of the differential transmission line structure are performed, one for a layout with a solid ground plane and the other for a layout with a slot in the ground plane, shown in Fig. 2.30. The EM simulation results are shown in Fig. 2.31. The slot in the ground plane increases the attenuation of the common-mode signal more than the differential-mode signal, given the different EM propagation modes. The downside is that both the differential-mode




(a) GND. (b) No GND.

**Figure 2.30:** Layout of a differential pair of transmission lines with a solid ground plane (GND) and with a slot in the ground plane (No GND).

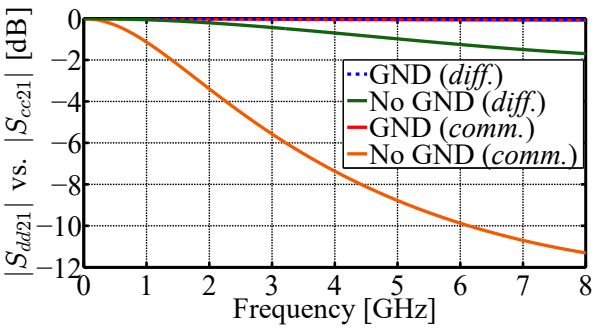



**Figure 2.31:** Comparison of the EM simulation results of a differential pair of transmission lines with a solid ground plane (GND) and with a slot in the ground plane (No GND). The magnitude of the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ are compared.

transmission coefficient $S_{dd21}$ and the common-mode transmission coefficient $S_{cc21}$ are less stable over the wide frequency range.

The main practical downside of this modification is that creating a slot in the ground plane makes the entire measurement system more susceptible to EM interference, which can be coupled to the transmission lines and components. A compromise can be achieved by removing the Inner layer ground plane in the PCB stack-up shown in Fig. 1.3, which is on the bottom side of the Rogers substrate, while keeping the ground plane on the bottom side of the FR4 substrate, which is on Bottom layer of the probe PCB. The attenuator circuit can also be modified by adding additional blocking capacitors at the input of the circuit, in order to achieve DC signal decoupling, and to increase the input impedance at low frequencies.

## 2.4 Summary

Methods for characterizing multiport devices at high frequencies by measuring scattering parameters are presented. Mixed-mode S-parameters are better suited to characterize differential (balanced) circuits than traditional single-ended S-parameters. Traditional vector network analyzers are designed for measuring single-ended S-parameters. The pure-mode vector network analyzer is a concept for measuring mixed-mode S-parameters directly. Although no such devices are commercially available, dual-source vector network analyzers can be used instead. Different measurement methods are compared by characterizing the typical circuits explored in this thesis. By comparing the measurements performed using a traditional four-port VNA, a dual-source four-port VNA and a traditional two-port VNA, good repeatability of the differential-mode and common-mode characteristics is demonstrated. Most measurements discussed in this thesis are performed using a two-port VNA.

The series and shunt characterization methods are presented. The main benefit of using the series characterization method is for extracting the port-to-ground parasitics, while the shunt method is best suited for characterizing low impedance devices under test. Equivalent circuit models of the surface-mount resistors and capacitors used in the attenuator circuit design are extracted. It is shown that resistors with a higher nominal resistance have a higher drop in impedance at frequencies in the gigahertz range, as a result of parasitics. A multi-layer ceramic capacitor suitable for RF applications is modelled using the two-port shunt method. The extracted model accurately describes the impact of skin effect at frequencies up to 2 GHz.

The attenuator circuit is used to lower the input RF signal level. The resistors used in the attenuator circuit set the attenuation ratio of the electro-optical probe circuit. The output voltage of the attenuator is limited by the maximum signal level allowed for the laser diode to keep operating in the linear region. Electromagnetic simulations and S-parameter measurements of multiple iterations of the attenuator circuit design are performed. The stability of the differential-mode and common-mode signal attenuation is improved, and the mode conversion is reduced. The attenuator designs are evaluated by measuring probe circuits with the different attenuator circuit designs implemented. By optimizing the attenuator circuit design, the CMRR is increased by around 10 dB to 20 dB.

# Chapter 3

# Laser diode characterization

## 3.1 Introduction to laser diode characterization

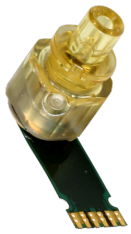
The laser is the central component of the electro-optical probe circuit. The laser diode is used to convert the measured RF signal into an optical signal, which is transmitted using an optical fiber to a photodetector. By converting the measured RF signal into an optical signal, galvanic isolation of the measurement system is achieved. In this way, good immunity of the measurement system to electromagnetic interference is achieved, making it suitable for operation in an electromagnetically polluted environment [2, 85, 86]. A vertical-cavity surface-emitting laser (VCSEL) is used because of its compact size, fast speed, light weight, high conversion efficiency and low cost [86].

The input RF signal is applied differentially to the laser diode, between the anode and the cathode, where neither of the electrodes is connected to the ground. This improves the immunity of the system to electromagnetic noise [2]. Due to asymmetries in the internal structure of the VCSEL and package-related parasitics, there is some mode conversion in the laser diode [87]. This means that along with the wanted differential-mode signal some of the unwanted common-mode signal that is applied to the laser diode is also transmitted. The laser is the main component which limits the CMRR of the probe circuit. The laser is directly modulated and the light intensity modulation presents the measured voltage waveform. The optical signal is transmitted using an optical fiber to the photodetector which is located in the processing stage of the measurement system. The photodetector converts the optical signal back into an RF signal which can then be processed and analyzed. The lower cutoff frequency, signal-to-noise ratio and sensitivity of the electro-optical measurement system depend primarily on the lower frequency cutoff and the noise floor of the photodetector model used [69].

Based on the voltage-current-power characteristics of the VCSEL, the operating point is chosen in the center of the linear region, in order for the laser to be able to work with maximum signal amplitudes, as described in [88]. The operating point of the laser is set using a bias circuit. The bias circuit is realized in a differential configuration, based on the design described in [87, 89]. Good symmetry of the bias circuit design is important in order not to introduce additional mode conversion on the differentially driven laser. The good characteristics of the bias circuit ensure that the input RF signal is routed into the laser diode, and is blocked from going into the bias circuit. Multiple bias circuit topologies are designed and evaluated. An isolated power-over-fiber (PoF) power supply is used to bias the laser diode, as well as a non-isolated power supply, which is directly connected to a voltage source. The isolated and non-isolated power supply bias modules are characterized. The impact of power supply isolation on the characteristics of the laser diode is examined in terms of noise in the differential-mode and the common-mode signal transmission.

EMC standards for measurements of electromagnetic emissions of integrated circuits re-

quire a bandwidth up to 1 GHz [13]. System-level ESD pulses contain information in the frequency band up to 5 GHz [2]. VCSEL models with a specified data rate of 10 Gbit/s are used. This is enough given the required bandwidth for characterization of ESD and EMC voltage waveforms. The VCSELs are integrated into a transmitter optical subassembly (TOSA) package aligned to a housing fitted for the LC optical connector [90]. Two package types are used. One is a TOSA package with a small flexible PCB, shown in Fig. 3.1a. The VCSEL is mounted as a 6-pad surface-mount device. The other package type is a 5-lead through-hole TOSA package, shown in Fig. 3.1b. The TOSA casing is the same for both laser types, while the fixtures are different. The VCSEL is realized as a 5-pin device. The main two pins are the laser anode and cathode. Anode and cathode pins for the monitor photodiode are also provided, and can be used for optional monitoring of the light intensity level. The remaining pin is the laser case (ground) pin. In the through-hole TOSA package, the laser pins are connected directly to the leads of the through-hole package.



(a) TOSA package with the flexible PCB.

(b) Through-hole TOSA package.

**Figure 3.1:** VCSEL TOSA package with the flexible PCB and the through-hole TOSA package [90].

The TOSA package with the flexible PCB uses a small PCB with CBCPW transmission lines, which provides a transition between the pins of the VCSEL casing and the surface-mount pads. The solder pads include the laser anode and cathode pads, as well as the monitor diode anode and cathode, while the laser case (ground) pin is realized as two separate pads, one next to the laser anode pad and the other next to the laser cathode pad. The flexible PCB allows for simple mounting and soldering of the VCSEL. However, the flexible PCB creates a longer signal path, which introduces additional parasitics into the signal transmission path. The CBCPW transmission lines on the flexible PCB provide good matching for the 100 Ω differential input impedance of the VCSEL. The downside is the mechanical sensitivity of the flexible PCB, as well as the sensitivity of the RF characteristics of the flexible PCB to mechanical manipulation, such as bending and twisting. The through-hole package provides a significantly more robust connection between the VCSEL and the characterization structure PCB.

The RF performance of different VCSEL models is analyzed and compared. Based on the mixed-mode S-parameter analysis, the differential-mode and common-mode characteristics of the laser diodes are compared. An equivalent circuit model of the VCSEL is extracted. Based on the characterization and modelling results, the VCSEL layout is optimized in order to

improve the CMRR characteristics. The signal-to-noise ratio of the VCSEL and its impact on the performance of the electro-optical measurement system is analyzed.

This chapter is structured as follows. Section 3.2 presents the design and characterization of the laser bias circuit, as well as the bias modules used to set the operating point of the laser diode. In Section 3.3 laser diodes from different manufacturers and in different package types are characterized. In Section 3.4 the equivalent circuit model of the VCSEL is presented. In Section 3.5 the optimized laser layout is characterized and the signal-to-noise ratio of the electro-optical measurement system is evaluated. The summary is given in Section 3.6.

This chapter is based on the following papers:

[87] Štimac, H., Blečić, R., Gillon, R., Barić, A., "Differential Electro-Optical Equivalent Circuit Model of a Vertical-Cavity Surface-Emitting Laser for Common-Mode Rejection Ratio Estimation", Journal of Lightwave Technology, Vol. 37, No. 24, Dec 2019, pp. 6183-6192.

[89] Štimac, H., Gillon, R., Barić, A., "Broadband radiofrequency design of a laser diode bias circuit", in 2016 22nd International Conference on Applied Electromagnetics and Communications (ICECOM), Sep 2016, pp. 1-6.

## 3.2 Laser bias circuit

The laser bias circuit is used to set the DC bias current of the laser diode, while blocking the radio frequency signal from entering the bias circuit instead of the laser diode. The bias circuit is designed to operate in the frequency range up to 5 GHz. Given the wide operating frequency range of the bias circuit, the main challenge is to achieve a large enough input impedance at high frequencies. Different laser diode bias methodologies are described in [88]. The bias circuit is realized using microstrip transmission lines and surface-mount components. While ferrite beads offer a higher maximum impedance than comparable resistors, their impedance drops significantly at frequencies above 1 GHz [91]. Resistors are very linear and display predictable behaviour even at frequencies of several gigahertz [2]. An example of this is shown in [73] and [92]. Several different bias circuits are designed and characterized. Electromagnetic simulation software is used to optimize the bias circuit designs [93]. Test printed circuit boards are designed and their S-parameters are measured. Based on the performance of the initial design, potential areas of improvement are explored. Design changes are proposed and explored using electromagnetic simulation software. The bias circuit design is optimized and evaluated over several iterations.

### 3.2.1 Laser DC characterization

The voltage-current characteristic of the characterized VCSEL is measured and presented in Fig. 3.2. The laser is characterized in the safe range of bias currents, up to 7 mA, although higher bias currents are allowed. In this range, the maximum output optical power is around 1 mW. The optimum laser bias point is selected in the center of the linear region in order for the laser to be able to work with maximum RF signal amplitudes. A bias current of 4 mA is selected, with the maximum amplitude of approximately 2 mA. For asymmetric voltage waveforms, the bias current can be adjusted to be near the minimum or maximum current of approximately 2 mA and 6 mA, respectively. The dynamic resistance of the VCSEL is matched for differential applications and is around 100 Ω.

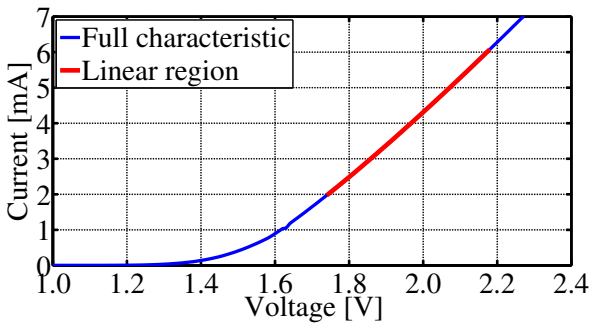
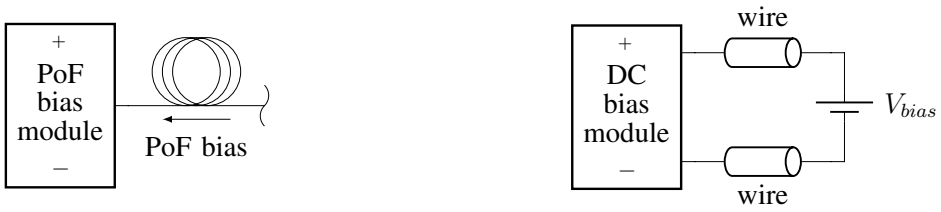



**Figure 3.2:** Measured voltage-current characteristic of the characterized VCSEL.

### 3.2.2 Bias modules

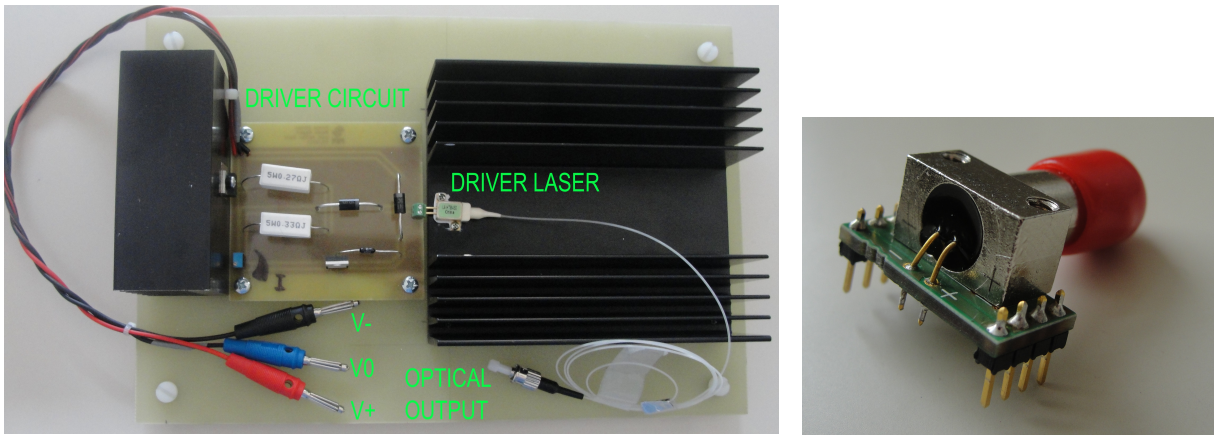
Bias modules are connected to the bias circuit and used as the power supply to bias the laser diode. Two types of bias modules are used for the research presented in this thesis. The first one is a power-over-fiber (PoF) bias module [94], shown in Fig. 3.3a. The PoF bias module is used as a reference for an isolated power supply. The PoF bias module consists of a PoF receiver module mounted to a PCB, as shown in Fig. 3.4b. The power is supplied using an optical fiber to the PoF receiver module, which converts it into an electrical signal used to bias the laser. The PoF module used provides a constant voltage of around 6 V [94], while the required bias current is set by adjusting the optical power provided by the PoF driver laser, shown in Fig. 3.4a. By using an optical fiber connection, electrical isolation of the probe power supply is achieved. By using both an isolated power supply and an isolated RF signal path, complete galvanic isolation of the probe circuit is achieved.




(a) Isolated power supply PoF bias module.

(b) Non-isolated power supply DC bias module.

**Figure 3.3:** Schematic of the isolated power supply PoF bias module and the non-isolated power supply DC bias module.




(a) PoF driver circuit.

(b) PoF receiver module.

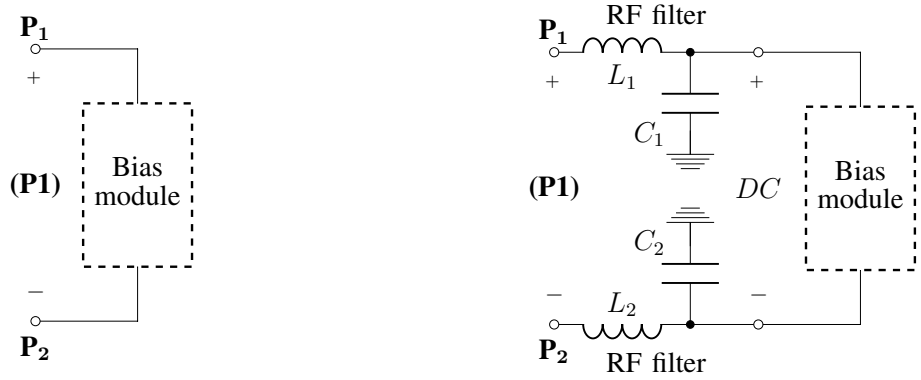
**Figure 3.4:** Isolated power supply PoF bias driver circuit and receiver module design.

The second type of the bias module is used as a reference for a non-isolated power supply. The non-isolated DC bias module consists of a PCB with two differential wires which are directly connected to a DC voltage source, as shown in Fig. 3.3b. The DC bias module is used in constant voltage mode, where the required laser bias current is set by the DC voltage source.

The DC bias module is used to evaluate the impact of the noise coming from the power supply and noise coupling on the wires, on the performance of the characterized probes. Although noise immunity of a wired DC connection can be improved using ferrite loaded wires, coaxial cables, and by filtering the noise coming from the power supply as described in [88], such improvements are not made. The goal is to evaluate the performance of the electro-optical measurement system in the best case and worst case scenario for the power supply isolation. The performance of the bias circuits, lasers and the probe circuits when using the isolated PoF power supply and the non-isolated DC power supply is compared.

### Bias module RF characterization

The bias modules are characterized using a characterization structure which has two sockets which are used to connect the bias module PCB. The bias modules are characterized as differential devices with two physical ports $P_1$ and $P_2$, which form the differential logical port (P1), as shown in Fig. 3.5a. Two-port S-parameters of the structures are measured using a two-port VNA [68]. The measurements are performed in the frequency range from 1 MHz to 5 GHz. The differential input impedance $Z_{d1}$ at the logical port (P1) of the bias module characterization structure is calculated using (2.73) and (2.74), as described in Section 2.1.4. The input impedance is measured when the socket terminals of the bias module characterization structure are left open, when a Thru calibration module is connected between the two ports, when the non-isolated power supply DC bias module is connected, and when the isolated power supply PoF bias module is connected. The magnitude of the measured differential input impedance $Z_{d1}$ for all four bias module terminations is shown in Fig. 3.6.




(a) Bias module characterization setup.

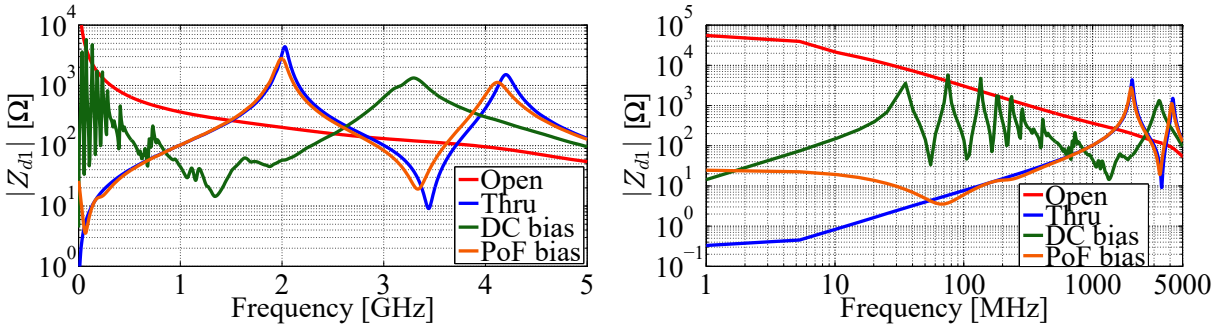
(b) Bias module RF filtering characterization setup.

**Figure 3.5:** Schematic of the bias module characterization setup (left) and the bias module characterization setup with RF noise filtering (right).

When the ports of the bias module characterization structure are left open, the differential input impedance $Z_{d1}$ drops steadily from a very high value at low frequencies. This is a result of the PCB and socket parasitics, as well as the transmission line effects at higher frequen-

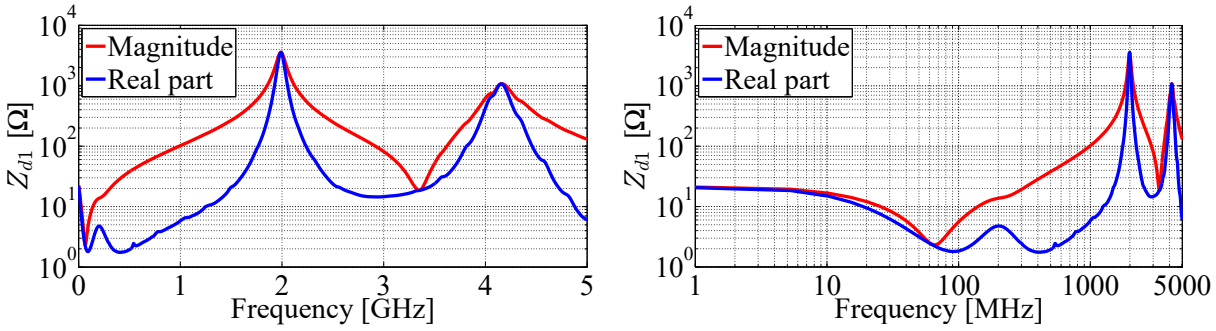
cies. No resonances are observed, indicating good wideband performance of the sockets and the characterization structure. The measurement results of the Thru calibration structure show antiresonances at 2 GHz and 4.2 GHz, and a resonance at 3.4 GHz. This is a result of the interface between the sockets on the characterization PCB and the headers on the bias module PCB, as well as the signal propagation through the transmission lines on the bias module PCB. The measurement results of the non-isolated power supply DC bias module display significant noise at lower frequencies up to 2 GHz, manifested in the form of numerous resonances and antiresonances. The nominal input impedance of the DC bias module at low frequencies is under 10 Ω, and corresponds to the input impedance of the DC voltage source. The antiresonance in the characteristic around 3.3 GHz is a result of the impact of the signal propagation through the DC bias module PCB, as well as the relatively long differential wires connecting the DC bias module and the DC voltage source, given that no RF noise filtering is used.

The measurement results of the isolated power supply PoF bias module are very similar to the Thru calibration structure. This indicates that the dominant resonance at 3.3 GHz and the antiresonances at 2 GHz and 4.1 GHz are introduced by the signal propagation through the PoF bias module PCB. The PoF bias module has a low nominal input impedance at low




(a) Linear frequency scale. (b) Logarithmic frequency scale.

**Figure 3.6:** Measurements of the bias module characterization setup terminated with an open circuit, the Thru calibration module, the non-isolated power supply (DC bias) module, and the isolated power supply (PoF bias) module. The magnitude of the differential-mode input impedance $Z_{d1}$ is compared.




(a) Linear frequency scale. (b) Logarithmic frequency scale.

**Figure 3.7:** Comparison of the measured magnitude and real part of the differential-mode input impedance $Z_{d1}$ of the characterized isolated power supply PoF bias module.

frequencies, below 100 Ω. The low input impedance of the PoF bias module does not contribute significantly to the input impedance of the bias circuit, which needs to be high in comparison to the 100 Ω dynamic resistance of the VCSEL. In comparison to the characteristic of the non-isolated power supply DC bias module, there is no noise present in the characteristic of the isolated power supply PoF bias module. This makes the PoF bias module the preferred choice for usage in the electro-optical probes and characterization structures explored in this thesis. The RF characteristics of the bias modules are not dependent on the bias current level. The magnitude and real part of the measured differential input impedance $Z_{d1}$ of the isolated power supply PoF bias module are shown in Fig. 3.7. At frequencies up to 70 MHz the real part has the dominant impact on the trend of the impedance magnitude. At higher frequencies the impedance magnitude is on average around ten times higher than the real part of the impedance.

### Bias module RF filtering

Based on the characterization results of the bias modules, a circuit design with additional RF filtering is evaluated. The RF filter has two main functions: increasing the differential input impedance of the bias circuit seen by the input RF signal at the port (P1), and suppression of the RF noise coming from the DC input of the bias circuit, through the bias module. The bias module characterization structure with an additional RF filter is shown in Fig. 3.5b. The characterization structure is used to evaluate the impact of the different RF filter configurations on the differential input impedance of the isolated power supply PoF bias module.

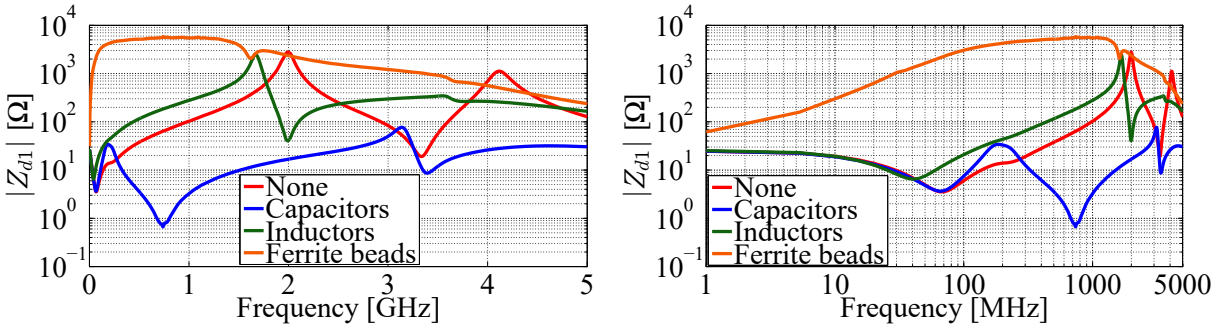
All components used are in a 0402 imperial surface-mount package in order to minimize the size of the filter circuit and reduce the parasitics introduced. Series inductors are used to block the RF signal while allowing the DC signal to pass through. Inductors with an inductance of 12 nH [95] and ferrite beads [92] are used as the inductive components. The small component package size limits the available inductance, but allows for inductors with a self resonant frequency in the gigahertz range to be used. Ferrite beads have a higher maximum impedance, but a worse tolerance than inductors, which can introduce more unwanted asymmetry into the bias circuit. The small DC resistance of the ferrite beads is not an issue in terms of the added impedance and power consumption. Shunt capacitors with a capacitance of 100 pF [80] are used for filtering the RF noise coming from the power supply by directing it towards the ground. Three different configurations of the RF filter are used, as listed in Table 3.1. One configuration uses only series inductors (Inductors), and the other uses only series ferrite beads as the inductive elements (Ferrite beads), while the shunt capacitor pads are left open. Another configuration uses only the shunt capacitors to filter the signal (Capacitors), while the series inductor pads are shorted. A configuration without the RF filter is used as a reference (None), where the series inductor pads are shorted and the shunt capacitor pads are left open.

The magnitude of the differential input impedance $Z_{d1}$ of the isolated power supply PoF bias

**Table 3.1:** Configurations of the bias module RF filter shown in Fig. 3.5b.

| Configuration | $L_1, L_2$ | $C_1, C_2$ |
|---|---|---|
| None | – | x |
| Capacitors | – | capacitor |
| Inductors | inductor | x |
| Ferrite beads | ferrite bead | x |

module is measured when using the different RF filter configurations. The measurement results are compared in Fig. 3.8. Using series inductive components increases the input impedance, particularly in the frequency range between 100 MHz and 2 GHz. Ferrite beads show superior performance compared to inductors, as they offer a higher input impedance over the entire frequency range and flatten out the resonances and antiresonances in the impedance characteristic. Shunt capacitors lower the input impedance at higher frequencies, as they create a direct low impedance path towards the ground. The performance of the different RF filter configurations is further evaluated by implementing them on the bias circuit design which is characterized in Section 3.2.5.




(a) Linear frequency scale.

(b) Logarithmic frequency scale.

**Figure 3.8:** Comparison of the measurements of the isolated power supply PoF bias module characterized using different RF filter configurations listed in Table 3.1. The magnitude of the differential-mode input impedance $Z_{d1}$ is compared.

### 3.2.3 Bias circuit #1 layout

The initial design of the bias circuit is shown in Fig. 3.9. The bias circuit is designed for biasing a VCSEL in a TOSA package with a flexible PCB. The bias circuit consists of two input resistors, microstrip transmission lines and sockets used for connecting the bias module. The role of the resistors is to achieve a high differential input impedance of the bias circuit. Based

on the voltage-current characteristics of the laser diode used, the selected bias current of 4 mA and the available power supply voltage of 6 V, it is determined that the maximum impedance of the biasing path can be 1 kΩ. Two 500 Ω resistors in a surface-mount 0402 imperial package are used [73]. Two 50-Ohm microstrip transmission lines connect the surface-mount resistors at the RF input of the bias circuit with the sockets used for connecting the bias module. The total power consumption of the laser bias circuit is 24 mW, where approximately 1/3 of the power is used by the laser, while 2/3 are dissipated on the bias circuit input resistors. The bias circuit is realized on the PCB stack-up shown in Fig. 1.3. The transmission lines and SMT resistors are located on the Top layer of the PCB, on the top side of the Rogers substrate, while the Inner layer of the PCB, on the bottom side of the Rogers substrate is used as the ground plane. In order to avoid interference with the signal propagation through the transmission lines, the sockets for connecting the bias module, as well as the input through-hole SMA connectors used to connect the RF signal, are located on the Bottom layer of the PCB, on the bottom side of the FR4 substrate.

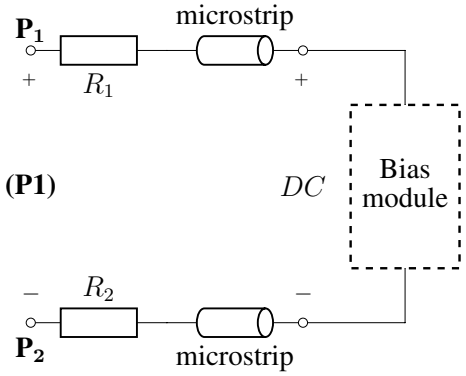
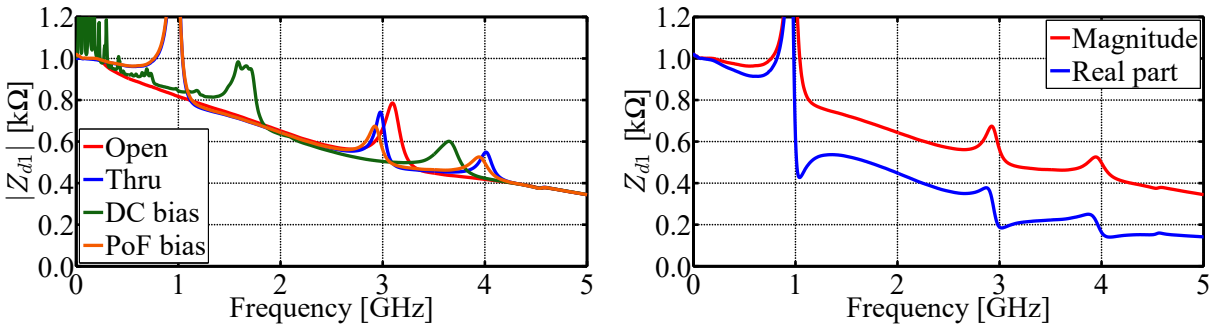



**Figure 3.9:** Bias circuit #1 layout schematic.

The bias circuit #1 layout is characterized as a differential circuit with two physical ports $P_1$ and $P_2$, which form the differential logical port (P1), as shown in Fig. 3.9. Two-port S-parameters of the bias circuit are measured using a two-port VNA [68]. The measurements are performed in the frequency range from 1 MHz to 5 GHz. The differential input impedance $Z_{d1}$ at the logical port (P1) of the bias circuit is calculated using (2.73) and (2.74), as described in Section 2.1.4. The input impedance is measured when no bias module is connected (Open), when a Thru calibration module is connected, when the non-isolated power supply DC bias module is connected, and when the isolated power supply PoF bias module is connected. The magnitude of the measured differential input impedance $Z_{d1}$ for all four bias module socket terminations is shown in Fig. 3.10a.

The general trend of the magnitude of the differential input impedance $Z_{d1}$ of the bias circuit is similar in all four cases. The main difference between the measurements is observed in the frequencies at which the resonant peaks appear. The resonant peaks are present in all four




(a) Impedance magnitude comparison of all bias circuit terminations.

(b) Impedance magnitude and real part when using the PoF bias module.

**Figure 3.10:** Differential-mode input impedance $Z_{d1}$ measurements of the characterized bias circuit #1 layout. Comparison of the magnitude of the input impedance of the bias circuit terminated with an open circuit, the Thru calibration module, the non-isolated power supply (DC bias) module, and the isolated power supply (PoF bias) module (left). Comparison of the magnitude and real part of the input impedance of the bias circuit terminated with the PoF bias module (right).

cases because none of the terminations is equivalent to a 100 Ω differential matched load. As when characterizing only the bias modules (Fig. 3.6), the results of characterizing the Thru calibration structure and the isolated power supply PoF bias module are very similar, with the same low and high frequency values and the resonant peaks appearing at similar frequencies. Significant noise is present in the input impedance characteristic of the non-isolated power supply DC bias module, as a result of the noise from the power supply and noise coupling on the wires. Compared to the non-isolated DC bias module, there is no noise present in the impedance characteristic of the isolated PoF bias module.

The magnitude and real part of the measured differential input impedance $Z_{d1}$ of the bias circuit #1 with the isolated power supply PoF bias module connected are shown in Fig. 3.10b. At frequencies up to 1 GHz the real part has the dominant impact on the trend of the impedance magnitude. At higher frequencies the impedance magnitude is on average around 2–3 times higher than the real part. The differential input impedance of the bias circuit drops from a nominal value of 1 kΩ at low frequencies to 345 Ω at 5 GHz, while the real part of the impedance drops from 1 kΩ to 141 Ω. While the nominal value of the differential input impedance $Z_{d1}$ of bias circuit #1 layout is satisfactory, the input impedance drops to approximately 1/3 of the nominal value at 5 GHz. The goal is to optimize the bias circuit design in order increase the input impedance at higher frequencies and make the impedance frequency profile more stable.

### 3.2.4 Bias circuit #2 layout

Electromagnetic simulations of the bias circuit design are performed using a commercially available EM solver based on the method of moments (MoM) [93]. The goal is to evaluate the differential input impedance profile of the designed bias circuit layout. Based on the two-port

S-parameter simulations, the differential input impedance $Z_{d1}$ of the bias circuit is calculated. An equivalent circuit model of the input 500 Ω resistors is used for the simulations. The circuit model of the resistors used is shown in Fig. 2.17 and described in Section 2.2.1. An ideal 100 Ω resistor is connected instead of a bias module. A 100 Ω resistor is chosen in order to avoid the resonant effects caused by the impedance mismatch. The performance of the bias circuit #1 design is analyzed. Potential areas of improvement of the bias circuit design are explored. The goal is to increase the input impedance at high frequencies. Two main areas of improvement are explored: the resistor solder pad size and creating a slot in the ground plane.

### Solder pad size

The surface-mount solder pads of the resistors $R_1$ and $R_2$ are wider than the 50-Ohm microstrip traces, shown in Fig. 3.9. This sharp change in trace width causes an impedance discontinuity [96]. The goal is to minimize the impact of the resistor solder pads on the input impedance of the bias circuit, by reducing their size. An analysis is performed for different solder pad sizes, for the resistors in a 0402 imperial SMT package. The layout of the solder pads and the surface-mount resistor package is shown in Fig. 3.11.

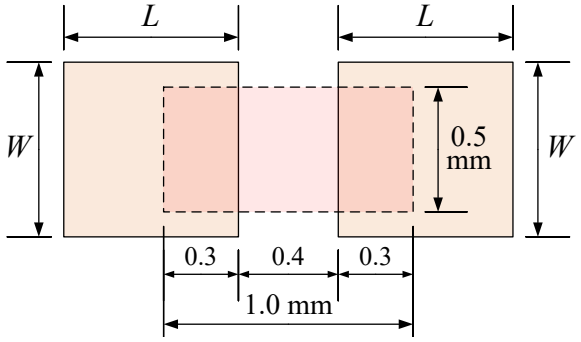



**Figure 3.11:** Resistor 0402 imperial SMT package and solder pad dimensions.

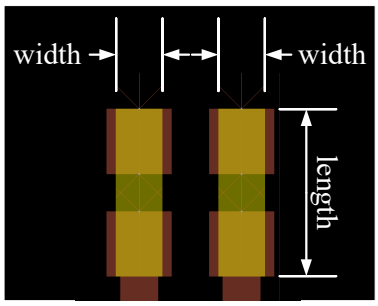
EM simulations are performed for different resistor solder pad sizes. Both ideal and modelled resistors $R_1$ and $R_2$ are used to perform the simulations, in order to evaluate the impact of the solder pad parasitics, in combination with the parasitics related to the internal structure of the resistors, shown in Fig. 2.17. The bias circuit is terminated with an ideal 100 Ω resistor. The solder pad dimensions used on the bias circuit #1 design layout are 0.7 mm x 0.7 mm. The simulation results are shown in Table 3.2. The magnitude of the differential input impedance $Z_{d1}$ at the frequency of 5 GHz is compared. Based on the results presented it can be concluded that a significant impedance gain can be achieved by using smaller solder pad dimensions. This reduces the drop in the input impedance of the bias circuit at high frequencies. However, decreasing the solder pad size makes it increasingly more difficult to solder the SMT components. A compromise is reached and the solder pad dimensions used in the optimized bias circuit design are 0.6 mm x 0.6 mm.

**Table 3.2:** Comparison of the simulation results of the bias circuit #1 layout differential-mode input impedance $Z_{d1}$ for different resistor solder pad sizes.

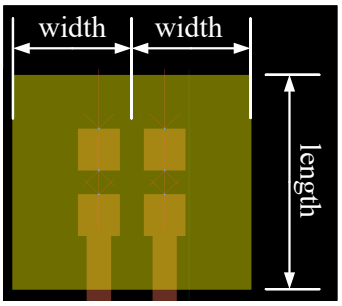
| Pad length | Pad width | $\lvert Z_{d1}$ (@ 5 GHz)$\rvert$ Ideal resistors | $\lvert Z_{d1}$ (@ 5 GHz)$\rvert$ Modelled resistors |
|---|---|---|---|
| 0.7 mm | 0.7 mm | 503 Ω | 336 Ω |
| 0.6 mm | 0.6 mm | 615 Ω | 386 Ω |
| 0.5 mm | 0.6 mm | 692 Ω | 419 Ω |

### Slot in the ground plane

After reducing the size of the resistor solder pads, the impact of using a slot in the ground plane is evaluated. A slot in the ground plane beneath the resistors can decrease the parasitics introduced by the surface-mount pads [96]. In turn, this can lead to an increase in the differential input impedance of the bias circuit [97]. The ground plane slot is positioned under the resistors, on the Inner layer of the PCB (Fig. 1.3), that is, the bottom side of the Rogers substrate, as shown in Fig. 3.12a. If the ground plane slots are wide enough to overlap, they form a single slot as shown in Fig. 3.12b.



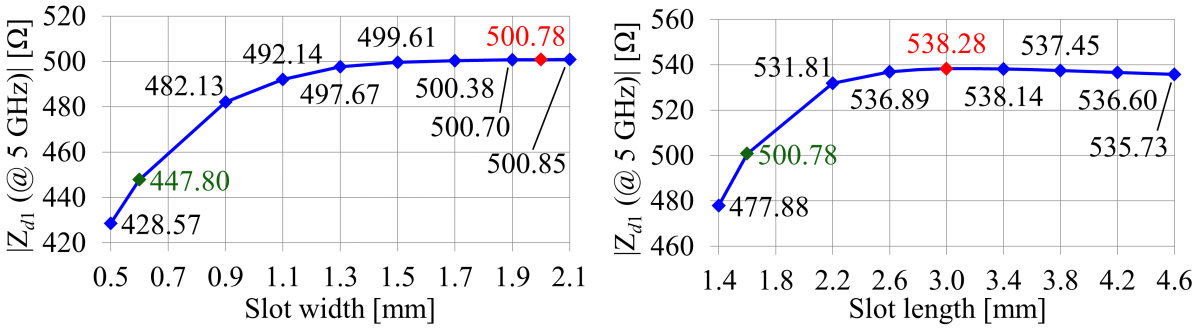

(a) Individual resistor slots.




(b) Combined resistor slot.

**Figure 3.12:** Layout of the slot in the ground plane beneath the resistors.

Initially, the slot length is fixed to 1.6 mm, which is equal to the total resistor footprint length. Electromagnetic simulations of the bias circuit layout are performed. For all ground plane slot simulations, equivalent circuit models of the resistors $R_1$ and $R_2$ are used, the bias circuit is terminated with an ideal 100 Ω resistor, and the solder pad dimensions are 0.6 mm x 0.6 mm. The simulation results for the varied slot widths are shown in Fig. 3.13a. It can be observed that the differential input impedance $Z_{d1}$ of the bias circuit increases with the slot width. However, after a certain width, the increase in impedance is minimal. It is decided that a slot width of 2.0 mm will be used under each resistor, which means that a slot in the ground plane with a total width of 4.0 mm will be used. Finally, the impact of the slot length is




(a) Input impedance as a function of the ground plane slot width (slot length is 1.6 mm).

(b) Input impedance as a function of the ground plane slot length (total slot width is 4.0 mm).

**Figure 3.13:** Simulation results of the magnitude of the differential-mode input impedance $Z_{d1}$ of the bias circuit #2 layout as a function of the ground plane slot width and length. Simulation results when the slot width is equivalent to the solder pad width, and when the slot length is equivalent to the solder pad length, respectively, are highlighted in green. The selected optimum slot width and length dimensions are highlighted in red.

simulated. The slot width is fixed to 4.0 mm. The simulation results are shown in Fig. 3.13b. As it can be seen, the input impedance increases with the slot length up to a certain point, after which it starts to decrease. Based on the simulation results, a slot length of 3.0 mm is chosen, in order to achieve the maximum input impedance of the bias circuit.

### Bias circuit #2 design

The bias circuit #1 design shown in Fig. 3.9 is modified. The size of the resistor solder pads is reduced and slots are added in the ground plane beneath the resistor solder pads. The schematic of the bias circuit #2 layout with these modifications implemented is shown in Fig. 3.14. Compared to the bias circuit #1, the bias circuit #2 design features smaller resistor solder pads, with a size of 0.6 mm x 0.6 mm, as well as a slot in the ground plane with a length of 3.0 mm and a total width of 4.0 mm. A detailed comparison of the two circuit layouts is shown in Fig. 3.15.

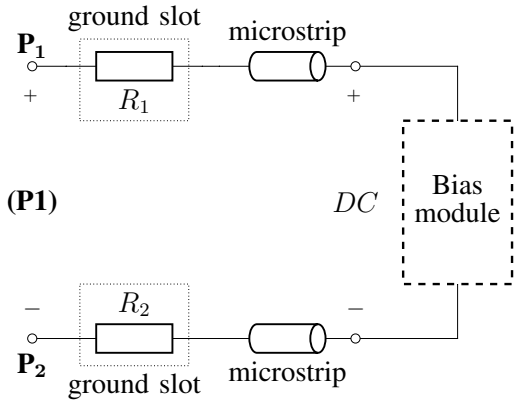



**Figure 3.14:** Bias circuit #2 layout schematic.

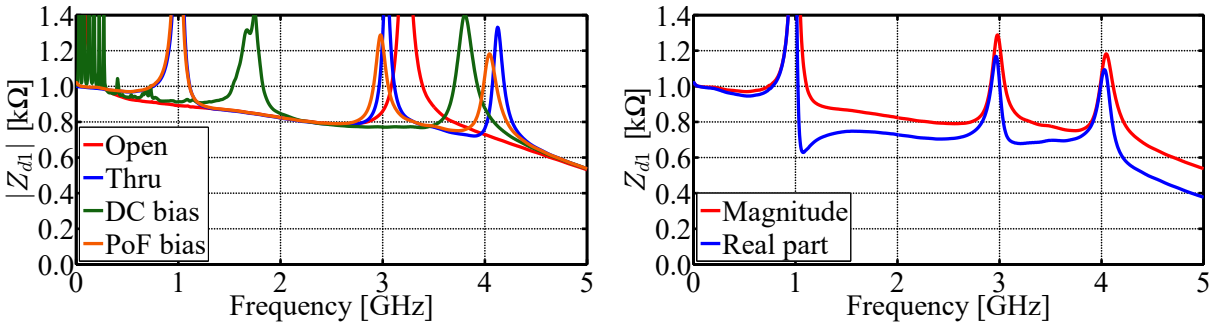
(a) Bias circuit #1 PCB layout detail.

(b) Bias circuit #2 PCB layout detail.

**Figure 3.15:** Comparison of the solder pad and ground slot layout of the bias circuit #1 and bias circuit #2 characterization PCB.

Two-port S-parameters of the bias circuit #2 layout shown in Fig. 3.14 are measured. The differential input impedance $Z_{d1}$ at the logical port (P1) of the bias circuit is calculated. The input impedance is measured when no bias module is connected (Open), when a Thru calibration module is connected, when the non-isolated power supply DC bias module is connected, and when the isolated power supply PoF bias module is connected. The magnitude of the measured differential input impedance $Z_{d1}$ for all four bias module socket terminations is shown in Fig. 3.16a. The general trend of the magnitude of the differential input impedance $Z_{d1}$ of the bias circuit is similar in all four cases. As for the bias circuit #1, the main difference between the measurements is observed in the frequencies at which the resonant peaks appear. The resonant peaks are also more pronounced compared to the bias circuit #1 design, although the resonant frequencies are very similar. The measurement results of the bias circuit with the Thru calibration structure termination and with the isolated power supply PoF bias module are the most similar, while significant noise is present in the measurement using the non-isolated power supply DC bias module.

The magnitude and real part of the measured differential input impedance $Z_{d1}$ of the bias circuit #2 when using the isolated power supply PoF bias module are shown in Fig. 3.16b. As



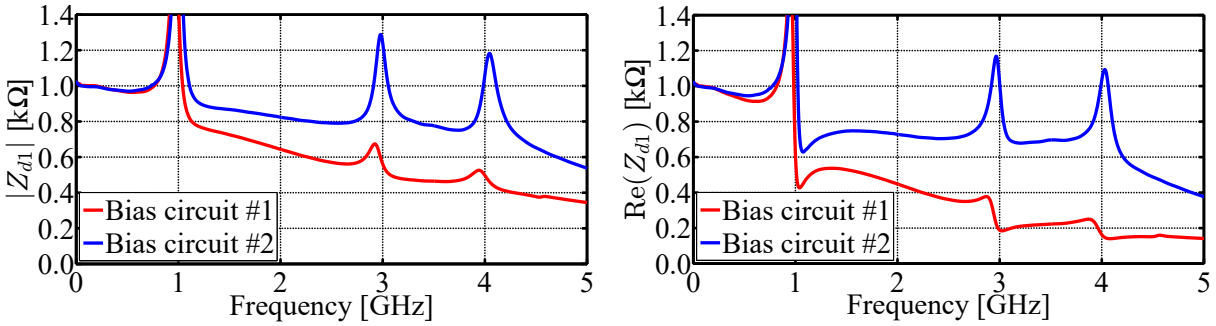

(a) Impedance magnitude comparison for all bias circuit terminations.

(b) Impedance magnitude and real part when using the PoF bias module.

**Figure 3.16:** Differential-mode input impedance $Z_{d1}$ of the characterized bias circuit #2 layout. Comparison of the magnitude of the input impedance of the bias circuit terminated with an open circuit, the Thru calibration module, the non-isolated power supply (DC bias) module, and the isolated power supply (PoF bias) module (left). Comparison of the magnitude and real part of the input impedance of the bias circuit terminated with the PoF bias module (right).

for the bias circuit #1, at frequencies up to 1 GHz the real part has the dominant impact on the trend of the impedance magnitude. At higher frequencies the real part of the impedance is significantly higher relative to the magnitude, when compared to the bias circuit #1, and is mostly at around 80% of the impedance magnitude value. The differential input impedance of the bias circuit drops from a nominal value of 1 kΩ at low frequencies to 537 Ω at 5 GHz, while the real part of the impedance drops from 1 kΩ to 345 Ω.

The differential input impedance $Z_{d1}$ measurement results of the bias circuit #1 and the bias circuit #2 are compared in Fig. 3.17. The bias circuits are terminated with an isolated power supply PoF bias module. The bias circuit #2 design shows a significant increase in the input impedance for frequencies above 1 GHz. At the maximum measurement frequency of 5 GHz, the impedance magnitude is increased by more than 50%. The increase in the real part of the impedance is observable in the same frequency range and it is even more pronounced than the increase of the impedance magnitude. The real part of the input impedance at the maximum measurement frequency of 5 GHz is more than 2.5 times higher for the bias circuit #2 compared to the bias circuit #1. It is demonstrated that the input impedance of the bias circuit is increased at higher frequencies by placing ground plane slots beneath the resistors and by reducing the solder pad size [89]. This reduces the parasitic capacitance and achieves a more stable frequency profile of the differential input impedance of the bias circuit #2.




(a) Magnitude.

(b) Real part.

**Figure 3.17:** Comparison of the measurements of the bias circuit #1 layout and the bias circuit #2 layout, terminated with the isolated power supply (PoF bias) module. The magnitude and real part of the differential-mode input impedance $Z_{d1}$ are compared.

### 3.2.5 Bias circuit #3 layout

The bias circuit #2 design is modified and an RF filter is added to the bias circuit. The RF filter is used to increase the input impedance of the bias circuit seen by the RF signal at the differential input port (P1) and to filter the noise coming from the bias module connected to the DC input of the bias circuit. The bias module filter layout characterized in Section 3.2.2 is implemented in the bias circuit #3 design shown in Fig. 3.18.

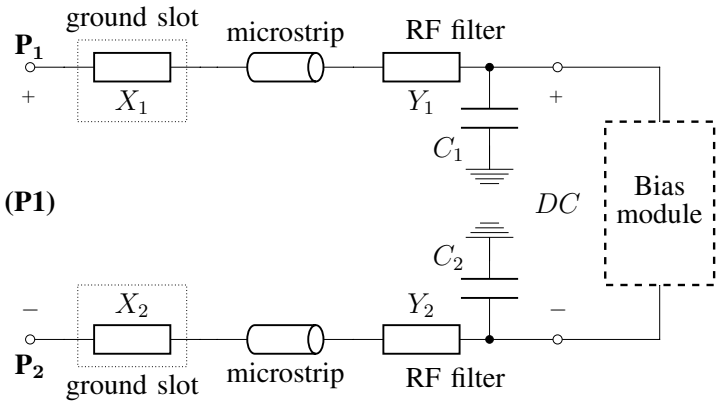



**Figure 3.18:** Bias circuit #3 layout schematic.

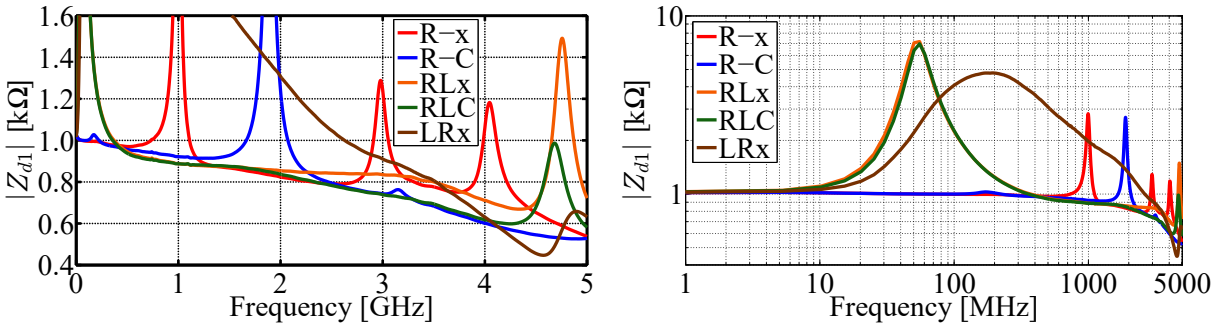
Five different configurations of the bias circuit are used, as listed in Table 3.3. The reference configuration R–x uses only 500 Ω resistors [73] as the input components $X_1$ and $X_2$, while the pads of the series elements $Y_1$ and $Y_2$ are shorted and the shunt element pads $C_1$ and $C_2$ are left open. This configuration is equivalent to the bias circuit #2 design. Configuration R–C uses the resistors as the input components $X_1$ and $X_2$, 100-pF shunt capacitors [80] $C_1$ and $C_2$ are used for filtering the RF noise coming from the power supply and directing it towards the ground, while the series element pads $Y_1$ and $Y_2$ are shorted. Configuration RLx uses the resistors as the input components $X_1$ and $X_2$, ferrite beads [92] are used as the series inductive elements $Y_1$ and $Y_2$ to suppress the RF signal, while the shunt element pads $C_1$ and $C_2$ are left open. Configuration RLC uses the resistors as the input components $X_1$ and $X_2$, the ferrite beads are used as the series inductive elements, and the shunt capacitors $C_1$ and $C_2$ are used as well, in order to achieve maximum filtering of the RF signal. Configuration LRx replaces the position of the inductive and resistive elements, by placing the ferrite beads as the input components $X_1$ and $X_2$, while the resistors are used in place of the series elements $Y_1$ and $Y_2$, and the shunt element pads $C_1$ and $C_2$ are left open. By placing the ferrite beads at the input of the bias circuit, more emphasis is put on the higher maximum impedance of the ferrite beads [91], compared to

**Table 3.3:** Configurations of the bias circuit #3 shown in Fig. 3.18.

| Configuration | $X_1, X_2$ | $Y_1, Y_2$ | $C_1, C_2$ |
|---|---|---|---|
| R–x | resistor | – | x |
| R–C | resistor | – | capacitor |
| RLx | resistor | ferrite bead | x |
| RLC | resistor | ferrite bead | capacitor |
| LRx | ferrite bead | resistor | x |

the more stable impedance profile and a higher impedance at frequencies of several gigahertz of the resistors [2].

Two-port S-parameters of the bias circuit #3 layout shown in Fig. 3.18 are measured. The differential input impedance $Z_{d1}$ at the logical port (P1) of the bias circuit is calculated. The magnitude of the differential input impedance of the bias circuit #3 layout, biased using the isolated power supply PoF bias module, is characterized for the different bias circuit configurations listed in Table 3.3. The measurement results are compared in Fig. 3.19. The capacitive and inductive components in all RF filter configurations flatten out the resonances in the impedance characteristic and shift the frequency of the remaining resonances. The shunt capacitors in the bias circuit configurations R–C and RLC cause a drop in impedance at higher frequencies above 2 GHz, because they introduce a direct ground path for the input RF signal. Series ferrite beads introduce a spike in the input impedance in the lower frequency range. This spike is relatively narrow and is limited to frequencies between 10 MHz and 400 MHz for the configurations RLx and RLC. The best performance is observed for the configuration LRx. Using ferrite beads at the input of the bias circuit results in the maximum increase of the input impedance for frequencies up to 3.5 GHz. With this design the magnitude of the differential input impedance remains above 1 kΩ up to 2.6 GHz. The bias circuit LRx configuration utilizes the high maximum impedance of the ferrite beads at the input of the bias circuit, while using resistors in the RF filter extends the frequency bandwidth of the bias circuit.




(a) Linear frequency scale.

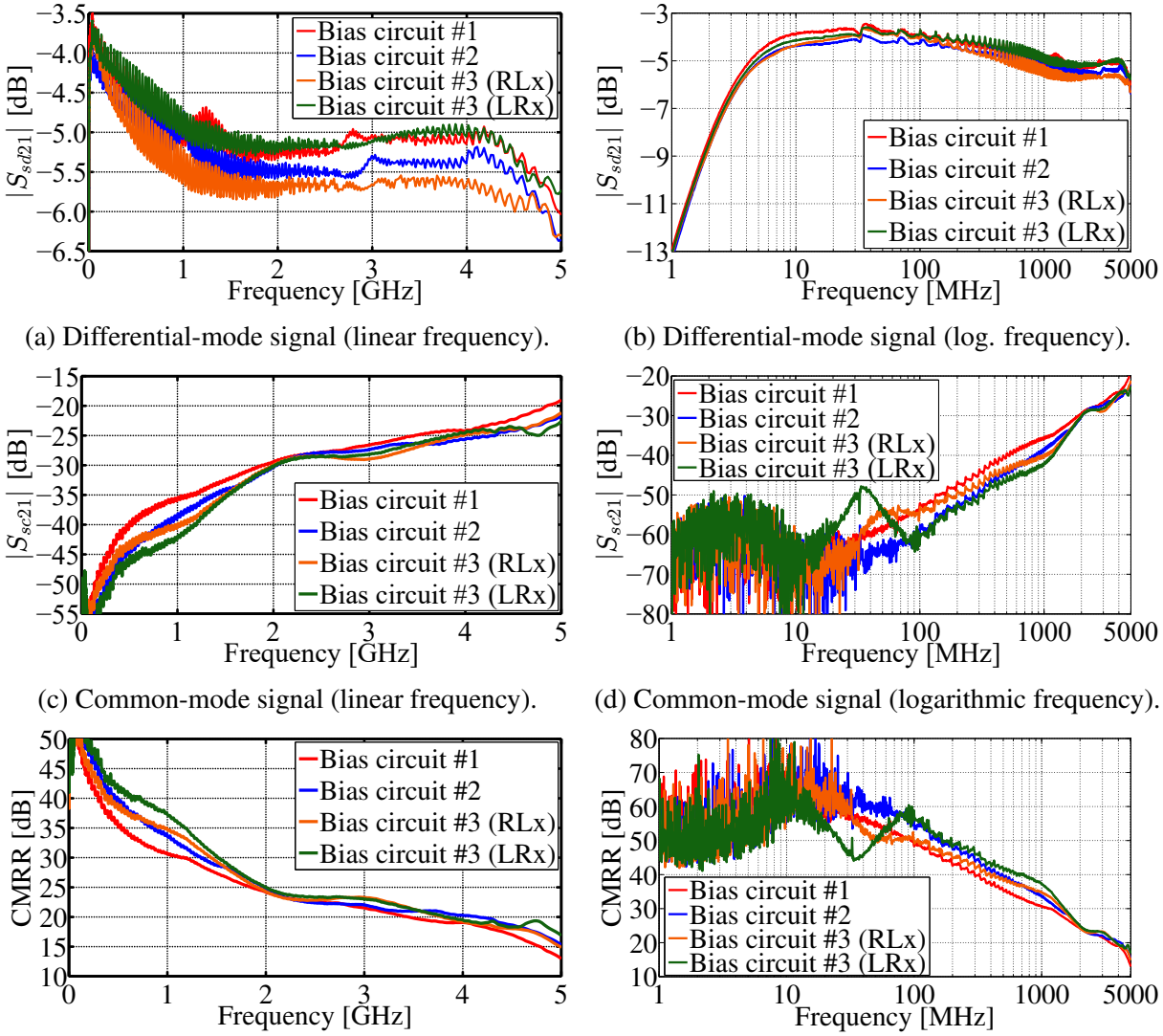
(b) Logarithmic frequency scale.

**Figure 3.19:** Comparison of the measurements of the bias circuit #3 layout characterized using different RF filter configurations listed in Table 3.3, terminated with the isolated power supply (PoF bias) module. The magnitude of the differential-mode input impedance $Z_{d1}$ is compared.

### Bias circuit design comparison

The results obtained by characterizing the different bias circuit layouts by themselves are verified, by using the different bias circuit designs to bias a laser diode. The VCSEL model #1 with the flexible PCB (Fig. 3.1a) is characterized. The laser is biased using the following four bias circuit layouts: bias circuit #1, bias circuit #2, bias circuit #3 RLx configuration, and bias

circuit #3 LRx configuration. The isolated power supply PoF bias module is used. The laser characterization structure shown in Fig. 3.23 has two physical input ports $P_1$ and $P_2$, which form the logical balanced mixed-mode port (P1). The photodetector output port $P_3$ presents the output port of the probe circuit, which forms the logical single-ended port (P2) for the mixed-mode analysis. Three-port S-parameters of the lasers, each with a different bias circuit design and the same VCSEL layout are measured using a dual-source four-port VNA [67]. The measurements are performed in the frequency range from 1 MHz to 5 GHz. The three-port standard S-parameters are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58). The differential-mode and common-mode signal transmission, as well as the CMRR of the lasers with the different bias circuit designs are compared in Fig. 3.20.




(a) Differential-mode signal (linear frequency).

(b) Differential-mode signal (log. frequency).

(c) Common-mode signal (linear frequency).

(d) Common-mode signal (logarithmic frequency).

(e) Common-mode rejection ratio (lin. frequency).

(f) Common-mode rejection ratio (log. frequency).

**Figure 3.20:** Comparison of the measurements of the VCSEL biased using the different bias circuit layouts. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The isolated power supply (PoF bias) module is used.

The differential-mode transmission coefficient $S_{sd21}$ measurements are very similar for all the four bias circuit layouts, and the difference between the measured characteristics is under 1 dB in the entire frequency range up to 5 GHz. The common-mode transmission coefficient $S_{sc21}$ is the highest for the bias circuit #1 layout. The common-mode signal level is the lowest for the bias circuit #3 LRx configuration in the frequency range between 100 MHz and 1.4 GHz. At higher frequencies, the results for the bias circuit #2 and bias circuit #3 layouts are similar to each other. Given the very similar differential-mode characteristics and the differences in the common-mode characteristics of the bias circuit designs, these differences also translate into the CMRR. It is observed that each new version of the bias circuit design has a higher CMRR. The CMRR is the highest for the bias circuit #3 LRx configuration in the frequency range between 100 MHz and 1.7 GHz. In the medium frequency range, the CMRR characteristics of the different bias circuit designs are comparable. At frequencies close to 5 GHz the bias circuit #3 layout LRx is once again the best.

Compared to the initial bias circuit #1 layout, the CMRR is increased by as much as 7 dB in the frequency range between 100 MHz and 1.5 GHz, with the difference in the CMRR decreasing as the characteristics converge at 2 GHz. At the maximum frequency of 5 GHz, the CMRR is increased by 4 dB. The results of characterizing the bias circuit layouts by themselves are confirmed by the measurements of the lasers biased using the compared bias circuit designs. The bias circuit #3 design LRx configuration is confirmed to be the best bias circuit layout for biasing the VCSEL model with the flexible PCB.

### 3.2.6 Bias circuit #4 layout

The bias circuit #3 layout LRx configuration is modified to fit the VCSEL through-hole package, shown in Fig. 3.1b. The schematic of the new bias circuit #4 layout designed for the through-hole VCSEL package is shown in Fig. 3.21. The new design uses a series combination of ferrite beads and resistors at the input of the bias circuit, in order to achieve the highest possible input impedance in combination with a stable frequency impedance profile. By combining both ferrite beads and resistors at the input of the bias circuit, their relative benefits are utilized. Ground plane slots are added under the two pairs of surface-mount components in order to reduce the parasitics. The bias circuit #4 layout, that is, the microstrip transmission lines, are longer compared to the bias circuit #3 layout in order to compensate for the length of the flexible PCB which is not present on the through-hole VCSEL package.

The bias circuit #4 layout is realized using two types of inductive components: ferrite beads and conical inductors. Compared to conventional inductors in the same package size, conical inductors typically have a higher and more stable impedance over a wider range of frequencies. Conical inductors in a 0402 imperial SMT package with an inductance of 840 nH are used [98]. Two VCSELs in a through-hole package are measured. One laser is biased using the bias cir-

cuit #4 layout realized using ferrite beads [92], while the other is biased using the bias circuit #4 layout realized using conical inductors [98].

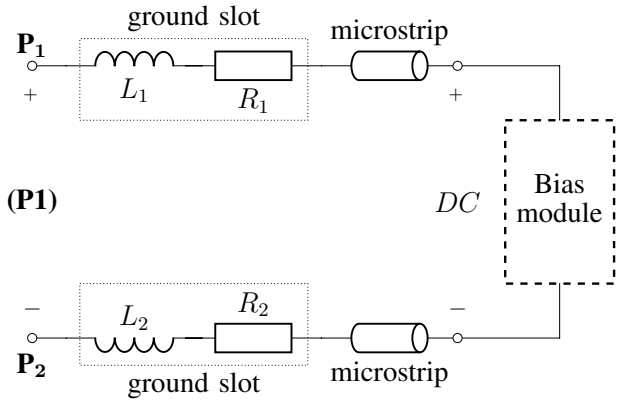
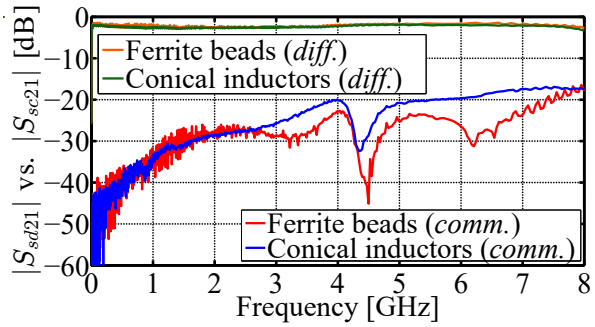



**Figure 3.21:** Bias circuit #4 layout schematic.

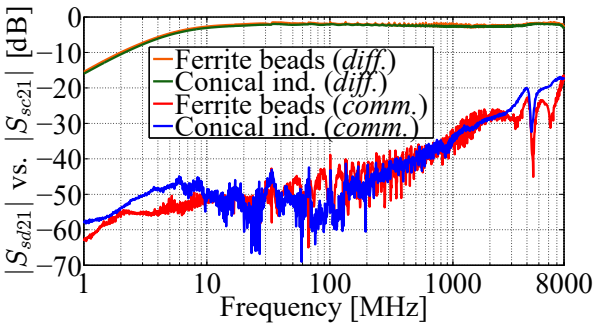
Three-port S-parameters of the laser characterization structure shown in Fig. 3.23 are measured using a two-port VNA [68]. The measurements are performed in the frequency range from 1 MHz to 8 GHz. The mixed-mode S-parameters are calculated and compared in Fig. 3.22. The VCSEL is biased using the isolated power supply PoF bias module. The differential-mode transmission coefficient $S_{sd21}$ is very similar for both bias circuits, without any notable differences. The general trend of the common-mode transmission coefficient $S_{sc21}$ is similar in the frequency range up to 2.6 GHz. At higher frequencies, the common-mode signal level is lower for the bias circuit design realized using the ferrite beads, with the difference between the two characteristics being 5–10 dB. The resonant frequency around 4.5 GHz remains similar.

The difference between the two common-mode characteristics translates into the difference in the CMRR. In the frequency range up 2.6 GHz, the general trend of the CMRR characteristics is very similar for both bias circuit layouts. At higher frequencies, using the ferrite beads results in an increase in CMRR of between 5 dB and 10 dB. For the bias circuit realized using the ferrite beads, the CMRR of the VCSEL remains above 20 dB up to 7.1 GHz, compared to 3.5 GHz for the bias circuit realized using the conical inductors. While the higher and more stable impedance of the conical inductors offers advantages compared to conventional inductors, the broadband characteristics of the ferrite beads offer superior performance overall, particularly at higher frequencies above 2.6 GHz. Ferrite beads also offer other advantages compared to conical inductors, like better mechanical robustness, as well as easier and more repeatable soldering, which results in better repeatability of the bias circuit characteristics. The bias circuit #4 layout realized using the ferrite beads is used to bias the VCSELs in the through-hole package that are characterized in this thesis [87].

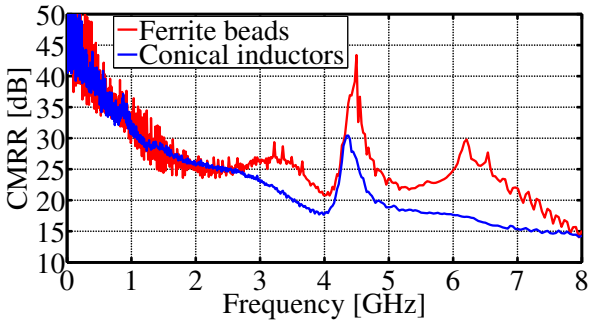
The implemented bias circuit design achieves a relatively stable and high input impedance, as well as good symmetry. The good characteristics of the bias circuit ensure that the input RF signal is routed into the laser diode, and is blocked from going into the bias circuit. The



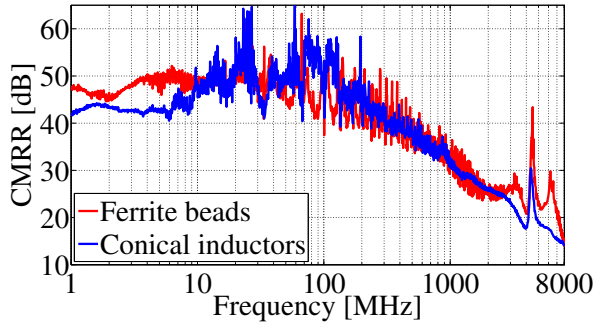

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 3.22:** Comparison of the measurements of the VCSEL biased using the bias circuit #4 layout realized using ferrite beads and using conical inductors. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The isolated power supply (PoF bias) module is used.

dimensions of the bias circuit are designed to fit on the |Z| Probe® [14] PCB layout. In general, using a more compact bias circuit design with shorter transmission lines is possible. Using shorter transmission lines results in a smaller drop in input impedance at higher frequencies and a more stable frequency impedance profile. The miniaturization of the bias circuit design is limited by the size of the VCSEL package and the PoF receiver module package, given that sufficient space must be left in order to be able to connect the optical fiber. Using a larger gap between the two components, also results in less coupling between the metal parts of the VCSEL and PoF receiver module cases.

## 3.3 Laser diode RF characterization

In order to evaluate the performance of the laser models used in this thesis, their RF characteristics are measured. VCSELs in a package with a flexible PCB and in a through-hole package are characterized. Lasers from two different manufacturers are used. The schematic of the laser characterization structure is shown in Fig. 3.23. The laser characterization structure is realized on the PCB stack-up shown in Fig. 1.3. The central part of the laser characterization structure is the VCSEL that is characterized. The VCSEL is mounted on the Bottom layer of the PCB, on the bottom side of the FR4 substrate. The VCSEL is characterized in a differential configuration where the physical port $P_1$ is connected to the laser anode (+) and the physical port $P_2$ is connected to the laser cathode (–). An optical fiber is connected to the VCSEL. The input RF signal of the differentially driven laser is converted into an optical signal and transmitted to a photodetector. The physical output port $P_3$ of the photodetector represents the output port of the laser characterization setup.

The VCSEL characterization results include the entire electro-optical signal path: the electrical signal path in the laser, the electro-optical signal conversion in the laser, the transition between the laser and the optical fiber, the signal transmission through the optical fiber, the transition between the optical fiber and the photodetector, the opto-electrical signal conversion in the photodiode and the electrical signal path in the photodetector up to the output port. The measured RF characteristics of the VCSEL are dependent on the photodetector model [69] used for the characterization. The photodetector characteristics determine the lower cutoff frequency and the noise floor. As discussed in Section 2.1.3, the measurement results close to the lower cutoff frequency of the photodetector of 2 MHz, where the common-mode signal level is typically very low, are difficult to measure accurately. For this reason, the VCSEL characteristics at

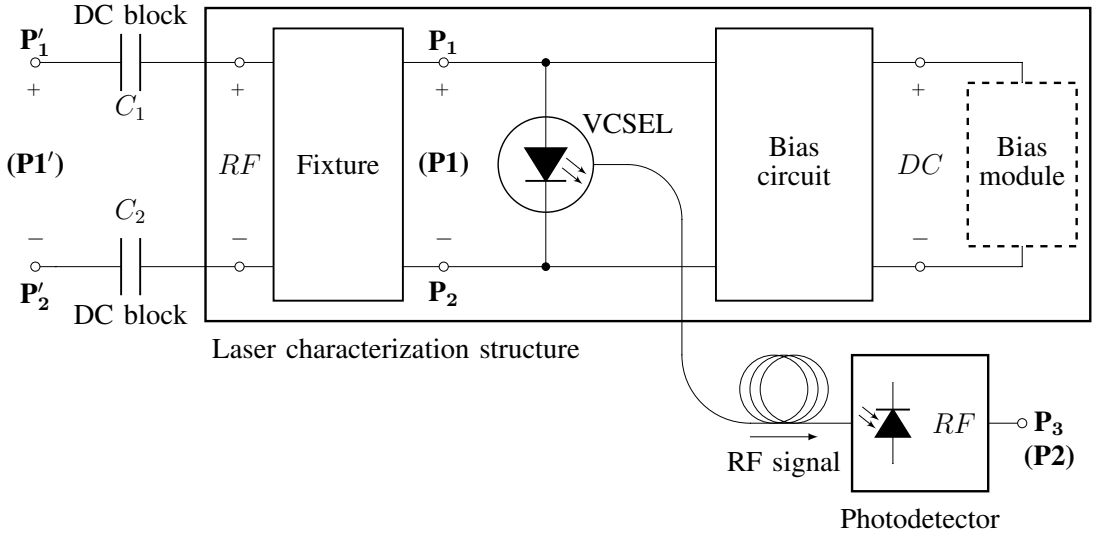



**Figure 3.23:** Laser characterization structure schematic.

frequencies below 100 MHz are typically not taken into account when comparing the different laser layouts presented in this thesis.

Each laser diode is biased using one of the bias circuit designs characterized in Section 3.2, depending on the VCSEL package used. The isolated power supply PoF bias module (Fig. 3.3a) and the non-isolated power supply DC bias module (Fig. 3.3b) can be connected to the bias circuit using sockets. The bias circuit is realized on the Top layer of the laser characterization PCB, while the bias module is connected on the Bottom layer of the PCB. At the input of the laser characterization structure, there is a fixture consisting of two SMA connectors and two transmission lines. The type of the transmission lines used and the layout of the traces depend on the VCSEL model that is characterized. One SMA connector is connected to the laser anode, and the other is connected to the laser cathode. The transmission lines of the fixture are realized on the Top layer of the PCB, while the input SMA connectors are placed on the Bottom layer. In this way, the ground plane on the Inner layer of the laser characterization PCB separates the Bottom layer, on which all the cables are connected, and the Top layer used for routing the traces. External DC block components [99] are connected to the input of the laser characterization structure in order to prevent the DC bias signal from going into the VNA. The laser measurement setup is shown in Fig. 3.24.

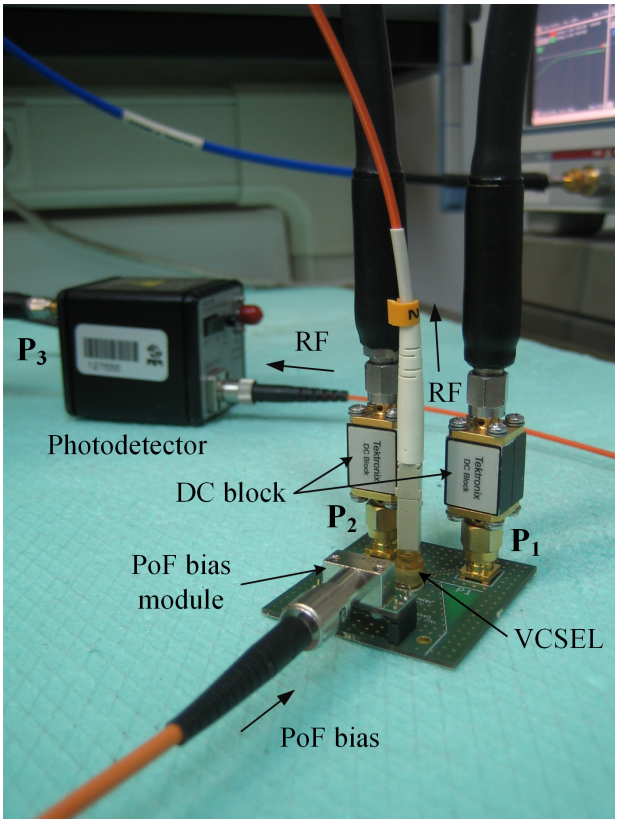
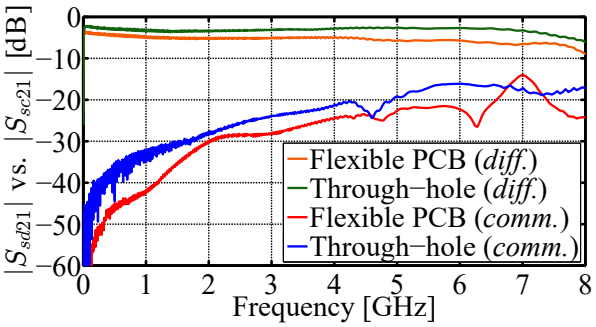



**Figure 3.24:** Laser measurement setup.

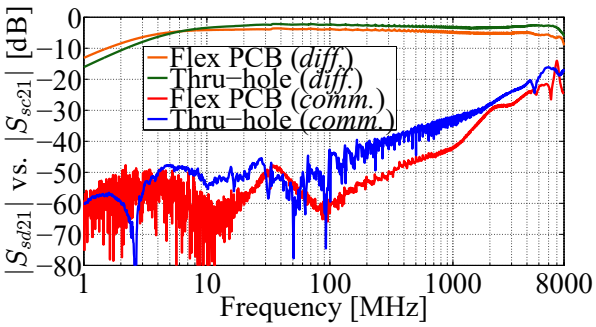
### 3.3.1 Laser package comparison

The VCSEL model #1 [90] is characterized in the package with the flexible PCB (Fig. 3.1a) and in the through-hole package (Fig. 3.1b). The first laser characterization structure is designed for the VCSEL package with the flexible PCB, biased using the bias circuit #3 design LRx configuration (Fig. 3.18), described in Section 3.2.5. The second laser characterization structure is designed for the VCSEL through-hole package, biased using the bias circuit #4 design realized using ferrite beads (Fig. 3.21), described in Section 3.2.6. The isolated power supply PoF bias module shown in Fig. 3.3a is used. Three-port S-parameters of the two laser characterization structures are measured. The measurements are performed in the frequency range from 1 MHz to 8 GHz. The VCSEL with the flexible PCB is measured using a dual-source four-port VNA [67]. The VCSEL in the through-hole package is measured using a two-port VNA [68]. The impact of the test fixture is de-embedded from the measurement results, and the reference plane is shifted from the ports $P_1'$ and $P_2'$ to the ports $P_1$ and $P_2$ at the input of the VCSEL, as shown in Fig. 3.23. Mixed-mode S-parameters are used to evaluate the performance of the characterized VCSELs. The two physical ports $P_1$ and $P_2$ form the logical balanced input port (P1), and the output single-ended physical port $P_3$ forms the logical single-ended output port (P2) for the mixed-mode analysis. The three-port standard S-parameters are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58).

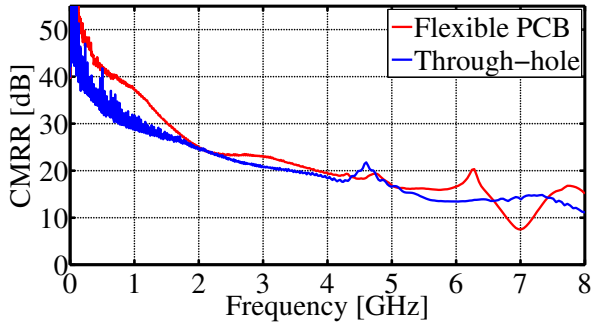
The characteristics of the VCSEL model #1 in the package with the flexible PCB and the through-hole package are compared in Fig. 3.25. The value of the differential-mode transmission coefficient $S_{sd21}$ is around –3 dB for both VCSEL models. The differential-mode signal of the VCSEL with the flexible PCB is around 1.5 dB lower than the VCSEL in the through-hole package at lower frequencies around 100 MHz, while the difference increases to around 3 dB at frequencies of several gigahertz. The differential-mode signal level is very stable for both lasers. It remains within $\pm$3 dB of the nominal value up to 7.8 GHz for the through-hole laser and up to 7.7 GHz for the laser with the flexible PCB. The differential signal level of the laser with the flexible PCB is lower because of the longer signal transmission path and the higher attenuation of the signal in the flexible PCB. The common-mode transmission coefficient $S_{sc21}$ for both characterized VCSELs increases steadily in the frequency range up to 2 GHz. At higher frequencies, the common-mode signal continues to increase, but at a slower rate. The common-mode level is lower for the laser with the flexible PCB in almost the entire frequency range, by around 3–10 dB. The CMRR of the laser with the flexible PCB is higher in the frequency range up to 2 GHz. At higher frequencies the results are more comparable, with more resonances in the CMRR characteristic of the VCSEL with the flexible PCB. The CMRR is above 20 dB up to 3.9 GHz for the VCSEL with the flexible PCB, and above 3.4 GHz for the through-hole VCSEL package.



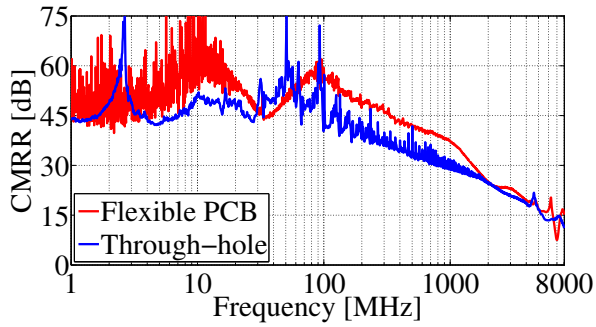

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

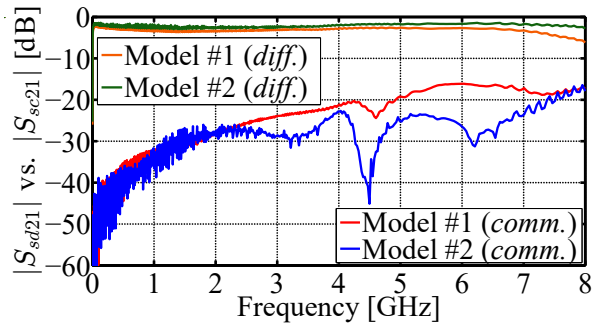
**Figure 3.25:** Comparison of the measurements of the VCSEL model #1 in the package with the flexible PCB and in the through-hole package. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The lasers are biased using the isolated power supply (PoF bias) module.

### 3.3.2 Laser model comparison

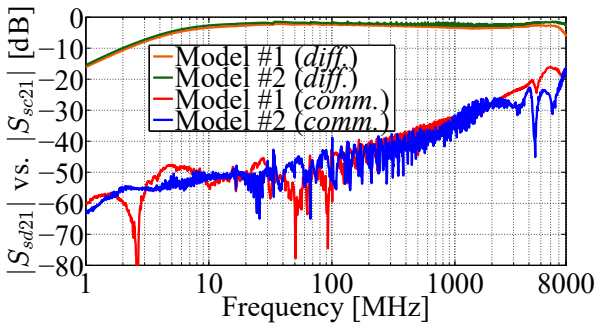
The VCSEL model #2 is sourced from a different manufacturer [100]. Only the 5-lead through-hole TOSA package is used, shown in Fig. 3.1b. The voltage, current and power characteristics of the VCSEL model #2 are comparable to the model #1. The VCSEL model #2 is characterized using a structure with the bias circuit #4 design, realized using ferrite beads (Fig. 3.21). The laser is biased using the isolated power supply PoF bias module. Three-port S-parameters of the laser characterization structure are measured using a two-port VNA [68], and the mixed-mode S-parameters are calculated. The mixed-mode S-parameter characteristics of the VCSEL model #2 are compared to the VCSEL model #1 in the through-hole package, as shown in Fig. 3.26. The differential-mode transmission coefficient $S_{sd21}$ is very similar for both lasers in almost the entire frequency range. The VCSEL model #1 has an approximately 1 dB lower differential-mode signal value, which drops off at frequencies above 7 GHz. The VCSEL model #2 differential-mode signal is very stable and remains within $\pm 1$ dB of the nominal value in the entire frequency range up to 8 GHz. The common-mode transmission coefficient $S_{sc21}$ is similar for both lasers in the frequency range up to 300 MHz, and between 1.3 GHz and 2.2 GHz. The common-mode signal level is lower for the VCSEL model #2 in the frequency

range between 300 MHz and 1.3 GHz, with the difference of around 3–5 dB, and in the high frequency range above 2.2 GHz, with the of difference of around 5–10 dB. The resonance around 4.5 GHz is also more pronounced for the VCSEL model #2.

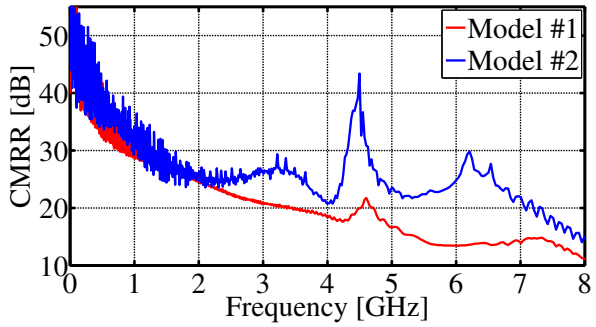
Given the similar differential-mode characteristics, the difference between the common-mode characteristics of the two lasers translates into the difference in the CMRR. The CMRR of both lasers is comparable in the frequency range up to 300 MHz, and between 1.3 GHz and 2.2 GHz. In the frequency range between 300 MHz and 1.3 GHz, the VCSEL model #2 has around 3–5 dB higher CMRR. At higher frequencies above 2.2 GHz, the VCSEL model #2 has a higher and more stable CMRR, with the difference between the two characteristics being around 5–10 dB. The CMRR of the VCSEL model #2 remains above 20 dB up to 7.1 GHz. This analysis demonstrates the advantages of using the VCSEL model #2, compared to the VCSEL model #1 in the same package.



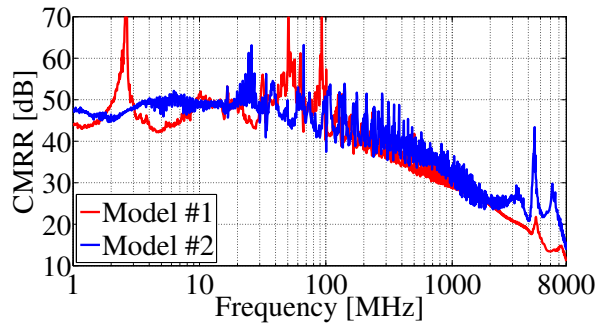

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

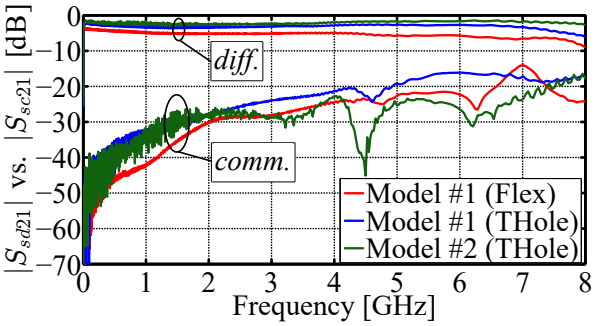
**Figure 3.26:** Comparison of the measurements of the VCSEL model #1 and model #2 in the through-hole package. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The lasers are biased using the isolated power supply (PoF bias) module.

### 3.3.3 Laser model and package comparison

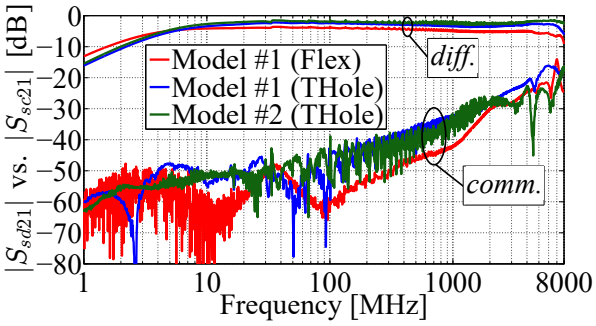
The mixed-mode S-parameter characteristics of the VCSEL model #1 with the flexible PCB, the VCSEL model #1 in the through-hole package, and the VCSEL model #2 in the through-hole

package are compared in Fig. 3.27. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is similar for all three lasers. The differential-mode signal level is the highest and most stable for the VCSEL model #2, while it is the lowest for the VCSEL model #1 with the flexible PCB. The common-mode transmission coefficient $S_{sc21}$ is the lowest for the VCSEL model #1 with the flexible PCB in the frequency range up to 2.3 GHz. In the higher frequency range above 2.9 GHz, the common-mode signal level is in general the lowest for the VCSEL model #2, while the VCSEL model #1 in the through-hole package has the worst common-mode signal suppression.

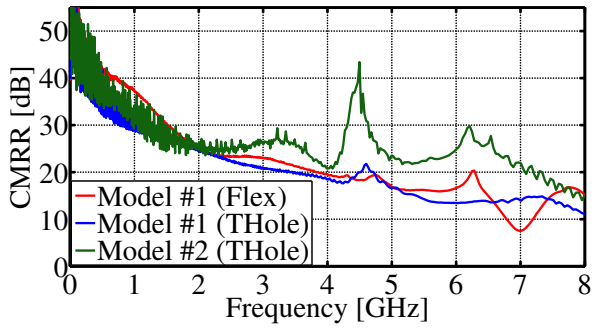
The CMRR of the VCSEL model #1 with the flexible PCB is the highest in the frequency range up to 1.8 GHz, and is between 3 dB and 5 dB higher than for the VCSEL model #2. At higher frequencies, the VCSEL model #2 has the highest CMRR, which is around 5–10 dB higher than for the VCSEL model #1 with the flexible PCB. In order to achieve good characteristics of the electro-optical probe circuit, the benefits of having a higher and more stable CMRR over a wide high frequency range outweigh the downsides of having a slightly lower CMRR in the lower frequency range, where the absolute CMRR level is relatively high. By having a more stable frequency profile of the CMRR, a wider bandwidth of the probe circuit can be



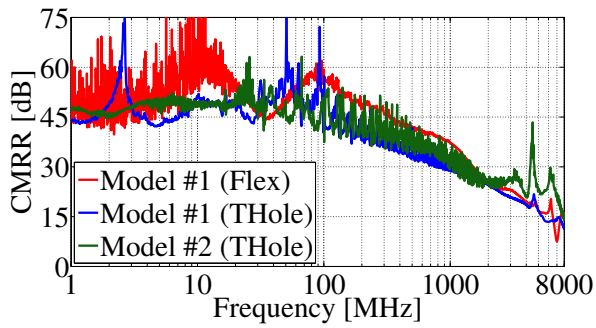

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).



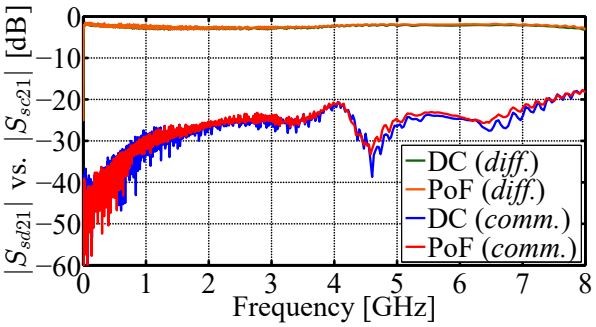

(d) Common-mode rejection ratio (log. frequency).

**Figure 3.27:** Comparison of the measurements of the VCSEL model #1 in the package with the flexible PCB, the VCSEL model #1 in the through-hole package, and the VCSEL model #2 in the through-hole package. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The lasers are biased using the isolated power supply (PoF bias) module.

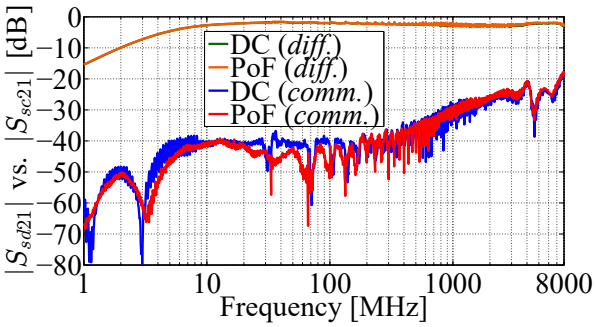
achieved. Additionally, the through-hole VCSEL package offers significant benefits in terms of mechanical robustness, eliminating the sensitivity of the RF characteristics of the flexible PCB to bending and twisting, better stability and repeatability of the optical connection, as well as a smaller circuit size due to eliminating the flexible PCB. For these reasons, the VCSEL model #2 is used in the laser diode and probe circuit layouts discussed in the remainder of this thesis.

### 3.3.4 Laser power supply isolation

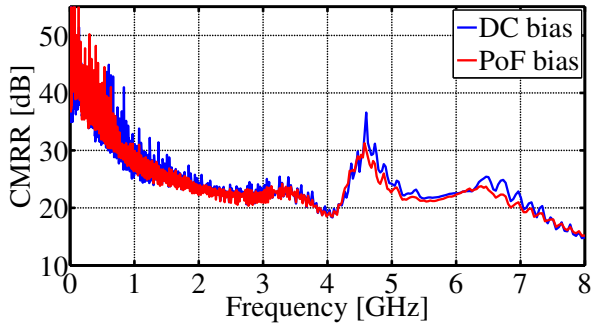
The mixed-mode S-parameters of the VCSEL model #2 are presented in Fig 3.28. The characteristics of the VCSEL model #2 biased using the isolated power supply PoF bias module (Fig. 3.3a) and the non-isolated power supply DC bias module (Fig. 3.3b) are compared. The impact of the power supply isolation on the characteristics of the VCSEL is evaluated. The differential-mode transmission coefficient $S_{sd21}$ is very similar for both bias methods, without any significant differences. The general trend and level of the common-mode transmission coefficient $S_{sc21}$ is also very similar when using both bias methods. The level of ringing differs slightly between the two characteristics, with the isolated PoF bias module characteristic being slightly smoother.



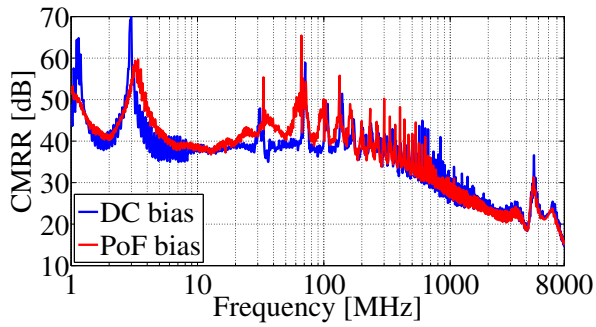

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 3.28:** Comparison of the measurements of the VCSEL model #2 biased using the isolated power supply (PoF bias) module and the non-isolated power supply (DC bias) module. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

The same is true for the comparison of the CMRR characteristics of the two bias modules. The general trend of the two CMRR characteristics is very similar, with the characteristic of the VCSEL measurement when using the isolated PoF bias module being slightly smoother. Given that there are no significant differences between the measurement results using the two bias methods, it can be concluded that there is no significant impact of the power supply isolation on the VCSEL characteristics, when the VCSEL is characterized by itself in the presented differential configuration.

## 3.4 Laser equivalent circuit model

Existing VCSEL equivalent circuit models are typically presented in a single-ended configuration [101–115]. These models commonly include an equivalent circuit model of the laser chip, with elements representing the different regions of the laser diode structure [101]. Most papers include two-port single-ended VCSEL chip models, based on the physical layout of the chip and the contacts [102–109]. The VCSEL chip model can be expanded to a three-port model, where the parasitics towards the ground are not modelled [110]. Some three-port VCSEL models include a rate equation model, along with the single-ended equivalent circuit model [111]. Other VCSEL models also include the bondwire and electrical package parasitics, with the standard VCSEL chip model and parasitics [112–115]. Modelling of the laser dynamics in terms of the light-current and thermal characteristics by using rate equations and behavioral models is an integral part of existing equivalent circuit models [116–119].

Transistor outline (TO) headers are widely used for opto-electronics packaging applications [120]. The TO-46 header is a commonly used package for VCSEL chips [121, 122]. Some papers model only the TO-headers without the VCSEL chip, in particular the TO-46 header model [123]. Other TO-Can header circuit models are also available, featuring similar lumped element model structures [124]. Although these papers discuss package-related parasitics, the header models are typically presented in a single-ended configuration.

A small-signal differential electro-optical equivalent circuit model of a VCSEL is extracted. In contrast to existing VCSEL models which are typically presented in a single-ended configuration and are focused on modelling the laser dynamics, the presented differential model is primarily aimed at modelling the parasitics related to the VCSEL package as well as the internal structure of the VCSEL chip, and the impact of the parasitic asymmetry on the propagation of the differential-mode and common-mode signals.

A methodology combining Y-parameters and mixed-mode S-parameters is used to create a differential equivalent circuit model of the VCSEL. The model is extracted from the measurements of the laser diode S-parameters. The electrical characteristics of the VCSEL chip are modelled using the admittance Π-model. The parasitics between the laser package and the characterization printed circuit board are modelled. The impact of the asymmetry of the parasitics from each of the signal pins towards the ground plane is examined. The electro-optical and opto-electrical conversion of the signal are modelled using an approach based on the mixed-mode S-parameters. The differential-mode signal represents the wanted signal transmitted by the laser diode. The common-mode signal is the unwanted signal. The differential VCSEL model is used to model the behaviour of the transmission coefficients for both differential-mode and common-mode input signals. The ratio between the differential-mode and the common-mode signal is expressed as the common-mode rejection ratio.

The circuit model is developed for a 5-lead VCSEL in a TOSA package. The laser is mounted on a characterization printed circuit board. The laser diode bias circuit is realized on the characterization structure in order to recreate a practical usage scenario. In this way, the biasing is separated from the measurement process. The laser is operating in the linear region, with a constant bias current. The three-port S-parameters of the VCSEL are measured. The circuit model is developed in order to model the transmission of differential-mode and common-mode signals for EMC and ESD measurements in an electromagnetically polluted environment. The model covers the frequency bandwidth between 1 MHz and 5 GHz, required for these applications. By calculating the CMRR, the ratio between the wanted and unwanted signal levels can be estimated. All the elements in the proposed lumped element equivalent circuit model are frequency independent.

### 3.4.1 Measurement

The characteristics of the VCSEL model #2 [100] in the 5-lead through-hole TOSA package (Fig. 3.1b) are measured. The laser is specified for data rates up to 10 Gbit/s. The laser diode is mounted on a characterization printed circuit board. The VCSEL characterization structure consists of a fixture, the laser diode and the bias circuit. The schematic of the VCSEL characterization structure is shown in Fig. 3.29. The test fixture is realized using CBCPW feed lines and two through-hole SMA connectors. The CBCPW topology is used for the 50-Ohm transmission lines, in order to minimize the coupling between the two input signal paths [81]. The laser bias circuit #4 design (Fig. 3.21) described in Section 3.2.6 is used. The isolated power supply PoF bias module [94], shown in Fig. 3.3a, is used as the voltage source to bias the laser diode. In this way, complete galvanic isolation of the measurement system is achieved. The VCSEL operating point is selected in the center of the linear region, based on the voltage-current characteristics, in order to allow for maximum RF signal amplitudes. A constant bias current of 4 mA is used for the S-parameter measurements.

The VCSEL characterization setup is shown in Fig. 3.29. The RF measurements are performed using a two-port VNA [68]. DC blocks [99] are connected to the two RF input ports of the VCSEL characterization structure, in order to prevent the DC bias signal from going into the VNA. The DC block and the bias circuit input SMT components form a bias tee. The VNA output power is set to –7 dBm allowing for a higher dynamic range, while assuring that the laser diode operates in the linear region. A three-port S-parameter matrix of the structure is measured. The measurement calibration plane is set at the input of the DC blocks. Port $P_1$ is connected to the VCSEL anode (+), while port $P_2$ is connected to the VCSEL cathode (–). Port $P_3$ represents the output of the photodetector, that is used for the VCSEL characterization. The measured signal transmission function includes the impact of the entire electro-optical signal path: the electrical signal path in the laser, the impact of the electro-optical conversion of the

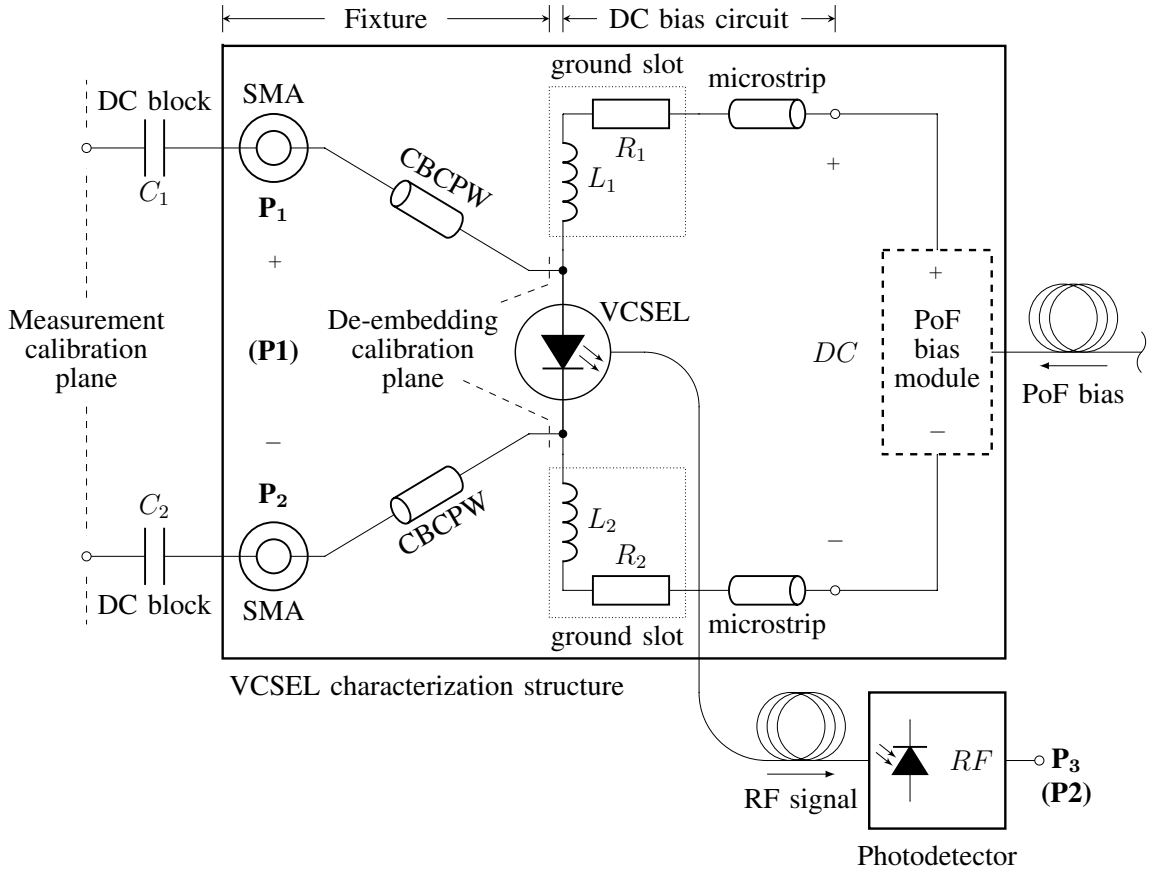



**Figure 3.29:** VCSEL characterization setup schematic.

signal in the laser diode, the partial reflection of the signal at the transition between the optical fiber and the laser diode, the attenuation of the signal in the optical fiber, the partial reflection of the signal at the transition between the optical fiber and the photodetector, the opto-electrical conversion of the signal in the photodetector, and the impact of the electrical signal path in the photodetector. The lower cutoff frequency is limited by the low-frequency cutoff of 2 MHz of the photodetector [69] used to perform the measurements.

Through-open-short-match (TOSM) calibration is used to calibrate the VNA [68]. A number of calibration structures are measured in order to extract the characteristics of the fixture. An electromagnetic simulation of the fixture CBCPW transmission line layout is performed using a commercially available EM solver based on the method of moments [93]. The equivalent circuit model presented in [82], and shown in Fig. 2.19, is used to model the characteristics of the input SMA connectors. The parameters of the connector circuit model are optimized and fitted to the measurement results of the calibration structures. The impact of the fixture on the measurement results is de-embedded. The calibration plane is shifted to the VCSEL anode and cathode pins, as shown in Fig. 3.29. The measurement correction performed at the photodetector output port is described in Section 3.4.3. The de-embedded three-port S-parameters of the VCSEL represent the basis for extracting the circuit model.

### 3.4.2 Electrical circuit model

A two-by-two S-parameter matrix of the two VCSEL input ports ($P_1$ and $P_2$) is extracted from the three-port measurement results. The S-parameters are converted to Y-parameters [23]. The Π-model elements (Fig. 2.13b), are calculated from the Y-parameters using (2.60)–(2.63), as described in Section 2.1.4. The Π-model is used to create an equivalent electrical circuit model of the VCSEL, as seen from the two input electrical ports. The paths from the laser anode and cathode towards the ground plane are modelled. A lumped element network is used to model each of the Π-model elements. The lumped elements of the equivalent Π-model network are optimized and fitted to the Π-model parameters extracted from the VCSEL measurement results. The complete proposed equivalent circuit model of the VCSEL is shown in Fig. 3.30. The optimized circuit model parameters are listed in Table 3.4.

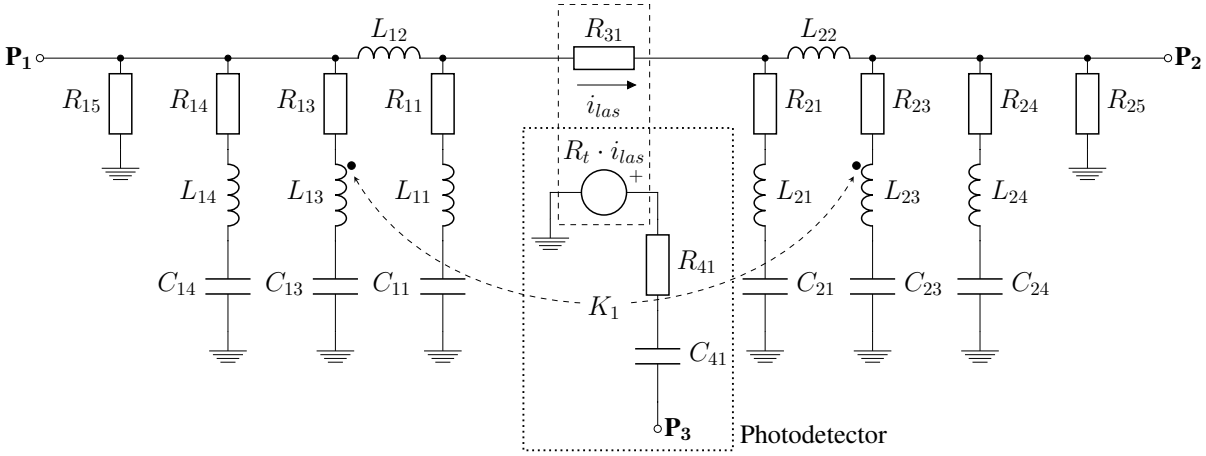



**Figure 3.30:** Proposed three-port VCSEL equivalent circuit model.

**Table 3.4:** VCSEL equivalent circuit model parameters used to fit the model to the measurement results.

| $C_{11}$ | $L_{11}$ | $R_{11}$ | $L_{12}$ | $C_{13}$ | $L_{13}$ | $R_{13}$ | $C_{14}$ | $L_{14}$ | $R_{14}$ | $R_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.53 pF | 2.23 nH | 2 Ω | 1.30 nH | 0.54 pF | 1.625 nH | 3.38 Ω | 8 pF | 4 µH | 500 Ω | 8.6 kΩ |
| $C_{21}$ | $L_{21}$ | $R_{21}$ | $L_{22}$ | $C_{23}$ | $L_{23}$ | $R_{23}$ | $C_{24}$ | $L_{24}$ | $R_{24}$ | $R_{25}$ |
| 0.71 pF | 1.52 nH | 2 Ω | 1.38 nH | 0.50 pF | 1.760 nH | 3.38 Ω | 8 pF | 4 µH | 500 Ω | 30.6 kΩ |
| | | | $K_1$ | $R_{31}$ | $R_t$ | $R_{41}$ | $C_{41}$ | | | |
| | | | 0.145 | 76.9 Ω | 82 Ω | 36.5 Ω | 440 pF | | | |

#### Port-to-ground elements

The port-to-ground elements $Y_1$ and $Y_2$ in the Π-model are used to model the coupling between the laser and the ground plane of the characterization PCB. The signal path from each of the two input ports towards the ground plane is modelled.

The circuit elements $R_{11}$, $L_{11}$, $C_{11}$, $L_{12}$, $R_{13}$, $L_{13}$, $C_{13}$, $R_{14}$, $L_{14}$, $C_{14}$ for port $P_1$ and circuit elements $R_{21}$, $L_{21}$, $C_{21}$, $L_{22}$, $R_{23}$, $L_{23}$, $C_{23}$, $R_{24}$, $L_{24}$, $C_{24}$ for port $P_2$ represent an equivalent lumped element model of the coupling between the laser pins and the ground plane of the characterization PCB, as well as the return signal path.

The series RLC elements closest to each port ($R_{14}$, $L_{14}$, $C_{14}$ for port $P_1$ and $R_{24}$, $L_{24}$, $C_{24}$ for port $P_2$) model the resonance at 30 MHz that appears in the Π-model elements $Y_1$ and $Y_2$ (Fig. 3.31).

The series RLC elements closest to the center of the equivalent circuit ($R_{11}$, $L_{11}$, $C_{11}$ for port $P_1$ and $R_{21}$, $L_{21}$, $C_{21}$ for port $P_2$), in combination with the series inductances next to them ($L_{12}$ for port $P_1$ and $L_{22}$ for port $P_2$), model the resonance at 3.7 GHz that is observed in the Π-model elements $Y_1$ and $Y_2$.

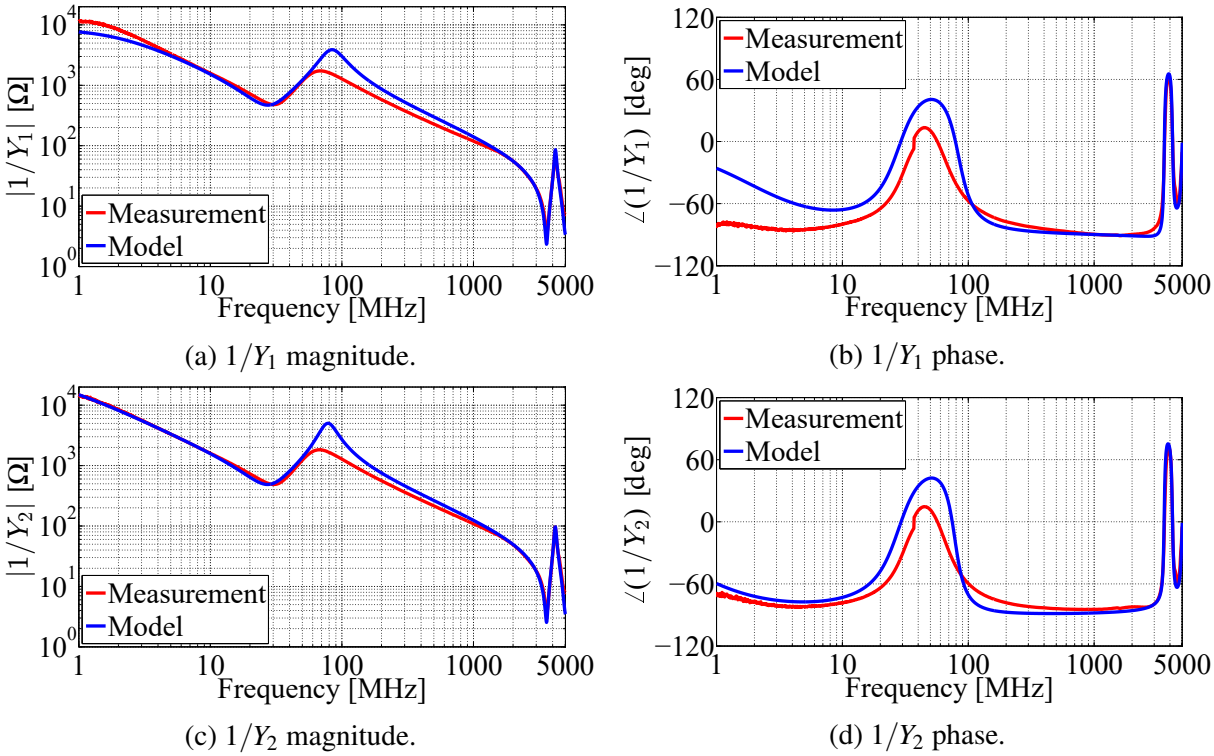
The remaining series RLC elements ($R_{13}$, $L_{13}$, $C_{13}$ for port $P_1$ and $R_{23}$, $L_{23}$, $C_{23}$ for port $P_2$) model the resonance at 4.9 GHz that is visible in the Π-model elements $Y_1$ and $Y_2$. The mutual inductance between the inductances $L_{13}$ and $L_{23}$ models the coupling between the laser leads. The mutual inductance is quantified by the coupling coefficient $K_1$.

The resistances connecting each port to the ground ($R_{15}$ for port $P_1$ and $R_{25}$ for port $P_2$) model the leakage current of the dielectric at low frequencies. The parasitic resistance represents the equivalent parallel resistance of the capacitance between the laser case and the ground plane of the characterization PCB [76]. These resistances model the characteristics of the Π-model elements $Y_1$ and $Y_2$ at low frequencies, below 10 MHz.

An asymmetry between the port-to-ground paths from the anode and from the cathode is observed. The difference exists between the reactive elements that model the high frequency resonances, as well as the resistances used for modelling the dielectric leakage current at low frequencies. These are the following elements of the port-to-ground series RLC circuits: $C_{11}$ and $C_{21}$, $L_{11}$ and $L_{21}$, $C_{13}$ and $C_{23}$, $L_{13}$ and $L_{23}$, as well as the resistances $R_{15}$ and $R_{25}$, and the series inductances $L_{12}$ and $L_{22}$. The origins and the impact of this asymmetry on the signal transmission are explored in Section 3.4.3.

The impedance magnitude and phase of the path from the anode towards the ground, and the path from the cathode towards the ground, are shown in Fig. 3.31. The overall agreement between the proposed circuit model and the measurement results is very good in the whole range of interest, from 1 MHz to 5 GHz. Small differences between the two measured port-to-ground impedances are observed. These differences are modelled by the asymmetries between the two port-to-ground paths in the proposed equivalent circuit. The uncertainty of the reflection coefficient measurements performed using a VNA is higher than for the measurements of the transmission coefficient between the two ports [70]. This effect is emphasized at frequencies below 50 MHz, where the nominal VNA measurement accuracy is lower than at higher frequencies, particularly for phase measurements [68]. The high impedance of the port-to-ground

parasitics at low frequencies additionally limits the measurement accuracy. Despite this measurement uncertainty at low frequencies, the general trend of the magnitude and phase of the port-to-ground impedances is well modelled.




(a) $1/Y_1$ magnitude.

(b) $1/Y_1$ phase.

(c) $1/Y_2$ magnitude.

(d) $1/Y_2$ phase.

**Figure 3.31:** Impedance magnitude and phase of the path from the anode towards the ground in the Π-model ($Y_1$), and the path from the cathode towards the ground in the Π-model ($Y_2$).

### Port-to-port element

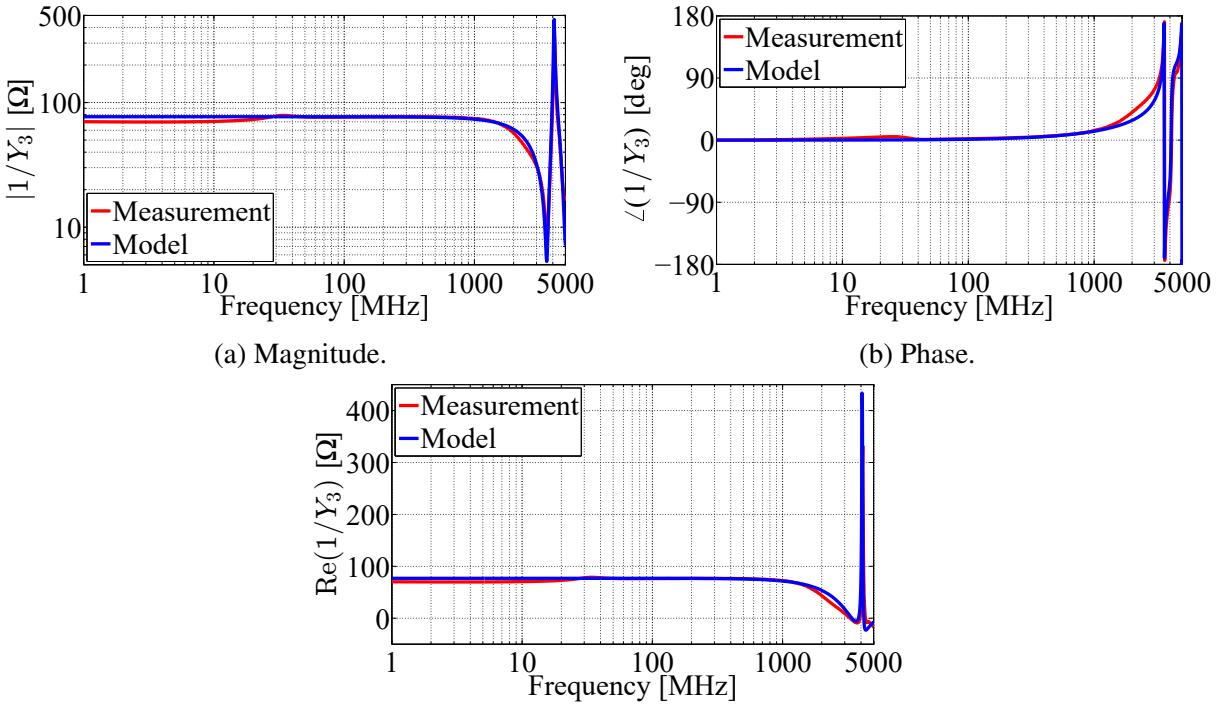
The port-to-port element $Y_3$ in the Π-model is used to model the path between the two VCSEL input ports. The signal propagation between the anode and the cathode is also affected by the Π-model port-to-ground elements $Y_1$ and $Y_2$.

The resistance $R_{31}$ models the active region of the VCSEL chip, where the electrical signal is converted into an optical signal. The resistance models the nominal value of the Π-model element $Y_3$.

The series inductances on each side of the VCSEL active element ($L_{12}$ for port $P_1$ and $L_{22}$ for port $P_2$), in combination with the series RLC elements closest to the active element ($R_{11}$, $L_{11}$, $C_{11}$ for port $P_1$ and $R_{21}$, $L_{21}$, $C_{21}$ for port $P_2$), model the resonance at 3.6 GHz that is observed in the Π-model element $Y_3$ (Fig. 3.32).

The mutual inductance between the port-to-ground inductances $L_{13}$ and $L_{23}$ models the antiresonance at 4.1 GHz that is observed in the Π-model element $Y_3$. The mutual inductance, which is a result of the coupling between the laser leads, is denoted by the coupling coefficient $K_1$.

The impedance magnitude and phase of the port-to-port element are shown in Figs. 3.32a and 3.32b. The real part of the impedance of the port-to-port element, representing the VCSEL active element, is shown in Fig. 3.32c. The overall agreement between the proposed circuit model and the measurement results is very good in the whole range of interest, from 1 MHz to 5 GHz. Given the lower measurement accuracy at low frequencies [68], the real part of the impedance of the port-to-port element is observed in the frequency range from 50 MHz to 500 MHz, where the value is stable. The nominal value of the active element of the VCSEL chip is 76.9 Ω. While the impedance of the port-to-port element is primarily extracted from the transmission coefficient, the reflection coefficient also impacts the value [23]. The measurement uncertainty of the reflection coefficient at low frequencies translates into a small deviation from the nominal value.




(a) Magnitude.

(b) Phase.

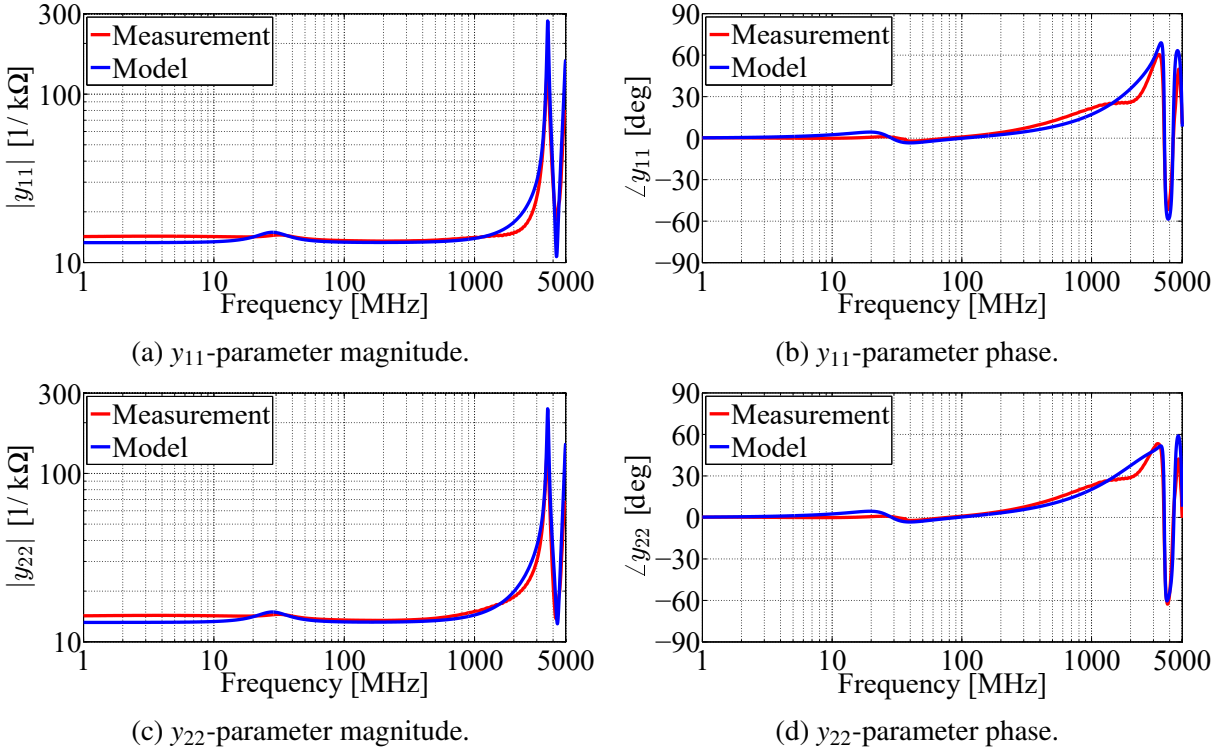
(c) Real part.

**Figure 3.32:** Magnitude, phase and real part of the impedance of the port-to-port element in the Π-model ($Y_3$).

### Π-model verification

The electrical Π-model is verified by observing the fitting between the model and the measurement results for Y-parameters at the input ports $P_1$ and $P_2$. Y-parameters are observed for their clear physical interpretation and sensitivity to small changes in admittance (impedance) values. The admittance magnitude and phase at ports $P_1$ and $P_2$ are shown in Fig. 3.33. The overall agreement between the proposed circuit model and the measurement results is very good in the whole range of interest, from 1 MHz to 5 GHz. Small differences between the two measured

port-to-ground impedances are observed, as a result of the asymmetries in the VCSEL structure, which are discussed in Section 3.4.3. The small discrepancies between the model and the measurements are a result of the limitations of extracting the admittance model previously described in Section 3.4.2.




(a) $y_{11}$-parameter magnitude.

(b) $y_{11}$-parameter phase.

(c) $y_{22}$-parameter magnitude.

(d) $y_{22}$-parameter phase.

**Figure 3.33:** Admittance magnitude and phase at the physical ports $P_1$ and $P_2$.

### 3.4.3 Electro-optical circuit model

For a VCSEL that is used in differential configuration, mixed-mode S-parameters [28] are more suitable to model the electro-optical signal transmission, than the measured standard single-ended S-parameters. The laser diode S-parameter measurement setup is shown in Fig. 3.29. There are three physical ports ($P_1$, $P_2$ and $P_3$), that are used to measure the single-ended S-parameters. The two physical single-ended ports $P_1$ and $P_2$ form the logical balanced port (P1). The physical single-ended port $P_3$ forms the logical single-ended port (P2), for the mixed-mode S-parameter analysis. The mixed-mode S-parameter network has one balanced (differential) port and one single-ended port. The measured single-ended S-parameters are used to calculate the mixed-mode S-parameters using (2.49)–(2.57). The common-mode rejection ratio is defined as the ratio between the wanted differential-mode signal transmission coefficient $S_{sd21}$ and the unwanted common-mode signal transmission coefficient $S_{sc21}$, and is calculated using (2.58).

Based on the mixed-mode S-parameters, the transmission of the differential-mode and the common-mode signal is modelled. The electro-optical signal transmission from the VCSEL

to the photodetector is modelled using a current-dependent voltage source, as shown in the equivalent circuit model in Fig 3.30. In addition to the output network, some of the electrical Π-model elements described in Section 3.4.2 also have an effect on the electro-optical signal transmission. The elements of the circuit model are optimized and fitted to the mixed-mode S-parameters of the measured VCSEL. The optimized circuit model parameters are listed in Table 3.4.

The resistance $R_{31}$ in the Π-model port-to-port element $Y_3$ models the electro-optical signal conversion in the active region of the the VCSEL chip. This controls the transmitted signal level for both the differential-mode and the common-mode signal over the entire frequency bandwidth.

The transfer resistance $R_t$ models the opto-electrical signal conversion in the photodetector, as well as the optical signal transmission, and the losses at the transitions between the laser, the optical fiber and the photodetector. The resistance $R_t$ controls the transmitted signal level for both the differential-mode and the common-mode signal over the entire frequency bandwidth.

The output circuit model resistance $R_{41}$ models the photodetector output impedance. It sets the level of the photodetector output port reflection coefficient at frequencies above 100 MHz. The output resistance also controls the transmitted signal level for both the differential-mode and the common-mode signal over the entire frequency bandwidth.

The output circuit model capacitance $C_{41}$ models the low frequency cutoff of the photodetector. The series capacitance affects the photodetector output impedance at low frequencies, below 100 MHz. The effects of the output series capacitance can be observed in the lower cut-off frequency of the differential-mode signal transmission, below 10 MHz (Fig. 3.38a). This capacitance also affects the slope of the common-mode signal transmission at low frequencies, below 30 MHz (Fig. 3.38b).

The series inductances on each side of the VCSEL active element in the Π-model ($L_{12}$ for port $P_1$ and $L_{22}$ for port $P_2$), as well as the series RLC elements on each side of the inductances ($R_{11}$, $L_{11}$, $C_{11}$ together with $R_{13}$, $L_{13}$, $C_{13}$ for port $P_1$, and $R_{21}$, $L_{21}$, $C_{21}$ together with $R_{23}$, $L_{23}$, $C_{23}$ for port $P_2$), cause the resonance at 4.7 GHz and the high frequency drop-off in differential-mode signal transmission obtained from the circuit model. This resonance is not present in the measurement results (Fig. 3.38a).

The asymmetry between the port-to-ground paths from the anode and from the cathode in the electrical Π-model has a dominant effect on the common-mode signal transmission. The resistances connecting each port to the ground ($R_{15}$ for port $P_1$ and $R_{25}$ for port $P_2$) affect the common-mode signal slope at low frequencies, below 30 MHz. The asymmetric port-to-ground series RLC elements ($R_{11}$, $L_{11}$, $C_{11}$ together with $R_{13}$, $L_{13}$, $C_{13}$ for port $P_1$, and $R_{21}$, $L_{21}$, $C_{21}$ together with $R_{23}$, $L_{23}$, $C_{23}$ for port $P_2$), in combination with the series inductances between them ($L_{12}$ for port $P_1$ and $L_{22}$ for port $P_2$), affect the slope and the level of the common-mode

signal over the entire frequency bandwidth. The greater the asymmetry between the elements, the higher the level of the resulting common-mode signal. The asymmetry between the two port-to-ground paths of the characterized VCSEL is a result of the structural asymmetry of the VCSEL chip, such as the different size and shape of the anode and cathode electrodes, different bondwire lengths, as well as additional asymmetries in the parasitics introduced by the tolerances of the VCSEL packaging and soldering process [125].

### Photodetector Model

The photodetector has an optical input port and an RF output port, as shown in Fig. 3.29. There is a transmission path between the photodiode at the optical input, and the port $P_3$ calibration plane at the output RF connector. This transmission path introduces a phase shift, which can be modelled using an ideal transmission line shown in Fig 3.34. There is also an impedance mismatch between the photodetector output impedance $R_{41}$ and the 50-Ohm characteristic impedance of the VNA. The impedance mismatch and the phase shift result in ringing that is observable in the $y_{33}$-parameter, as shown in Fig. 3.35. Y-parameters are more suitable to display this effect than S-parameters because the ringing is observed in both the magnitude and the phase.

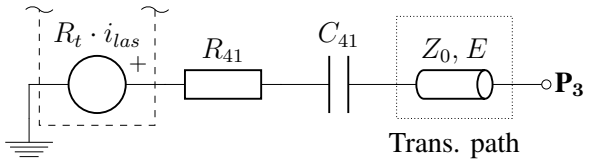
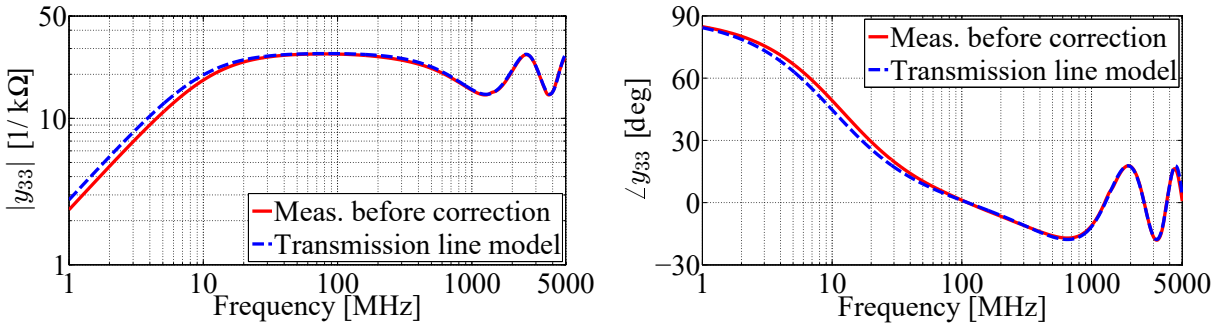



**Figure 3.34:** Photodetector equivalent circuit model with the transmission line segment for modelling the signal transmission path within the photodetector. By fitting the model to the measurement results, the following parameter values are extracted: characteristic impedance $Z_0 = 50\ \Omega$, phase shift $E = 71$ deg (@1 GHz). Other parameter values are listed in Table 3.4.



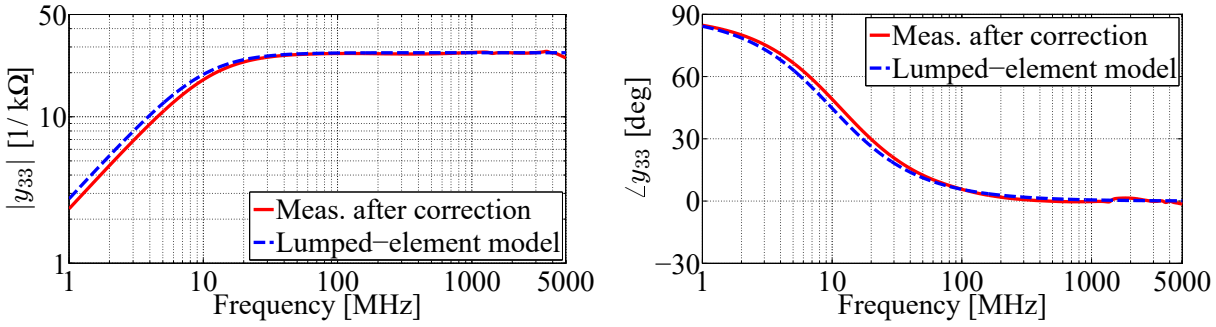

(a) Magnitude. (b) Phase.

**Figure 3.35:** Comparison of the admittance magnitude and phase at the physical port $P_3$ extracted from the measurement results before correction and the photodetector model with the transmission line segment shown in Fig. 3.34.

A measurement correction can be made at the photodetector output port by modelling this transmission path using an ideal transmission line segment. The transmission line segment can

be de-embedded from the output port measurement results in order to correct the phase shift and the ringing. This correction procedure is applied to the measurements, which are modelled using the lumped element model of the photodetector shown in Fig. 3.30. This measurement correction does not affect the magnitude of the differential-mode and common-mode transmission coefficients, as well as the other mixed-mode S-parameters presented in Figs. 3.37 and 3.38. The same correction method can be used to de-embed any adapters that are connected to the photodetector output, as long as their characteristics can be modelled using an ideal transmission line segment within the observed frequency range.

The overall agreement between the proposed circuit model and the measurement results is very good in the whole range of interest, from 1 MHz to 5 GHz, for both the photodetector model with the transmission line segment (Fig. 3.35) and the lumped element photodetector model (Fig. 3.36). The small discrepancy between the model and the measurements at frequencies below 30 MHz is a result of the reflection coefficient measurement uncertainty [68, 70].




(a) Magnitude. (b) Phase.

**Figure 3.36:** Comparison of the admittance magnitude and phase at the physical port $P_3$ extracted from the measurement results after correction and the photodetector lumped element model shown in Fig. 3.30.

The photodetector output port reflection coefficient is shown in Fig. 3.37. The overall agreement between the proposed circuit model and the measurement results is very good in the frequency range from 1 MHz to 4 GHz.

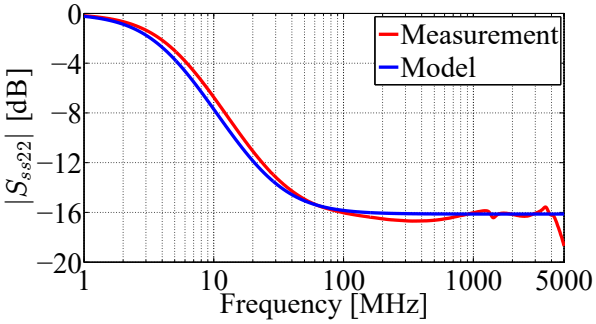



**Figure 3.37:** Output port reflection coefficient of the photodetector used for the VCSEL characterization.

### Electro-optical transmission model

The differential-mode transmission coefficient $S_{sd21}$ of the modelled VCSEL is shown in Fig. 3.38a. The overall agreement between the proposed circuit model and the measurement results is very good in the frequency range from 1 MHz to 4 GHz. At higher frequencies, a resonance is observed in the circuit model, which is not present in the measurement results. This is a limitation of the proposed equivalent circuit model, which combines the modelling of the electrical parasitics of the laser package with the differential-mode signal transmission.

The common-mode transmission coefficient $S_{sc21}$ of the modelled VCSEL is shown in Fig. 3.38b. The general trend of the common-mode characteristic is well modelled in the frequency range from 1 MHz to 4 GHz. There is significant noise in the common-mode characteristic, which results in multiple dips and peaks. The level of the common-mode signal is highly dependent on the small impedance magnitude and phase imbalance between the two port-to-ground paths. Given the measurement uncertainty of these parameters at low frequencies [68, 70], it is difficult to accurately determine the common-mode signal level. Taking into account the approximations in the circuit model used to describe the general trend of the common-mode characteristic, there is an offset between the circuit model and the very noisy common-mode measurement results.

To quantify the fitting of the proposed VCSEL equivalent circuit model to the measurements results, observed in the frequency range from $f_{min}$ to $f_{max}$, the frequency range is divided into $N$ equidistant discrete frequency points $f_i$. The term $y_{meas}(f_i)$ represents the measurement result at the discrete frequency $f_i$ in the observed frequency range, and $y_{model}(f_i)$ represents the result obtained using the proposed equivalent circuit model at the discrete frequency $f_i$. The fitting of the model is quantified using the normalized root-mean-square error (NRMSE) [126] as follows:

$$\text{NRMSE} = \frac{1}{N}\sqrt{\sum_{i=1}^{N}\left(\frac{y_{model}(f_i) - y_{meas}(f_i)}{y_{meas}(f_i)}\right)^2}. \tag{3.1}$$

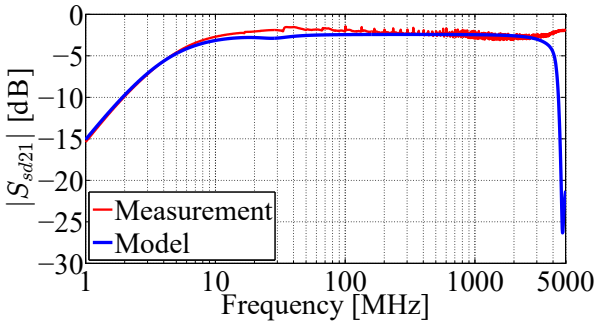
The visual offset seen between the characteristics obtained through measurements, and the characteristics obtained using the proposed equivalent circuit model, which are presented in dB, can be quantified by calculating the mean absolute error (MAE) [127] between the two characteristics expressed in dB. It should be noted that given that the characteristics in the logarithmic decibel scale are compared, the difference between the two characteristics presents the ratio of the two values, rather than the difference of values. The offset in dB is calculated as follows:

$$\text{Offset} = \frac{1}{N}\sum_{i=1}^{N}\left| y_{model}(f_i)\,[\text{dB}] - y_{meas}(f_i)\,[\text{dB}] \right| \,[\text{dB}]. \tag{3.2}$$

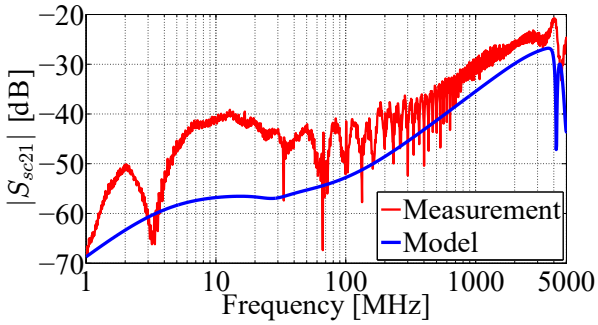
For the common-mode transmission coefficient $S_{sc21}$, shown in Fig. 3.38b, the observed frequency range is from 1 MHz to 4 GHz. The NRMSE of the proposed equivalent circuit model

is 0.004520. The offset between the measurements and the modelled characteristic is 4.1 dB.

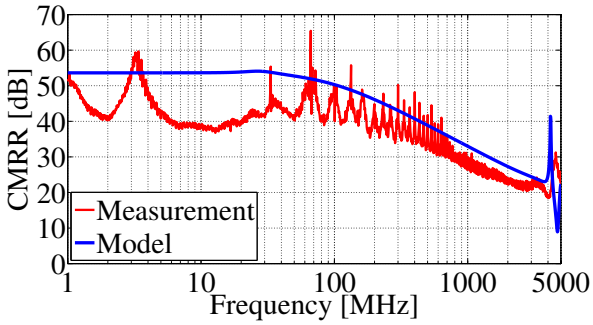
The common-mode rejection ratio of the modelled VCSEL is shown in Fig. 3.38c. The general trend of the CMRR characteristic is well modelled in the frequency range from 1 MHz to 4 GHz. The previously described limitations in modelling the differential-mode and common-mode characteristics affect the accuracy of the CMRR characteristic model. The proposed VCSEL equivalent circuit model is accurate for the differential-mode signal. The model predicts the general trend of the common-mode signal, but there is an offset from the measurement results. This deviation of the common-mode signal translates into a deviation in the CMRR. As a result of the noise in the common-mode characteristic, the CMRR value obtained from the measurements is also very noisy, and there is an offset between the circuit model and the measurement results. The NRMSE and the offset of the CMRR characteristic are calculated in the same way as for the common-mode transmission coefficient, using (3.1) and (3.2), respectively. The NRMSE of the modelled CMRR characteristic is 0.008484, while the offset between the measurement results and the CMRR value obtained from the circuit model is 3.8 dB, in the frequency range from 1 MHz to 4 GHz.




(a) Differential-mode signal transmission.




(b) Common-mode signal transmission.




(c) Common-mode rejection ratio.

**Figure 3.38:** Magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) of the modelled VCSEL.

The asymmetry between the paths from the VCSEL anode and cathode towards the ground, as well as in the internal structure of the laser diode, results in a limited CMRR value. The greater the asymmetry between the port-to-ground Π-model elements, the higher the unwanted common-mode signal level. The presented frequency independent equivalent circuit model

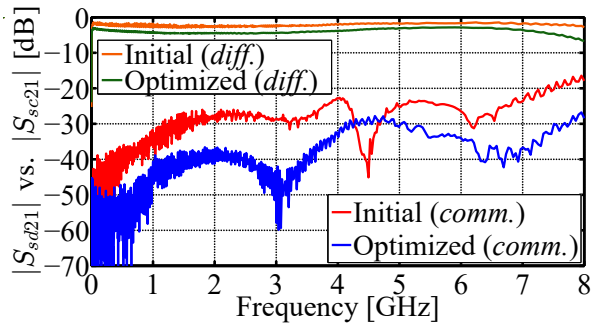
accurately describes the differential-mode signal measurements up to 4 GHz. The model accurately predicts the trend of the common-mode measurements, with a NRMSE of 0.004520, and an offset of 4.1 dB. As a result, the trend of the CMRR for the characterized VCSEL is accurately predicted, with a NRMSE of 0.008484, and an offset of 3.8 dB. The agreement of the modelled differential-mode signal transmission with the measured data is better than for the common-mode signal transmission. This is a result of the low level of the common-mode signal, and the fact that the higher-order effects that further degrade the common-mode signal, and thus the CMRR, are not included in the presented VCSEL circuit model.

The presented equivalent circuit model of the VCSEL can be used to estimate the impact of the asymmetry in the parasitics between the port-to-ground paths from the laser anode and the cathode, on the common-mode rejection ratio. The model covers the frequency bandwidth between 1 MHz and 4 GHz. The equivalent circuit model can be used for laser diode applications in EMC and ESD [87].

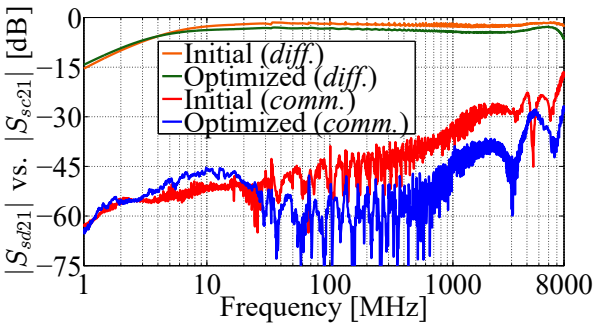
## 3.5 Optimized laser layout

The port-to-ground path of the laser diode is critical for achieving a high CMRR, as demonstrated by the analysis of the VCSEL equivalent circuit model presented in Section 3.4. The layout of the VCSEL characterization structure is optimized based on the results of this analysis. By reducing the parasitics between the VCSEL case and the PCB, and by controlling the impedance of the path from the laser case towards the ground, the CMRR of the laser is improved. The optimized layout of the VCSEL model #2 is characterized and compared to the initial VCSEL model #2 layout characterized in Section 3.3. The lasers are biased using the isolated power supply PoF bias module, shown in Fig. 3.3a. Three-port S-parameters of the optimized VCSEL model #2 characterization structure are measured and the mixed-mode S-parameters are calculated.

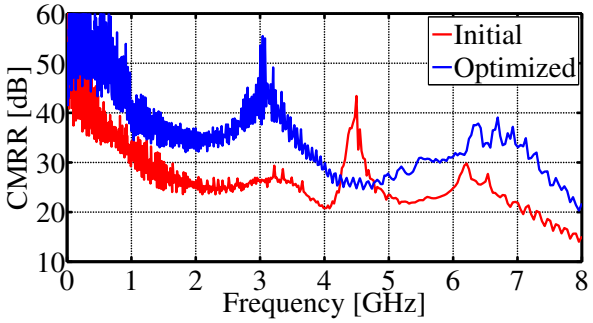
The mixed-mode S-parameter characteristics of the initial and the optimized VCSEL model #2 layout are compared in Fig. 3.39. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is similar for both lasers. The level of the differential-mode signal for the optimized VCSEL layout is around 1.5 dB lower than for the initial layout. The differential-mode characteristic of the optimized VCSEL layout drops off a bit above 7 GHz, but



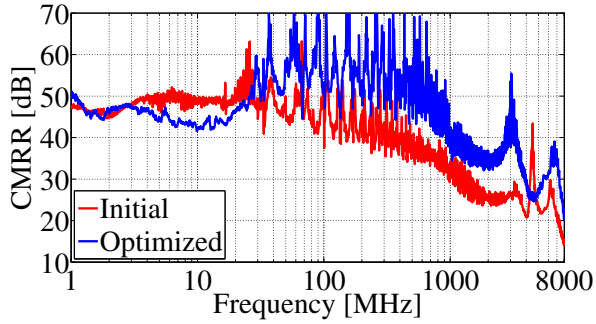

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 3.39:** Comparison of the measurements of the initial and the optimized VCSEL model #2 layout. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The lasers are biased using the isolated power supply (PoF bias) module.

remains within ±3 dB of the nominal value up to 7.9 GHz. While the general trend of the common-mode transmission coefficient $S_{sc21}$ is similar for both laser layouts, the common-mode signal level is significantly lower for the optimized laser layout, with the difference between the characteristics of around 10–15 dB.

Given the similar differential-mode characteristics and significantly better suppression of the common-mode signal for the optimized VCSEL layout, the CMRR of the laser with the optimized layout is significantly higher. The CMRR of the initial VCSEL layout is above 30 dB up to 1.2 GHz, above 25 dB up to 2.1 GHz, and above 20 dB up to 7.1 GHz. The CMRR of the optimized VCSEL layout is above 30 dB up to 3.9 GHz, above 25 dB up to 7.7 GHz, and above 20 dB in the entire frequency range. By optimizing the laser layout, the CMRR is increased by around 10–15 dB, allowing for significantly better performance of the electro-optical probe circuit to be achieved.

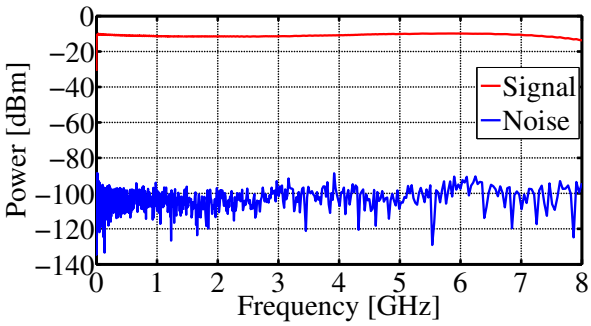
Additional performance improvements could be made by using VCSEL models with higher specified data rates. Such laser designs that are made for faster data rates, typically have better symmetry of the internal VCSEL structure and lower parasitics, leading to better performance with analog differential signals and a higher CMRR.

### 3.5.1 Signal-to-noise ratio

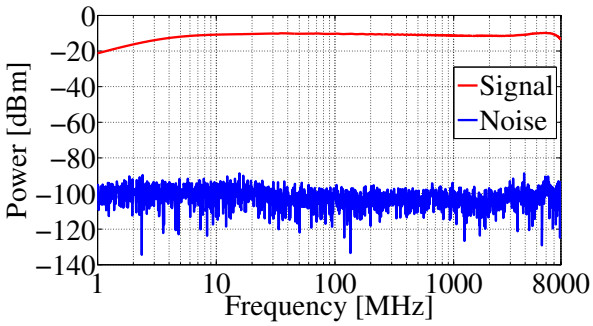
The signal-to-noise ratio (SNR) of the characterized optimized VCSEL model #2 layout is evaluated. The signal level, the noise level and the SNR characteristics of the VCSEL are shown in Fig. 3.40. The differential-mode signal level is around –10 dBm and remains relatively stable in almost the entire measurement frequency range. The differential-mode signal level is determined by the electro-optical signal conversion in the VCSEL, the attenuation of the signal in the optical transmission path, and the opto-electrical conversion of the signal in the photodetector. The drop in the signal level below 10 MHz is a result of the lower cutoff frequency of 2 MHz of the photodetector model [69] used to perform the measurements. The measured noise level is around –100 dBm. The signal and noise level are measured using a two-port VNA [68], with the output power level set to –7 dBm, the resolution bandwidth (RBW) filter set to 1 kHz, and 10 measurement averages being performed. The RBW filter and measurement averaging lower the effective noise level. The noise level is determined by the noise floor of the photodetector model used to perform the measurements. It does not depend on the level of the RF signal, nor the laser bias signal level. Environmental parameters like the ambient temperature can also impact the signal and noise level.

The signal-to-noise ratio is defined as the ratio of the signal level and the noise level shown in Fig. 3.40a. The maximum SNR that can be achieved is above 80 dB in most of the measurement frequency range. The SNR is limited at frequencies below 10 MHz due to the lower cutoff frequency of 2 MHz of the photodetector model [69] used to perform the measurements. Using

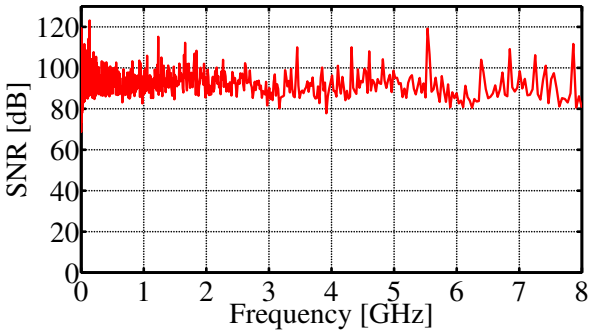
an RBW filter and averaging of multiple measurements lowers the effective noise level and improves the SNR. In the time domain measurements performed without averaging, the SNR of the VCSEL remains above 40 dB. The SNR of the VCSEL limits the SNR of the entire electro-optical measurement system. The goal is to attenuate the signal at the input of the probe circuit in such a way to get a constant differential-mode signal level at the input ports of the VCSEL. In this way, the maximum dynamic range of the measurement system is achieved.



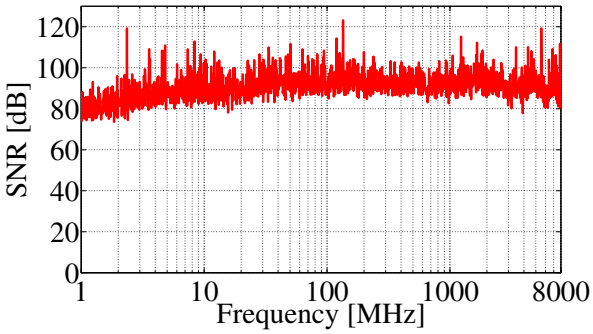

(a) Signal and noise level (linear frequency scale).




(b) Signal and noise level (log. frequency scale).




(c) Signal-to-noise ratio (linear frequency scale).




(d) Signal-to-noise ratio (log. frequency scale).

**Figure 3.40:** Measurements of the signal level, the noise level, and the signal-to-noise ratio (SNR) of the characterized optimized VCSEL model #2 layout.

A distinction needs to be made between the unwanted common-mode input signal, the photodetector noise level, and the noise level of the VNA used to characterize the electro-optical measurement system and its components. When characterizing the common-mode rejection ratio, differential-mode and common-mode stimulus is applied at the input of the device under test. The differential-mode signal represents the wanted component of the input signal, while the common-mode signal represents the unwanted component. The ratio between the wanted and the unwanted component of the input signal is the CMRR. The CMRR describes the ability of the device to suppress the unwanted common-mode component, while transmitting the wanted differential-mode component of the signal.

The signal-to-noise ratio represents the ratio between the maximum and the minimum wanted differential-mode signal level that can be applied at the input of the device, while still remaining above the noise level. The noise level is constant and it is dependent on the noise level of the photodetector model used. The minimum input signal level is determined by the noise level.

The maximum input signal level is dependent on the maximum signal amplitude that can be applied to the laser diode, while still continuing to operate in the linear region, as well as the attenuation of the signal between the probe input and the laser diode, in the case of the probe circuit. In general, the photodetector noise level does not present an issue when measuring the CMRR. Issues with measuring the CMRR can occur if the CMRR is higher than the SNR. In such a case, the common-mode signal level would be masked by the noise floor of the photodetector, and the measured CMRR would be equivalent to the SNR.

When characterizing the CMRR and the SNR using a VNA, the output power and the VNA noise level are the main limitations. The VNA noise level must be below the photodetector noise level, in order to be able to accurately measure the SNR. When measuring the SNR, the VNA output power level should be equivalent to the maximum allowed input signal level of the device under test. Given that the maximum output power of a VNA is typically around 0-10 dBm [66–68], this can be an issue when characterizing devices that have a relatively high maximum input signal level. For that reason, the SNR is measured on the laser which has a relatively low maximum input signal level, and not on the probe circuit, which has a relatively high maximum input signal level. When measuring the CMRR, if the VNA output power is too low, the common-mode signal which is typically lower than the differential-mode signal, can fall below the photodetector noise level, and in extreme cases below the VNA noise level. In both cases, the measured CMRR would be lower than the actual CMRR. This can be an issue for devices with a high maximum input signal level and a high CMRR, such as probe circuits with a high attenuation ratio. An amplifier can be used to increase the VNA output power, however this complicates the measurement setup and the de-embedding process. There are also strict requirements on the broadband linear response of the amplifier used to perform the measurements. Given that the SNR is typically higher than the CMRR, it requires a higher dynamic range of the VNA in order to be measured accurately.

## 3.6 Summary

The laser diode is used to convert the measured RF signal into an optical signal. In this way, immunity of the electro-optical measurement system to electromagnetic interference is improved. A vertical-cavity surface-emitting laser is used, because of its wide bandwidth, small size, light weight and low cost. The laser is differentially driven, and the input RF signal is applied between the anode and the cathode. The bias point of the VCSEL is set in the center of the linear region, in order for the laser to be able to work with maximum input voltage amplitudes. An isolated power-over-fiber power supply bias module and a non-isolated power supply bias module, which is directly connected to a voltage source, are characterized by measuring the differential-mode input impedance. By using the isolated power supply, complete galvanic isolation of the electro-optical measurement system is achieved, and the noise coming from the power supply is suppressed.

A differential bias circuit is designed and used to set the operating point of the laser diode. Multiple bias circuit iterations are designed and characterized by performing EM simulations, and measuring the differential-mode input impedance. The optimum performance is achieved by using a series combination of ferrite beads and resistors at the input of the bias circuit. In this way, the benefits of both component types are utilized in order to achieve a high input impedance over a wide frequency range. Additionally, the parasitics are reduced by creating slots in the ground plane beneath the passive components, and by reducing the solder pad size.

Lasers from multiple manufactures and in different package types are characterized. The differential-mode and common-mode signal transmission, as well as the CMRR of the lasers is measured. By using the through-hole VCSEL package, the best combination of CMRR, mechanical robustness and repeatability of laser characteristics is achieved. Power supply isolation does not have a significant impact on the performance of the characterized VCSEL. A differential equivalent circuit model of the VCSEL is extracted, and is used to model both the differential-mode and the common-mode signal transmission, as well as the CMRR. The impact of the parasitic asymmetry on the CMRR of the characterized VCSEL is shown. The VCSEL layout is optimized and the CMRR is improved. A CMRR of 30 dB up to 3.9 GHz is achieved. The characterized VCSEL is used in the electro-optical probe circuit. The signal-to-noise ratio of the laser is dependent on the signal-to-noise ratio of the photodetector used to perform the measurements, and it limits the signal-to-noise of the electro-optical probe circuit.

# Chapter 4

# Probe circuit design and characterization

## 4.1 Probe circuit development

The probe circuit is the functional circuit of the electro-optical differential voltage probe shown in Fig. 1.2. The probe circuit is divided into three main parts: the attenuator, the laser diode, and the bias circuit, as shown in Fig. 4.1. The attenuator circuit lowers the input signal level in order not to overdrive the laser diode. The laser diode converts the measured signal from the electrical into the optical domain. The bias circuit sets the operating point of the laser diode. The developments made to the attenuator circuit design in Section 2.3, the laser diode layout in Sections 3.3–3.5, and the bias circuit layout in Section 3.2 are implemented in the probe circuit design. The results of characterizing the individual parts of the probe circuit are verified by combining them into a probe circuit, and evaluating the performance of the probe circuit. The performance of different probe circuit layouts is analyzed and compared. Probe circuits with different attenuation ratios are characterized. The repeatability of the probe circuit characteristics between samples is analyzed.

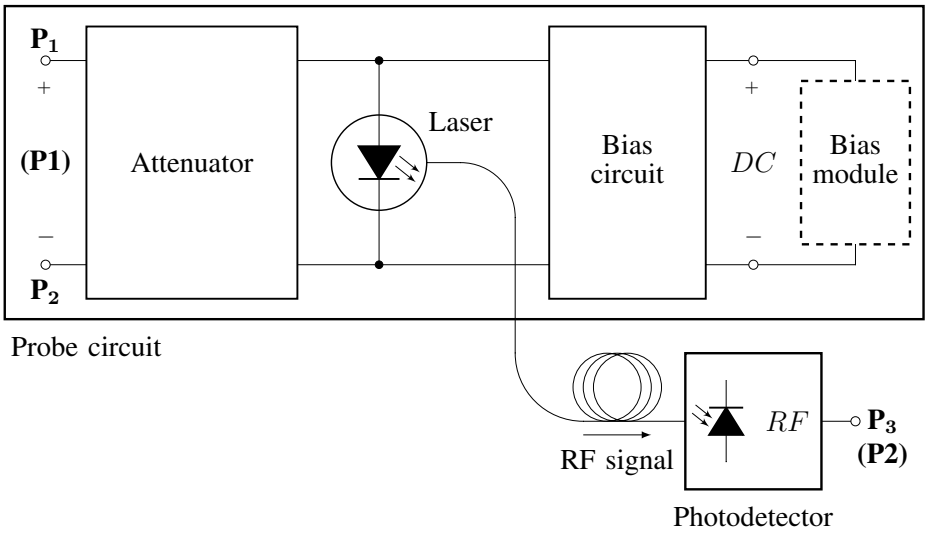



**Figure 4.1:** Probe circuit characterization setup schematic.

The probe circuit layout is optimized and implemented on two voltage probes. One probe is designed as a differential connectorized probe with a well-defined ground connection. The other probe is designed as a fully floating differential wafer probe. Despite the difference in the fixture and ground connection, both probes are realized in a differential configuration and the laser is driven differentially. The different fixture types and ground connections are used in order to evaluate the impact of the ground connection on the probe performance. The isolated power supply PoF bias module is used, as well as the non-isolated power supply DC bias module. The performance of the probes is compared when using each type of power supply, in order to evaluate the impact of the noise coming from the power supply and noise coupling on the electrical wires. Based on the mixed-mode S-parameter analysis, the differential-mode and common-mode characteristics of the probes are compared. The CMRR is a key metric

of performance for differential probes. Differential-mode and common-mode input impedance characterization of the probes is performed. Simple lumped element circuits are used to model the differential-mode and common-mode input impedance, and extract the values of the parasitics. A physical interpretation of the circuit model elements is given.

This chapter is structured as follows. Section 4.1 presents the development of the probe circuit design, from the initial design implemented on the wafer probe, to the implementation of the improvements made to the circuit elements on the probe circuit characterization structure. Section 4.2 describes the optimized probe circuit layout which is implemented on two probes with different ground connection types, which are characterized by measuring the S-parameters. In Section 4.3 the input impedance characteristics of the two probes are analyzed and modelled. Section 4.4 analyzes the impact of impedance matching between the elements of the probe circuit and the circuit symmetry on the common-mode rejection ratio that can be achieved. In Section 4.5 time domain measurements are performed using the developed electro-optical probe. The summary is given in Section 4.6.

This chapter is based on the following papers:

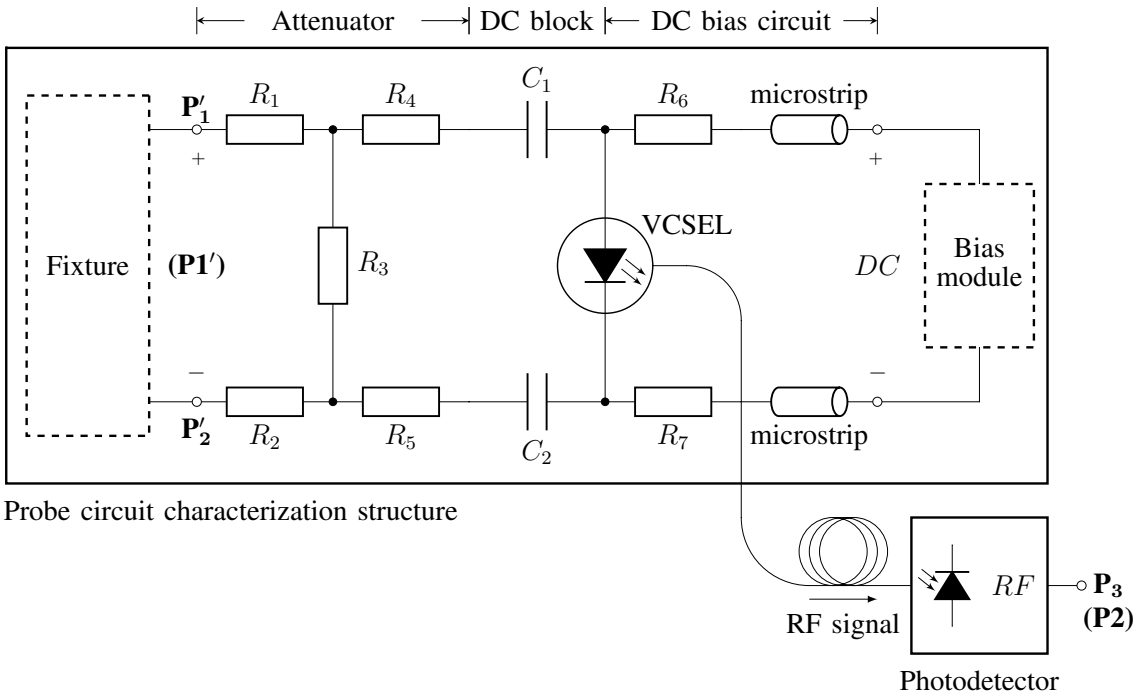
[85] Štimac, H., Gillon, R., Barić, A., "Common-mode rejection ratio characterisation of a broadband electro-optical differential ESD voltage probe", Electronics Letters, Vol. 55, No. 19, Sep 2019, pp. 1047-1049.

[128] Štimac, H., Bačmaga, J., Gillon, R., Barić, A., "Design and Characterization of Differential Electro-Optical Voltage Probes Operating in GHz Range: Analysis of Ground Connection and Power Supply Isolation", submitted to IEEE Transactions on Electromagnetic Compatibility, 2020.

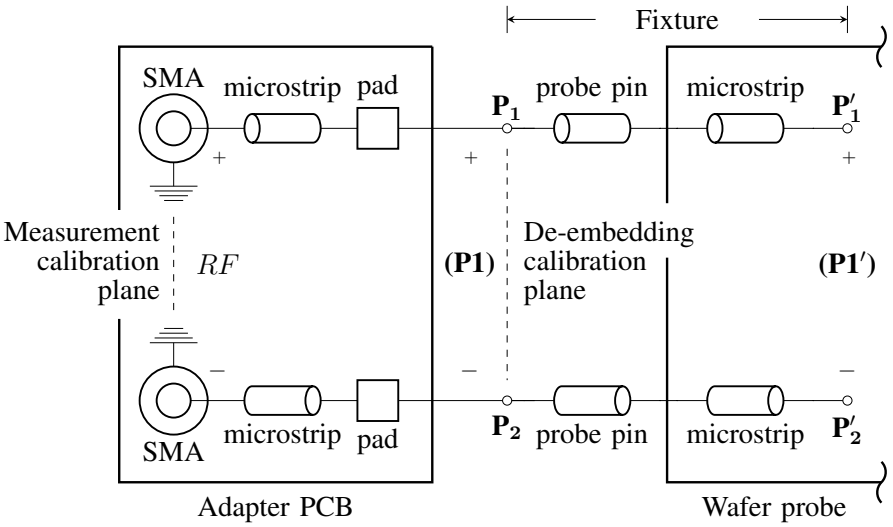
### 4.1.1 Initial wafer probe design

The initial designs of the attenuator circuit, the laser diode and the bias circuit are combined into a probe circuit and implemented on the initial wafer probe design shown in Fig. 4.2a. The attenuator #1 circuit design shown in Fig. 2.25a is used. The attenuator circuit is characterized and discussed in Section 2.3. The attenuator circuit is implemented without the ground plane, in order to reduce the parasitics and increase the CMRR. The VCSEL model #1 with the flexible PCB shown in Fig. 3.1a is used. The VCSEL model #1 is characterized in Section 3.3. The laser is biased using the bias circuit #1 layout shown in Fig. 3.9. The bias circuit design is characterized and discussed in Section 3.2.3.

The probe circuit is implemented as a fully floating two-pin differential wafer probe. The probe circuit is realized on a PCB with a probe fixture that consists of two 50-Ohm microstrip traces terminated with wafer probe pins with a 1 mm pitch, as shown in Fig. 4.2b. To allow simple characterization of the probe, an additional adapter PCB is used as a transition between




(a) Initial wafer probe circuit schematic.



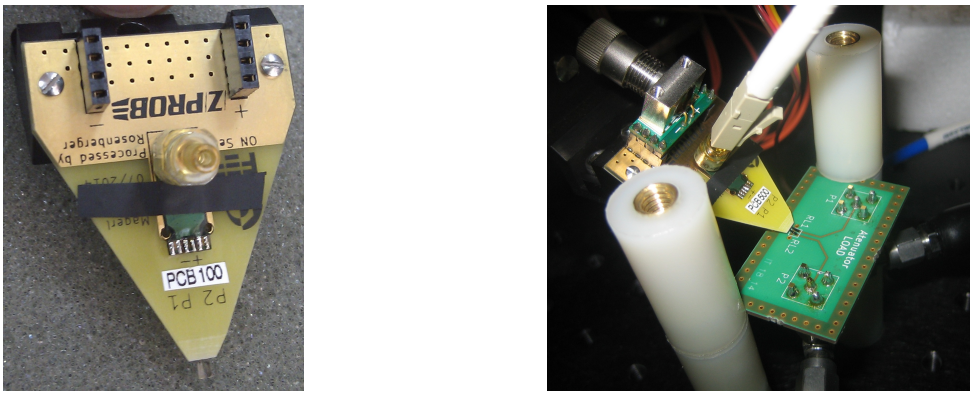

(b) Initial wafer probe fixture schematic.

**Figure 4.2:** Initial wafer probe schematic.

the measurement setup and the wafer probe. The adapter PCB has two input SMA connectors used for connecting the measurement equipment. These connectors allow for simple characterization and also provide a good ground connection between the measurement setup and the ground plane on the adapter PCB. Each SMA connector is connected to a pad using a 50-Ohm microstrip transmission line. The pads on the adapter PCB are used to land the wafer probe and achieve a differential connection between the measurement equipment and the probe circuit. There is no connection between the ground plane of the adapter PCB and the ground plane of the wafer probe, which means that the ground plane of the wafer probe is floating, and there is

no ground reference. The initial wafer probe PCB design is shown in Fig. 4.3a, while the probe characterization setup with the adapter PCB is shown in Fig. 4.3b.

The wafer probe is realized on the |Z| Probe® [14] PCB layout using the PCB stack-up shown in Fig. 1.3. The fixture traces, the attenuator circuit, and the bias circuit are realized on the Top layer of the PCB. The input SMA connectors, the laser, and the sockets for connecting the bias module are placed on the Bottom layer. In this way, the ground plane on the Inner layer of the PCB separates the top side of the probe where the circuits are realized and the traces are routed, from the bottom side of the PCB where all the cables are connected.




(a) Initial wafer probe design. (b) Initial wafer probe characterization setup.

**Figure 4.3:** Initial wafer probe PCB design and characterization setup.

The initial wafer probe design is implemented on two probes with different attenuation ratios. The list of components used in the attenuator circuit and the nominal performance parameters of the two probes are listed in Table 4.1. The attenuation of the probe approximately corresponds to the ratio of the input voltage and the output voltage of the attenuator circuit terminated with the VCSEL, as well as the inverse value of the differential-mode transmission coefficient $S_{sd21}$. The maximum differential-mode input voltage amplitude $V_{d1,max}$, and the nominal differential-mode input impedance $Z_{d1}$, at the balanced port (P1) are also listed. The value of the differential-mode transmission coefficient varies slightly between different samples of the same probe circuit. The exact value of the differential-mode transmission coefficient is dependent on the impedance of the probe fixture, the impedance of the components used in the

**Table 4.1:** Initial wafer probe design configurations.

| Configuration | $R_1$, $R_2$, $R_4$, $R_5$ | $R_3$ | Attenuation | $V_{d1,max}$ | $Z_{d1}$ |
|---|---|---|---|---|---|
| 100R | 100 Ω | 100 Ω | 11 (21 dB) | 2.2 V | 275 Ω |
| 1000R | 1000 Ω | 100 Ω | 500 (54 dB) | 100 V | 2095 Ω |

attenuator circuit which varies with their tolerance, the characteristics of the VCSEL sample used, as well as the optical connection and the attenuation in the optical signal path.

**Measurement procedure**

The initial wafer probe is characterized as a device with three physical ports, as shown in Fig. 4.2. The input physical ports $P_1$ and $P_2$ are connected through the attenuator circuit to the VCSEL anode and cathode, respectively. The output port $P_3$ is the photodetector output RF port. The characteristics of the probe are evaluated including the impact of the entire electro-optical signal path. This path includes the electro-optical signal conversion in the VCSEL, the transition between the VCSEL and the optical fiber, the optical signal propagation through the fiber, the transition between the fiber and the photodetector, the opto-electrical conversion of the signal in the photodetector, and the electrical signal path in the photodetector. The low frequency cutoff and the noise level of the photodetector model [69] used to perform the measurements impact the lower cutoff frequency and signal-to-noise ratio of the electro-optical measurement system. The measurement results close to the lower cutoff frequency of the photodetector, where the common-mode signal level is typically very low, have a higher measurement uncertainty, as discussed in Section 2.1.3. Because of that, the probe characteristics are typically compared for frequencies above 100 MHz, for the different probe circuit layouts presented in this thesis.

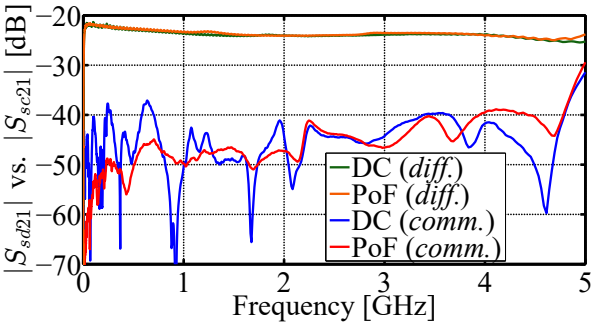
A three-port S-parameter measurement of the probe is performed using a vector network analyzer. A dual-source four-port VNA [67] is used and the probe is characterized in the frequency range from 1 MHz to 8 GHz. The VNA output power is set to 0 dBm in order to achieve the maximum dynamic range. Through-open-short-match (TOSM) calibration is used to calibrate the VNA [67]. A series of calibration structures are measured in order to extract the characteristics of the adapter PCB used to characterize the wafer probe. The parameters of the microstrip feed lines are extracted and electromagnetic simulations of the fixture are performed using a commercially available EM solver based on the method of moments [93]. The circuit model shown in Fig. 2.19 and presented in [82] is used to model the SMA connectors. The transmission line and connector model parameters are optimized to fit the modelled calibration structures to the measurement results. The impact of the adapter PCB consisting of two SMA connectors, microstrip feed lines and probe landing pads is de-embedded. The calibration reference plane is shifted to the input of the wafer pins, as shown in Fig. 4.2b. The de-embedded wafer probe measurement results include the impact of the wafer probe fixture, consisting of the wafer pins and input microstrip traces, in addition to the probe circuit characteristics.

In order to evaluate the differential-mode and common-mode performance of the probe, using mixed-mode S-parameters is more suitable than standard single-ended S-parameters [28]. The two physical input ports $P_1$ and $P_2$ form the logical balanced (differential) input port (P1), as shown in Fig. 4.2. The output single-ended physical port $P_3$ forms the logical single-ended

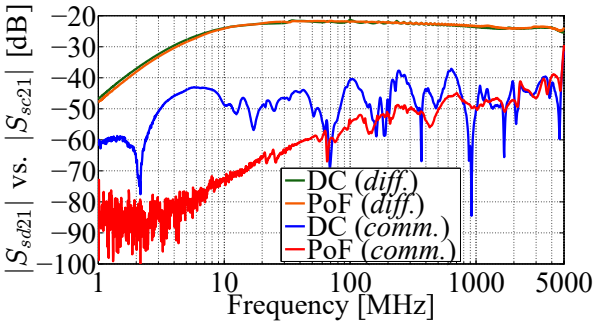
output port (P2). The mixed-mode S-parameters are calculated from the single-ended S-parameters using (2.49)–(2.57), as described in Section 2.1.1. The most important mixed-mode parameters related to the differential-mode and common-mode performance of the probes are the differential-mode signal transmission coefficient $S_{sd21}$, and the common-mode signal transmission coefficient $S_{sc21}$. The ratio between the wanted differential-mode signal transmission and the unwanted common-mode signal transmission is defined as the common-mode rejection ratio (CMRR) and is calculated using (2.58).

### Measurement results

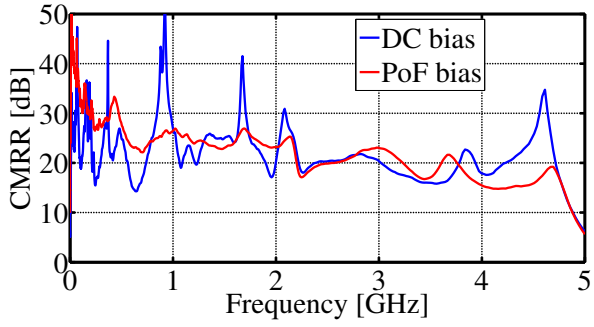
The mixed-mode S-parameter measurement results of the initial wafer probe with the 100R attenuator configuration are shown in Fig. 4.4. The probe is characterized when using the isolated power supply PoF bias module (Fig. 3.3a) and the non-isolated power supply DC bias module (Fig. 3.3b). The general trend of the differential-mode transmission coefficient $S_{sd21}$ is very similar for both power supply types. There is slightly less ringing for the measurement using the isolated power supply. The differential-mode signal level is stable and remains within $\pm$3 dB of the nominal value of approximately –21 dB up to 4.4 GHz.



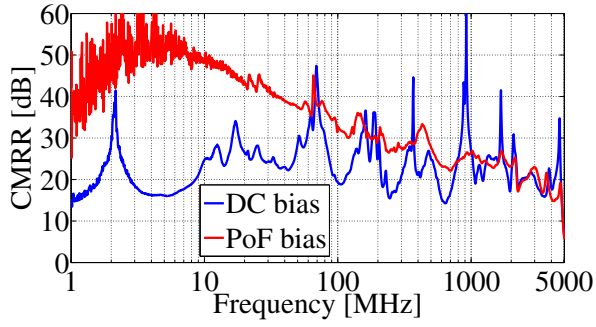

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

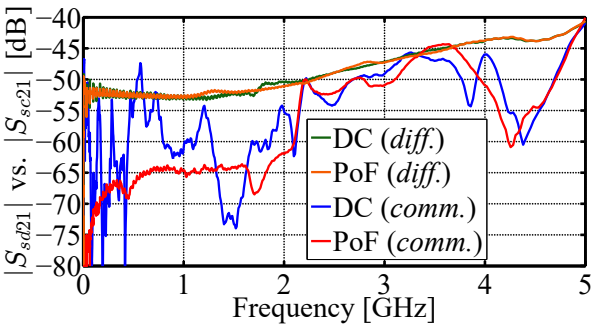
**Figure 4.4:** Comparison of the measurements of the initial wafer probe design 100R attenuator configuration biased using the isolated power supply (PoF bias) module and the non-isolated power supply (DC bias) module. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

The common-mode transmission coefficient $S_{sc21}$ measured when using the isolated power supply increases steadily with frequency. The increase in the common-mode signal level is significantly faster in the lower frequency range up to 100 MHz, as opposed to the higher frequency range, where there is a significant number of resonances. Significant noise is present in the common-mode characteristic measured when using the non-isolated power supply, in the frequency range up to 2 GHz, and up to 500 MHz in particular. The impact of the noise coming from the power supply is observable in the form of a large number of resonances and antiresonances in the common-mode characteristic.

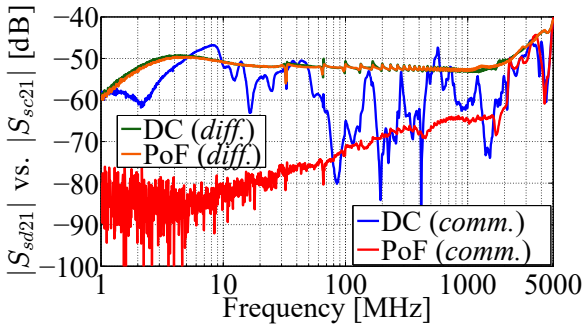
The CMRR of the probe when using the isolated power supply drops steadily with frequency, as a result of the increase in the common-mode signal level. The CMRR is above 30 dB up to 200 MHz, and above 20 dB up to 2.2 GHz. A large number of resonances and antiresonances are present in the CMRR characteristic when using the non-isolated power supply, in the frequency range up to 2 GHz, as a results of the noise coming from the power supply. In the frequency range up to 2.3 GHz, the CMRR level when using the non-isolated power supply is around 5–10 dB lower than when using the isolated power supply. At higher frequencies, the general trend of the two characteristics is similar.

The mixed-mode S-parameter measurement results of the initial wafer probe with the 1000R attenuator configuration are shown in Fig. 4.5. The probe is characterized when using the isolated power supply PoF bias module and the non-isolated power supply DC bias module. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is similar when using both power supply types, although the characteristic is a bit smoother when using the isolated power supply. The stable differential-mode signal level at lower frequencies is around 1.5 dB higher than the nominal value of –54 dB, and remains within $\pm$3 dB of that value up to 2.4 GHz. The attenuation of the probe decreases with frequency as a result of the surface-mount component parasitics which effectively lower the impedance of the components. Additionally, the lack of a ground plane under the attenuator affects the stability of the differential-mode signal over a wide frequency range, as demonstrated in Section 2.3.

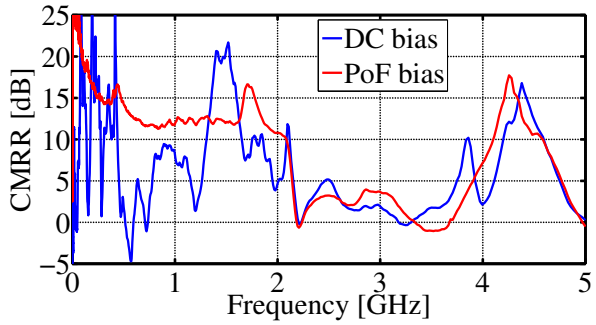
The common-mode transmission coefficient $S_{sc21}$ level of the measurement using the isolated power supply is steadily increasing with frequency up to 2.1 GHz. At this frequency there is a 10 dB increase in the common-mode signal value, and the common and differential signal levels become comparable. There is a wide resonance is the common-mode signal characteristic around 4.3 GHz. When using the non-isolated power supply, significant noise is present in the common-mode transmission coefficient, particularly in the frequency range up to 2.1 GHz. This is a result of the noise coming from the power supply, and it is manifested in the form of a large number of resonances and antiresonances in the common-mode characteristic. At frequencies above 2.1 GHz, the general trend of the common-mode characteristic with the non-isolated power supply is similar to the case when using the isolated power supply.



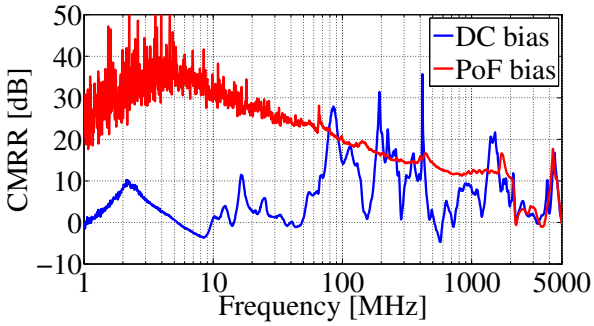

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.5:** Comparison of the measurements of the initial wafer probe design 1000R attenuator configuration biased using the isolated power supply (PoF bias) module and the non-isolated power supply (DC bias) module. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

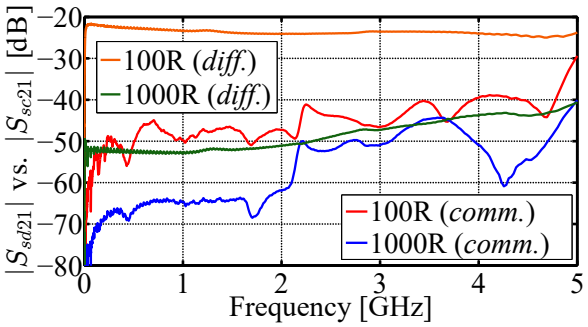
The CMRR of the probe measurement using the isolated power supply drops steadily from 30 dB at 10 MHz, to 20 dB at 100 MHz, and the value remains above 10 dB up to 2.1 GHz, after which the it drops close to zero. There is an increase in the CMRR value around 4.3 GHz, due to the resonance in the common-mode characteristic. In the CMRR characteristic measured using the non-isolated power supply there is a large number of resonances and antiresonances in the frequency range up to 2.1 GHz, as a results of the noise in the common-mode characteristic. At higher frequencies, the trend of the CMRR characteristic is similar for both power supply types. The probe is practically not usable with the non-isolated power supply biasing, as the CMRR value is very low and unstable in the entire measurement frequency range. For both the 100R and the 1000R probe attenuator configuration, it is observed that the impact of the power supply isolation is very pronounced in the common-mode transmission coefficient and translates into the CMRR. Regardless of the probe attenuation ratio, using the isolated power supply is necessary in order to obtain a higher and more stable CMRR characteristic.

The characteristics of the two initial wafer probe configurations with the different attenuation ratios, listed in Table 4.1, are compared in Fig. 4.6. The probes are biased using the isolated power supply PoF bias module. The differential-mode transmission coefficient $S_{sd21}$ of the 100R probe configuration is stable and remains within $\pm 3$ dB of the nominal value in

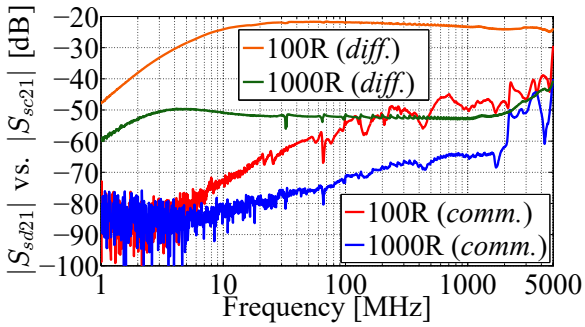
almost the entire measurement frequency range. The nominal differential-mode signal value of the 1000R probe configuration is around 30 dB lower than for the 100R probe. The differential signal level of the 1000R probe is less stable and increases by more than 10 dB in the frequency range up to 5 GHz, with the difference between the two probes dropping to below 20 dB. The difference in the stability of the differential-mode signal between the two probes is a result of the different resistors used in the attenuator circuit. The 1000 Ω resistors used in the 1000R probe attenuator circuit have a significant drop in impedance at higher frequencies, as opposed to the 100 Ω resistors, as shown in Fig. 2.16a. The 1000R probe, which uses the attenuator circuit with the higher impedance, also has a higher lower cutoff frequency.

The offset between the common-mode transmission coefficient $S_{sc21}$ of the two probes is around 15 dB in the lower frequency range, and remains relatively stable up to 2.2 GHz, after which the difference is between 5 dB and 10 dB up to 3.7 GHz. At higher frequencies, the difference between the common-mode characteristics of the two probes increases because of the resonance in the common-mode characteristic of the 1000R probe around 4.3 GHz.

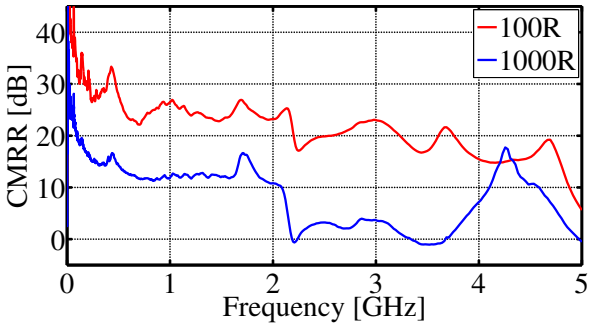
It is observed that the differential-mode signal is attenuated more than the common-mode signal of the 1000R wafer probe, compared to the 100R probe. This results in a significantly higher CMRR level of the 100R probe, compared to the 1000R probe, with the higher nominal



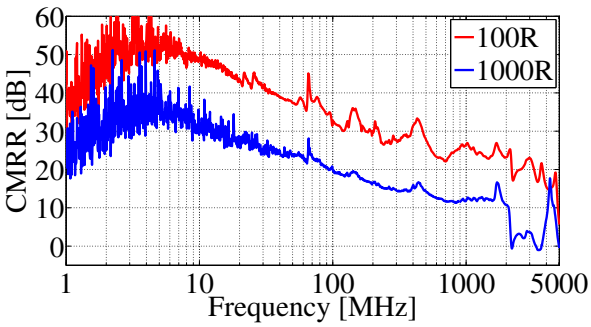

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.6:** Comparison of the measurements of the initial wafer probe design 100R attenuator configuration and the 1000R attenuator configuration. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the isolated power supply (PoF bias) module.

attenuation. Both probes display a similar trend of a steadily dropping CMRR in the frequency range from 10 MHz up to 2.1 GHz, with the difference between the characteristics of around 10–15 dB. The difference between the two characteristics increases to around 20 dB in the frequency range from 2.3 GHz to 3.7 GHz. There is a fast decrease in CMRR of both probes at high frequencies above 4.7 GHz.

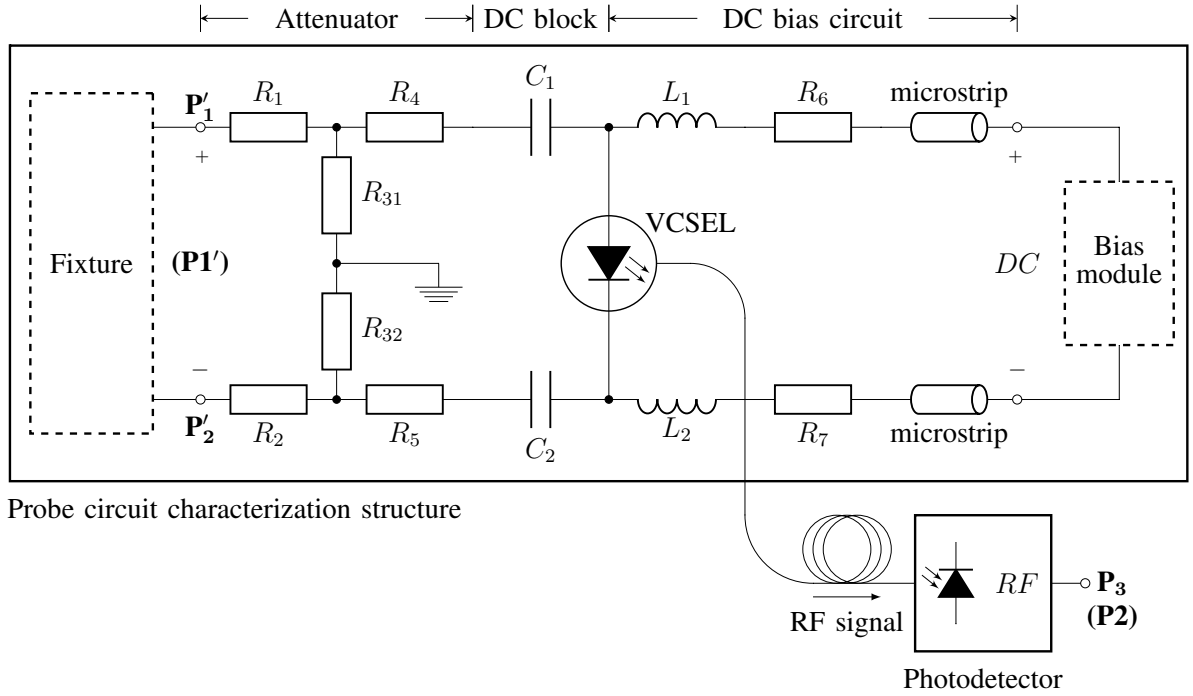
By comparing the two wafer probes with the different attenuation ratios, it is shown that the differential-mode signal is more stable over a wide frequency range for the probe with the lower attenuation. This a result of using resistors with a lower resistance, which have a more stable frequency impedance profile. In general, the differential-mode signal is attenuated more than the common-mode signal. It is difficult to attenuate the common-mode signal by the same amount as the differential-mode signal, given that there are contributions to the common-mode signal that are common for both probes, and which increase the common-mode signal level regardless of the attenuation ratio. The general trend of the CMRR characteristic is similar for both wafer probes, but a significantly higher CMRR is achieved for the probe with the lower attenuation ratio. Both wafer probes display a similar drop in CMRR at high frequencies around 4.5 GHz, which is not dependent on the probe attenuation ratio, and is likely a result of the probe circuit layout. Using the isolated power supply results in a higher and more stable CMRR, with significantly less noise in the characteristic.

### 4.1.2 Probe circuit

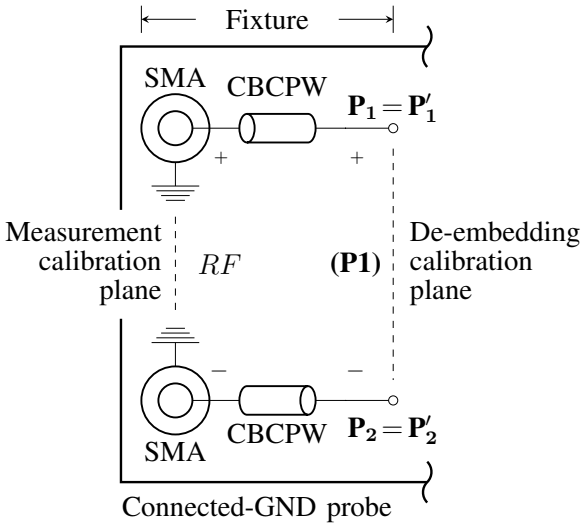
Based on the characterization of the initial wafer probe design, individual parts of the probe circuit are analyzed separately. The design of each part of the probe circuit is optimized based on the simulation and measurement results. Different attenuator circuit designs are evaluated and compared in Section 2.3. The attenuator #3 circuit design, shown in Fig. 2.25c, is selected because of the most stable differential-mode response, and best suppression of the common-mode signal compared to the other designs. A ground plane is used under the attenuator structure in order to make it less susceptible to electromagnetic interference and noise coupling. Different laser models are evaluated and compared in Section 3.3. The VCSEL model #2 in the through-hole package, shown in Fig. 3.1b, is selected because of the highest and most stable broadband CMRR response, as well as improved mechanical robustness and repeatability of the RF characteristics, compared to the VCSEL model #1 in the package with the flexible PCB. Different laser bias circuit layouts are evaluated and compared in Section 3.2. The bias circuit #4 layout realized using ferrite beads, shown in Fig. 3.21, is selected because of the highest input impedance, and the highest CMRR of the laser that can be achieved when using it, compared to the other layouts. These elements of the probe circuit design are combined and implemented in the probe circuit characterization structure shown in Fig. 4.7a.

The probe circuit characterization structure is implemented on a PCB with the stack-up

shown in Fig. 1.3. The circuits and the traces realized on the Top layer of the PCB are separated from the RF, DC and optical connections on the Bottom layer of the PCB, using the ground plane on the Inner layer. The fixture of the probe circuit characterization structure is realized using two SMA connectors and 50-Ohm CBCPW feed lines, as shown in Fig. 4.7b. The SMA connectors allow for simple characterization of the probe circuit and provide a good ground connection between the measurement setup and the ground plane of the probe circuit characterization structure. CBCPW transmission lines are used in order to reduce the coupling between the two input traces [81].




(a) Probe circuit schematic used in the probe circuit characterization structure, the connected-ground probe and the floating-ground probe.




(b) Fixture of the probe circuit characterization structure and the connected-ground probe.

**Figure 4.7:** Probe circuit characterization structure and the connected-ground probe schematic.

### Probe circuit attenuation ratio

The probe circuit design is implemented on two characterization structures with different attenuation ratios. The list of components used in the attenuator circuit and the nominal performance parameters of the two probe circuits are listed in Table 4.2. The attenuation of the probe circuit approximately corresponds to the ratio of the input voltage and the output voltage of the attenuator circuit terminated with the VCSEL, as well as the inverse value of the differential-mode transmission coefficient $S_{sd21}$. The maximum differential-mode input voltage amplitude $V_{d1,max}$, the nominal differential-mode input impedance $Z_{d1}$, and the nominal common-mode input impedance $Z_{c1}$, at the balanced port (P1) are also listed.

**Table 4.2:** Probe circuit design configurations.

| Configuration | $R_1$, $R_2$, $R_4$, $R_5$ | $R_{31}$, $R_{32}$ | Attenuation | $V_{d1,max}$ | $Z_{d1}$ | $Z_{c1}$ |
|---|---|---|---|---|---|---|
| 500R | 500 Ω | 50 Ω | 125 (42 dB) | 25 V | 1092 Ω | 275 Ω |
| 1000R | 1000 Ω | 50 Ω | 500 (54 dB) | 100 V | 2095 Ω | 525 Ω |

Three-port S-parameters of the two probe circuit characterization structures are measured. The measurements are performed using a two-port VNA [68], in the frequency range from 1 MHz to 8 GHz. Measuring three-port S-parameters using a two-port VNA requires a series of three measurements to be performed, each for a combination of two ports: $P_1$ and $P_2$, $P_1$ and $P_3$, $P_2$ and $P_3$, as described in Section 2.1.2. The remaining port is terminated with a matched load. The two-port measurement results are combined into a three-by-three S-parameter matrix using the technique described in [30, 50].

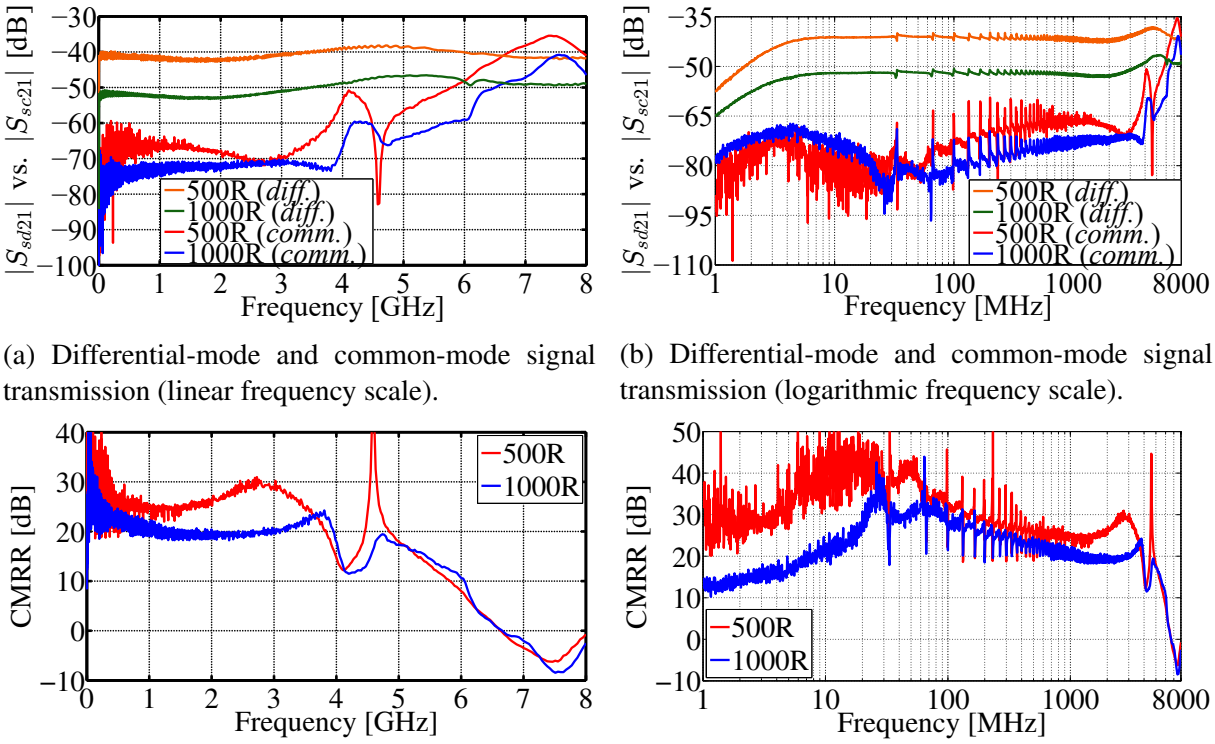
A series of calibration structures are measured in order to extract the characteristics of the probe circuit fixture. The impact of the fixture consisting of two SMA connectors and CBCPW feed lines is de-embedded from the measurement results. The calibration reference plane is shifted to the input of the probe circuit as shown in Fig. 4.7b. The de-embedded probe circuit measurement results include only the probe circuit characteristics.

Mixed-mode S-parameters are used to evaluate the performance of the characterized probe circuits. The two input physical ports $P_1$ and $P_2$ form the logical balanced input port (P1), and the output single-ended physical port $P_3$ forms the logical single-ended output port (P2) for the mixed-mode analysis, as shown in Fig. 4.7. The three-port standard S-parameters are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58).

The mixed-mode S-parameter measurement results of the two probe circuits with the different attenuation ratios, listed in Table 4.2, are compared in Fig. 4.8. The probe circuits are biased using the isolated power supply PoF bias module, shown in Fig. 3.3a. The level of the differ-

ential-mode transmission coefficient $S_{sd21}$ for both probe circuits, in the lower frequency range, is close to their respective nominal values. The difference in the differential signal levels is around 10–12 dB, corresponding to the difference between the nominal attenuation ratios. The attenuation of both probe circuits decreases above 2.5 GHz. The differential-mode transmission coefficient of the 500R probe circuit is within ±3 dB of the nominal value up to 4.2 GHz, with the lowest attenuation at 4.7 GHz. The differential-mode transmission coefficient of the 1000R probe circuit is within ±3 dB of the nominal value up to 3.8 GHz, with the lowest attenuation at 5.4 GHz. The differential-mode signal level of the 1000R probe circuit changes more significantly with frequency, and the difference between the two differential-mode characteristics is reduced to around 7 dB at 8 GHz.

The attenuation level of the probe circuits decreases with frequency as a result of the parasitics, which effectively lower the impedance of the attenuator circuit. This effect is more pronounced for the 1000 Ω resistors used in the 1000R probe circuit, than for the 500 Ω resistors used in the 500R probe circuit, due to their higher nominal resistance, as shown in Fig. 2.16a. This results in the difference between the two differential signal levels decreasing with frequency. Secondary parasitic effects cause a gradual drop in the differential signal at frequencies above 5–6 GHz. The 1000R probe circuit, with the higher attenuation ratio, also has the higher




(a) Differential-mode and common-mode signal transmission (linear frequency scale).

(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).

(c) Common-mode rejection ratio (lin. frequency).

(d) Common-mode rejection ratio (log. frequency).

**Figure 4.8:** Comparison of the measurements of the probe circuit 500R attenuator configuration and the 1000R attenuator configuration. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probe circuits are biased using the isolated power supply (PoF bias) module.

lower cutoff frequency, as was the case for the comparison of the two initial wafer probe design configurations with the different attenuation ratios.

The difference between the common-mode transmission coefficient $S_{sc21}$ of the two probe circuits varies between 5–10 dB, with the value being higher for the 500R probe circuit, with the lower nominal attenuation. The common-mode signal level is relatively stable for the 1000R probe circuit up 3.9 GHz. The common-mode signal level of the 500R probe circuit increases up to 1.2 GHz, after which it drops by around 5 dB to the local minimum at 2.7 GHz, and continues to increase again. Both probe circuits have a peak around 4.1 GHz, followed by a resonance which is more pronounced for the 500R probe circuit. For frequencies above 4.8 GHz, the common-mode signal level increases steadily for both probe circuits following a similar trend, and exceeds the differential-mode signal level above 6.7 GHz.

The CMRR level of the 1000R probe is around 20 dB in the frequency range up to 3.7 dB, while the CMRR level of the 500R probe varies between 25 dB and 30 dB in the same frequency range. At frequencies above 3.7 dB, the CMRR characteristics of both probe circuits follow a similar trend and have a very similar value. Both probe circuits have a resonance in the CMRR characteristic around 4.1 GHz, followed by an antiresonance around 4.6 GHz, after which the CMRR drops steadily to below 0 dB.

Similar to the characterization of the initial wafer probe design with the different attenuation ratios, it is observed that the differential-mode signal is attenuated more than the common-mode signal. This demonstrates that there is a common contribution to the common-mode signal level, which is the same for both probe circuits, and is independent of the probe circuit attenuation ratio. As a result, the probe circuit with the lower nominal attenuation ratio has the higher CMRR value. In the case of the two characterized probe circuits, the difference is around 5–10 dB. It is also observed that the differential-mode signal is more stable for the attenuator circuit design realized using resistors with the lower nominal resistance. As with the initial wafer probe design, the CMRR of both probe circuits decreases steadily for frequencies above 4.6 GHz. This indicates that the high frequency increase in the common-mode signal level is linked to the probe circuit layout, and is independent of the attenuation ratio used.

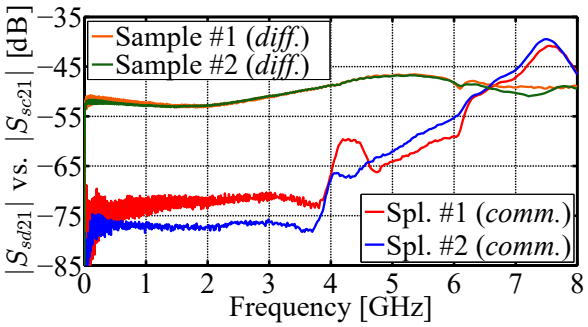
### Probe circuit sample repeatability

Two samples of the probe circuit with the 1000R attenuator configuration are assembled and characterized. Components on the sample #1 are soldered using a soldering iron, while the surface-mount components on the sample #2 are soldered using hot air soldering. The probe circuits are biased using the isolated power supply PoF bias module. The mixed-mode S-parameter measurement results of the two probe circuits are compared in Fig. 4.9. The differential-mode transmission coefficient $S_{sd21}$ characteristics of both probe circuit samples are very similar in almost the entire frequency range. The differential-mode signal level at lower fre-

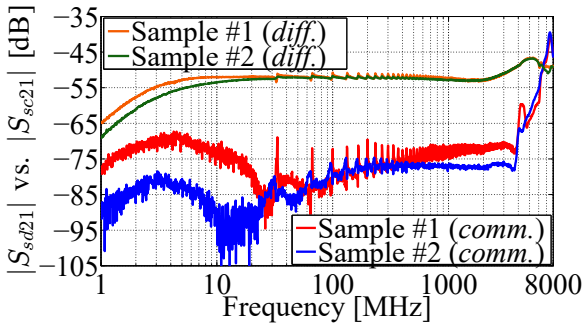
quencies corresponds to the nominal attenuation value of –54 dB. The probe circuit sample #1 has a slightly lower lower cutoff frequency and is more stable at frequencies above 6.2 GHz, compared to the sample #2. This can be related to small differences between the characteristics of the VCSEL samples used, or the attenuation in the optical signal path.

The common-mode transmission coefficient $S_{sc21}$ characteristics for both probe circuit samples follow a similar trend. The common-mode signal level is relatively stable up to around 3.7 GHz, after which it increases steadily. However, in this frequency range, the common-mode signal level of the probe circuit sample #2 is around 5 dB lower than for the sample #1. At frequencies above 4.6 GHz both probe circuits follow a similar trend, with the common-mode signal level of the sample #2 being around 3 dB higher. Given the similar differential-mode characteristics and the difference in the common-mode characteristics, the probe circuit sample #2 has an approximately 5 dB higher CMRR up to 3.7 GHz. At this frequency both probe circuits have a drop in CMRR of around 10 dB, with the dip in the CMRR being more pronounced for the probe circuit sample #1. At frequencies above 4.7 GHz, both probe circuit characteristics follow a similar trend, with the CMRR dropping steadily to below 0 dB.

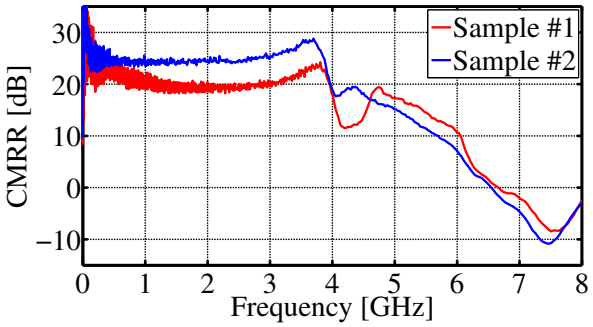
The differences between the characteristics of the two probe circuit samples, with identical circuit and layout configurations, are a result of the tolerances of the components used in the at-



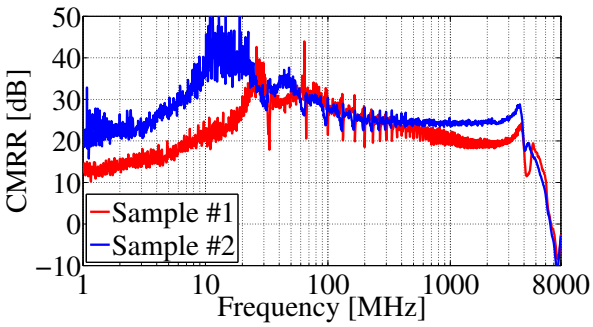

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.9:** Comparison of the measurements of the two samples of the probe circuit 1000R attenuator configuration. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probe circuits are biased using the isolated power supply (PoF bias) module.

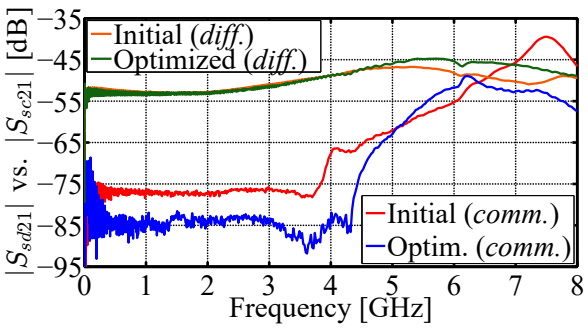
tenuator circuit and the bias circuit, the differences in the soldering process, and the differences in the characteristics of the VCSEL samples used. While typically the hot air soldering process results in more consistent component connections and lower parasitics introduced by soldering, the differences between the samples cannot be attributed solely to that. Using machine soldering to get consistent solder connections and more repeatable circuit samples is another alternative, but with the downside of increased production costs.

The modifications made to the characterized probe circuit design, compared to the initial wafer probe design, result in a significantly higher and more stable CMRR. Using a probe circuit with a lower attenuation ratio, a much higher CMRR can be achieved. The CMRR level can also vary significantly between samples with the identical probe circuit configuration. While a CMRR characteristic that is relatively stable up to 4 GHz can be achieved, at higher frequencies the CMRR decreases steadily, regardless of the probe circuit configuration. This indicates a fundamental limitation of the probe circuit design used.

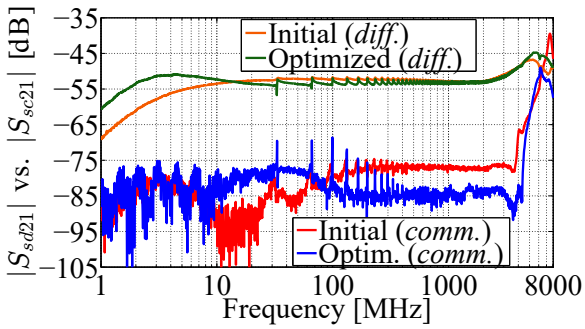
## 4.2 Optimized probe layout

The initial layout of the probe circuit shown in Fig. 4.7a and characterized in Section 4.1.2 is modified. The initial VCSEL model #2 layout is replaced with the optimized VCSEL model #2 layout, discussed in Section 3.5. The initial and the optimized probe circuit layout are characterized and compared. The 1000R attenuator configuration listed in Table 4.2 is used, and the probe circuits are biased using the isolated power supply PoF bias module, shown in Fig. 3.3a. Sample #2 of the initial probe circuit layout with the 1000R attenuator configuration is used. Both the optimized and the initial probe circuit layout are soldered using the hot air soldering process. Three-port S-parameters of the optimized probe circuit characterization structure are measured using a two-port VNA [68], and the mixed-mode S-parameters are calculated.

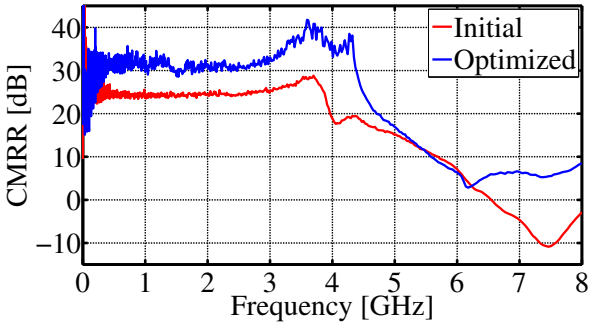
The mixed-mode S-parameter measurement results of the initial and the optimized probe circuit layout are compared in Fig. 4.10. The value of the differential-mode transmission coefficient $S_{sd21}$ at lower frequencies is close to the nominal value of –54 dB, for both probe circuit layouts. The general trend of the differential-mode signal is very similar for both probe circuit layouts in the frequency range up to 4.6 GHz. At higher frequencies there is a difference between the two differential-mode characteristics of around 3 dB. The decrease in attenuation is



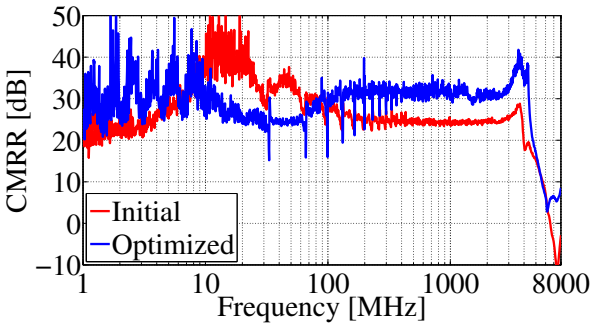

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.10:** Comparison of the measurements of the initial and the optimized probe circuit layout. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probe circuits are biased using the isolated power supply (PoF bias) module.

slightly higher for the optimized probe circuit layout. The lower cutoff frequency is also lower for the optimized probe circuit layout.

The general trend of the common-mode transmission coefficient $S_{sc21}$ is similar for probe circuit layouts and it is relatively stable up to around 4 GHz. In this frequency range, the value of the common-mode signal for the initial probe circuit layout is approximately 7 dB higher than for the optimized probe circuit layout, after which the common-mode signal for both probe circuit layouts increases steadily. At frequencies above 6.2 GHz, the common-mode signal level continues to increase for the initial probe circuit layout, while it slowly drops for the optimized probe circuit layout.

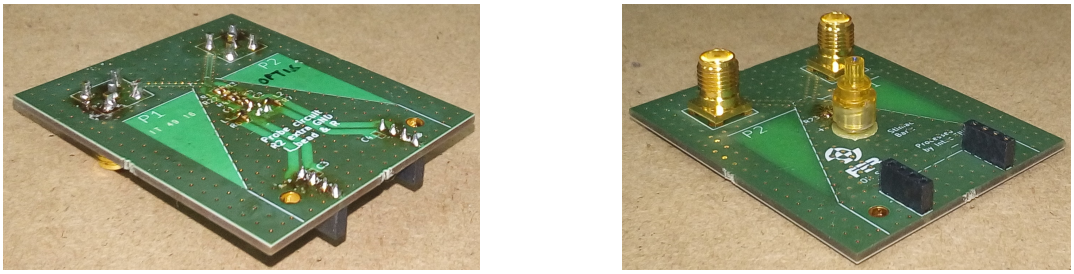
The general trend of the CMRR characteristics for both probe circuit layouts are similar. Given the comparable differential-mode signal levels and the lower common-mode signal level, the CMRR of the optimized probe circuit layout is around 7 dB higher than for the initial probe circuit layout, in the frequency range up to 4.5 GHz. The CMRR of the initial probe circuit layout is above 25 dB up to 3.9 GHz, after which it drops steadily. For the optimized probe circuit layout, the CMRR is above 30 dB up to 4.4 GHz, after which it drops steadily. Both CMRR characteristics drop below 10 dB, while the initial probe circuit layout characteristic continues to drop below 0 dB.

It is demonstrated that the optimization of the VCSEL layout translates into better performance of the probe circuit layout. The CMRR value is increased by around 7 dB, compared to the nominal probe circuit layout. The fast drop in CMRR at frequencies above 4.5 GHz, that is observed for other probe designs, is also present in the characteristic of the optimized probe circuit layout.

The optimized probe circuit layout is implemented on two voltage probes. One probe is designed as a differential connectorized probe with a well-defined ground connection. The other probe is designed as a fully floating differential wafer probe. Despite the difference in the fixture and ground connection, both probes are realized in a differential configuration and the laser is driven differentially. The different fixture types and ground connections are used in order to evaluate the impact of the ground connection on the probe performance. The performance of the probes is compared when using the isolated power supply PoF bias module, and the non-isolated power supply DC bias module, in order to evaluate the impact of the noise coming from the power supply and noise coupling on the electrical wires. The probe circuit 1000R attenuator configuration listed in Table 4.2 is used. The probes are designed for differential measurement of ESD voltage waveforms with amplitudes up to 100 V (200 $V_{PP}$). Although no significant power dissipation is expected when working with ESD pulses, the maximum allowed input differential RMS voltage between physical ports $P_1$ and $P_2$ is 14.1 V. This also makes the probes suitable for certain EMC measurement applications.

### 4.2.1 Connected-ground probe

The connected-ground probe is a differential connectorized probe with a well-defined ground connection. The probe circuit characterization structure with the optimized probe circuit layout is used as the connected-ground probe. The probe circuit design is shown in Fig. 4.7a. The 1000R attenuator configuration listed in Table 4.2 is used. The probe is realized on a PCB which uses a fixture realized using two SMA connectors and 50-Ohm CBCPW feed lines, as shown in Fig. 4.7b. The SMA connectors allow for simple characterization of the probe and provide a good ground connection between the measurement setup and the probe ground plane. CBCPW transmission lines are used in order to reduce the coupling between the two input traces [81]. The connected-ground probe is realized on the PCB stack-up shown in Fig. 1.3. The components and traces of the fixture, the attenuator circuit, and the bias circuit are positioned on the Top layer of the PCB. The SMA connectors used to make the input RF connection, the laser used for the optical connection, and the sockets used for connecting the bias module are located on the Bottom layer of the PCB. The Top and Bottom layer are separated by the ground plane on the Inner layer of the PCB. The connected-ground probe PCB design is shown in Fig. 4.11.



(a) Top side. (b) Bottom side.

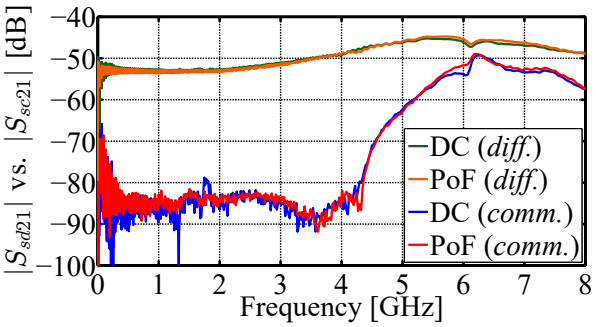
**Figure 4.11:** Connected-ground probe PCB design.

Three-port S-parameters of the connected-ground probe are measured. The measurements are performed using a two-port VNA [68], in the frequency range from 1 MHz to 8 GHz. Based on the measurements of a series of calibration structures, the characteristics of the probe fixture are extracted. The impact of the probe fixture is de-embedded from the measurement results, and the calibration reference plane is shifted to the input of the probe circuit, as shown in Fig. 4.7b. The de-embedded measurement results of the connected-ground probe include only the probe circuit characteristics. The two physical input ports $P_1$ and $P_2$ form the logical balanced (differential) input port (P1), while the single-ended physical port $P_3$ forms the logical single-ended output port (P2), as shown in Fig. 4.7. The entire electro-optical signal path is characterized, from the probe input RF ports to the photodetector output port. The measured three-port standard S-parameters of the connected-ground probe are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58), as described in Section 2.1.1.

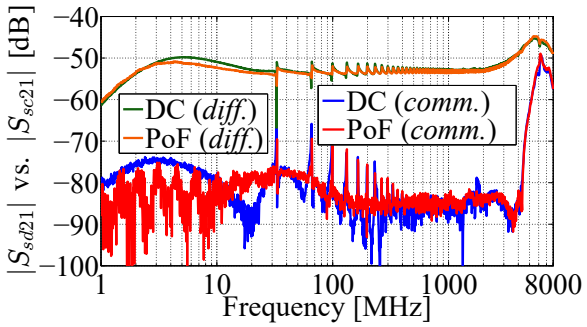
The mixed-mode S-parameter measurement results of the connected-ground probe are shown in Fig. 4.12. The characteristics of the probe when using the isolated power supply PoF bias module (Fig. 3.3a) and the non-isolated power supply DC bias module (Fig. 3.3b) are compared. The differential-mode transmission coefficient $S_{sd21}$ is effectively the same in both cases. The differential signal level at low frequencies is near the nominal value of –54 dB, and remains within ±3 dB of the nominal value up to 3.4 GHz. The attenuation decreases with frequency as a result of parasitic effects. Primarily the parasitic capacitance which effectively lowers the impedance of the components used in the attenuator circuit.

The common-mode transmission coefficient $S_{sc21}$ is relatively stable up to 4.3 GHz, after which the signal level increases significantly. This is a result of the interaction between the parasitics and the mode conversion in the VCSEL and the attenuator circuit. Slightly more noise is observable in the common-mode characteristic for the measurements with the non-isolated power supply, compared to the isolated power supply. This is expected given that the noise coming from the non-isolated power supply has more impact on the low level common-mode signal, compared to the differential-mode signal, which is around 30 dB higher.

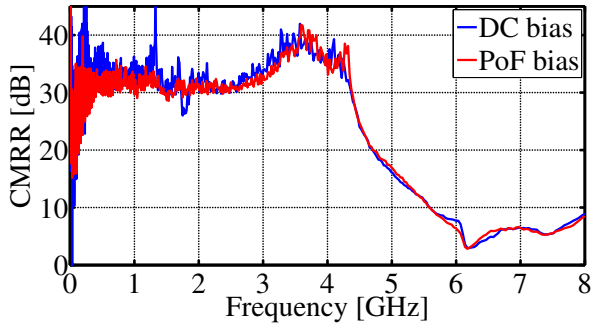
The CMRR of the connected-ground probe is relatively stable and remains above 30 dB up to 4.4 GHz. After this frequency the CMRR drops steadily, as a result of the increase in the



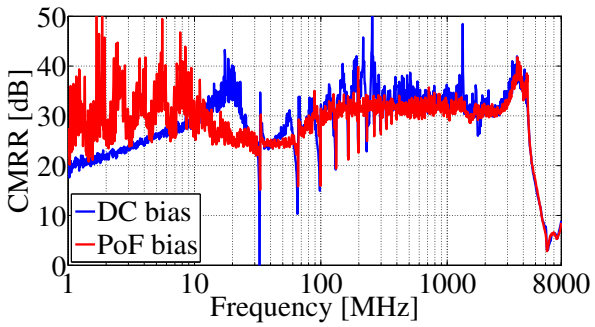

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.12:** Comparison of the measurements of the connected-ground probe biased using the isolated power supply (PoF bias) module and the non-isolated power supply (DC bias) module. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

common-mode signal level. The trend of the CMRR characteristic is similar for both power supplies, with a bit more noise present in the case of the non-isolated power supply, which comes from the common-mode characteristic.

### 4.2.2 Floating-ground probe

The floating-ground probe is a fully floating two-pin differential wafer probe. The optimized probe circuit layout shown in Fig. 4.7a, that is used on the connected-ground probe, is also implemented on the wafer probe PCB. The 1000R attenuator configuration listed in Table 4.2 is used. The probe fixture consists of two 50-Ohm microstrip traces terminated with wafer probe pins with a 1 mm pitch, as shown in Fig. 4.13. To allow simple characterization of the probe, an additional adapter PCB is used as a transition between the measurement setup and the wafer probe. The adapter PCB has two input SMA connectors used for connecting the measurement equipment. These connectors allow for simple characterization and also provide a good ground connection between the measurement setup and the ground plane on the adapter PCB. Each SMA connector is connected to a pad using a 50-Ohm CBCPW transmission line. CBCPW feed lines are used to reduce the coupling between the two traces. The pads on the adapter PCB are used to land the wafer probe and achieve a differential connection between the measurement equipment and the probe circuit. There is no connection between the ground plane of the adapter PCB and the ground plane of the wafer probe, which means that the ground plane of the wafer probe is floating, and there is no ground reference.

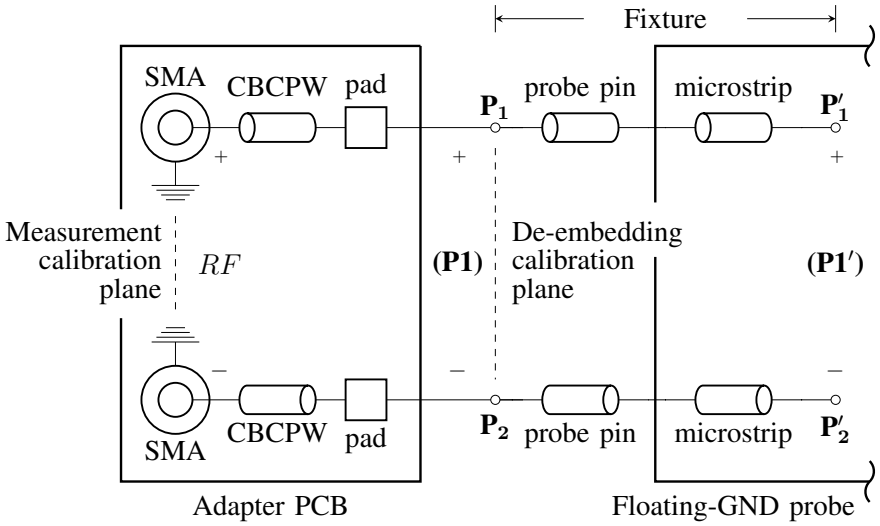
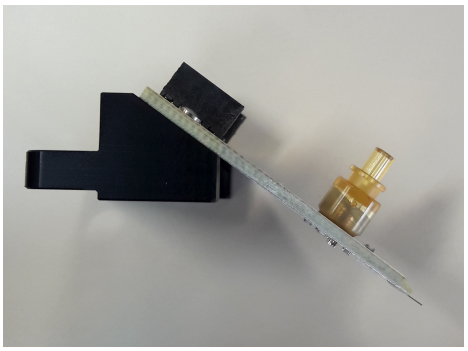



**Figure 4.13:** Fixture of the floating-ground wafer probe.

The floating-ground wafer probe is realized on the |Z| Probe® [14] PCB layout, using the PCB stack-up shown in Fig. 1.3. All the circuits and traces are realized on the Top layer of the PCB, while the RF, DC and optical connections are made on the Bottom layer of the PCB. The

ground plane on the Inner layer of the PCB is used to separate the components on the top and bottom side of the PCB. The floating-ground probe PCB design is shown in Fig. 4.14.

(a) Floating-ground probe design (top).



(b) Floating-ground probe design (side).

**Figure 4.14:** Floating-ground wafer probe PCB design.

Three-port S-parameters of the floating-ground probe are measured. The measurements are performed using a two-port VNA [68], in the frequency range from 1 MHz to 8 GHz. Based on the measurements of a series of calibration structures, the characteristics of the adapter PCB used to characterize the floating-ground probe are extracted. The impact of the adapter PCB consisting of two SMA connectors, CBCPW feed lines and probe landing pads is de-embedded. The calibration reference plane is shifted to the input of the wafer pins, as shown in Fig. 4.13. The de-embedded floating-ground probe measurement results include the characteristics of both the wafer probe fixture, consisting of the wafer pins and input microstrip traces, as well as the probe circuit.

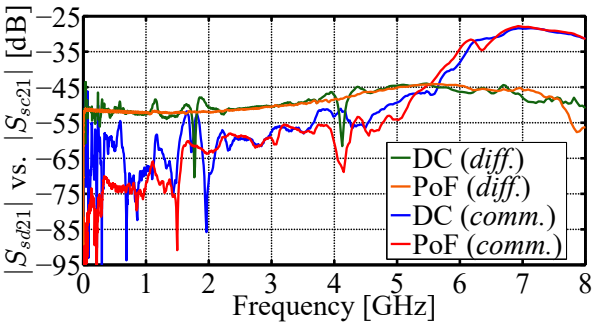
The two physical input ports $P_1$ and $P_2$ form the logical balanced (differential) input port (P1), while the single-ended physical port $P_3$ forms the logical single-ended output port (P2), as shown in Figs. 4.7a and 4.13. The measured three-port standard S-parameters of the floating-ground probe are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58), as described in Section 2.1.1.

The mixed-mode S-parameter measurement results of the floating-ground probe are shown in Fig. 4.15. The characteristics of the probe when using the isolated power supply PoF bias module (Fig. 3.3a) and the non-isolated power supply DC bias module (Fig. 3.3b) are compared. For the case of the isolated power supply, the differential-mode transmission coefficient $S_{sd21}$ is around –52 dB at low frequencies, and remains within $\pm 3$ dB of that value up to 3.6 GHz. The general trend of the differential signal when using the non-isolated power supply is similar, however, significantly more noise is present, causing sharp resonances in the characteristic.

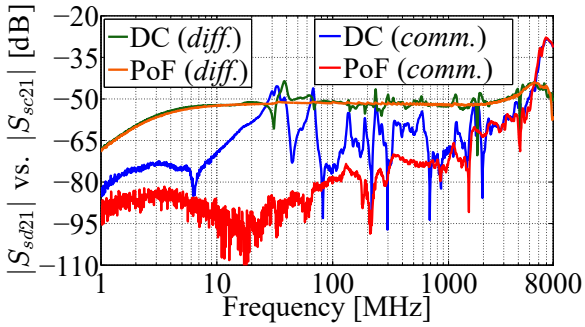
The common-mode transmission coefficient $S_{sc21}$ level when using the isolated power supply starts below –80 dB for frequencies below 100 MHz, and increases significantly with frequency. The relatively high common signal level is a result of the uncontrolled parasitic coupling between the floating wafer probe and the underlying characterization setup. The cou-

pling between these relatively large structures introduces a number of resonances that appear at lower frequencies. Severe noise is present in the common-mode characteristic when using the non-isolated power supply, particularly at frequencies below 2 GHz. At higher frequencies, the common-mode characteristics for both cases follow a similar trend.

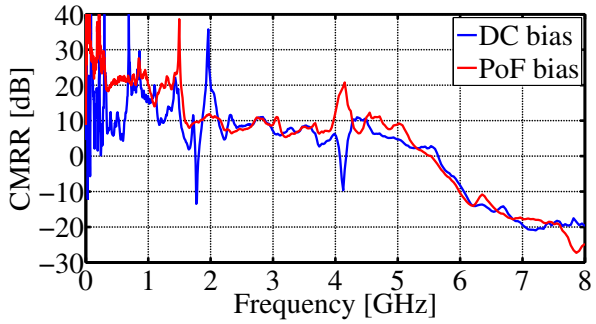
The CMRR of the floating-ground probe with the isolated power supply is around 25–30 dB up to 300 MHz, with a sudden drop to 20 dB, and a further significant drop at 1.5 GHz. The noise present in both the differential and common signal introduces significant noise to the CMRR characteristic. The CMRR characteristic of the floating-ground probe with the non-isolated power supply is too noisy for interpretation. The impact of the noise coming from the non-isolated power supply is very pronounced, especially for the common signal.



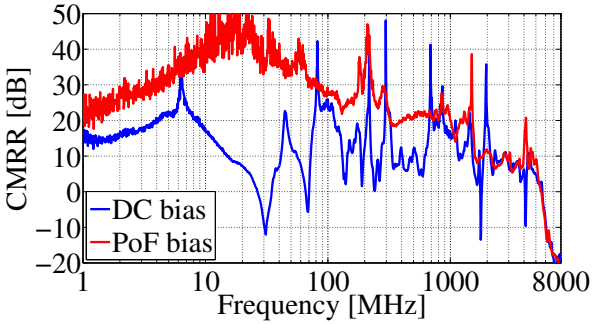

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

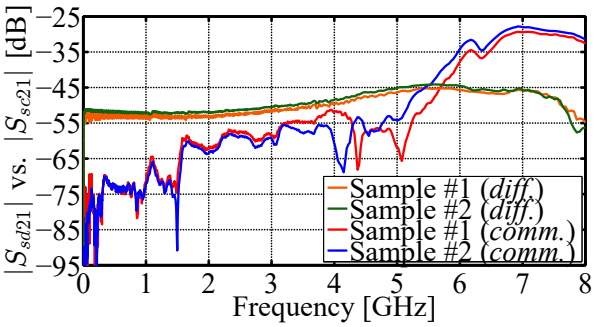
**Figure 4.15:** Comparison of the measurements of the floating-ground probe biased using the isolated power supply (PoF bias) module and the non-isolated power supply (DC bias) module. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

### Floating-ground probe sample repeatability

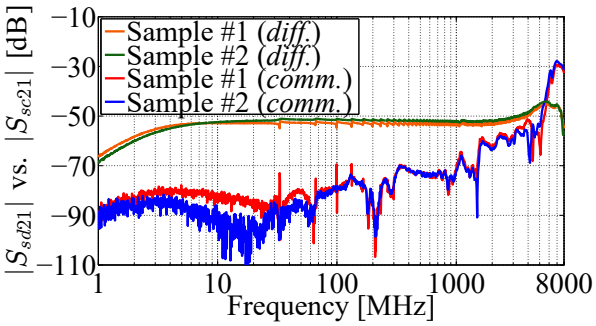
Two samples of the floating-ground wafer probe are assembled and characterized. The wafer probes are biased using the isolated power supply PoF bias module. The mixed-mode S-parameter measurement results of the two floating-ground probes are compared in Fig. 4.16. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is similar for both probes

in the entire measurement frequency range. The probe sample #1 has a slightly lower differential-mode signal level, compared to the sample #2, with the difference being around 1 dB at lower frequencies. The value of the common-mode transmission coefficient $S_{sc21}$ is similar for both probes up to 3.2 GHz. There are some differences between the two common-mode characteristics around the resonances in the frequency range from 3.9 GHz to 5.3 GHz. At higher frequencies, the general trend of the common-mode characteristics is similar for both probes, with the common-mode signal level increasing steadily.

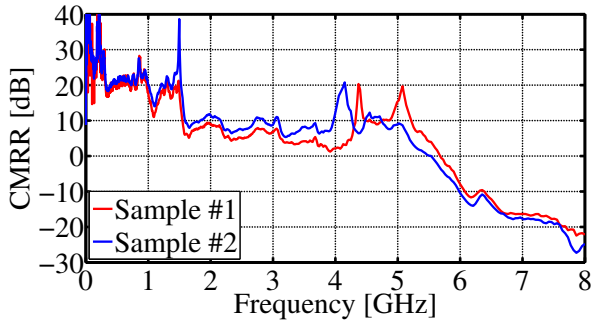
Given the similar differential-mode and common-mode characteristics, both probes have a similar CMRR characteristic. The floating-ground probe sample #2 has a slightly higher CMRR level overall, compared to the sample #1. For frequencies up to 900 MHz, the CMRR of the probe sample #2 is on average around 2 dB higher, while at higher frequencies the difference between the two characteristics typically varies between 2 dB and 5 dB. For frequencies above 5.1 GHz, the CMRR of both wafer probes drops steadily, following a similar slope.



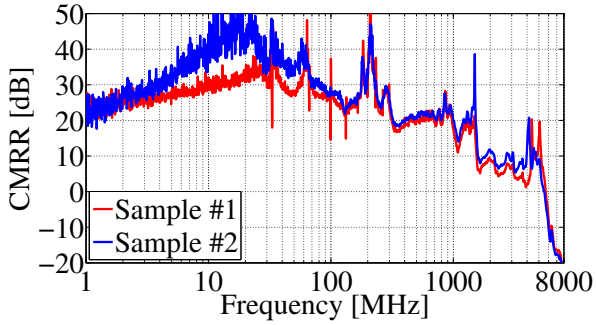

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.16:** Comparison of the measurements of the two floating-ground probe samples. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the isolated power supply (PoF bias) module.

It is shown that both samples of the floating-ground wafer probe have very similar characteristics. The differences in the probe performance are a result of the differences between the VCSEL samples used, the differences in the surface-mount components used, as well as the differences in the parasitics introduced by soldering. Both probes are assembled professionally,

which reduces the dissipation in the probe characteristics introduced by the soldering process. Compared to the repeatability of the probe circuit samples shown in Fig. 4.9, the professionally assembled floating-ground wafer probes show significantly better repeatability of the characteristics. The difference in the CMRR between the two measured floating-ground probe samples is lower, compared to the characterized probe circuit samples, particularly in the frequency range up to 1.5 GHz, where the CMRR level is the highest.

**Floating-ground probe design version comparison**

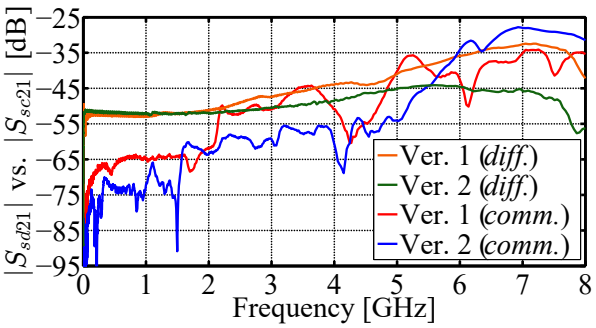
The initial wafer probe design (version 1), shown in Fig. 4.2 and discussed in Section 4.1.1, and the optimized floating-ground wafer probe design (version 2), shown in Figs. 4.7a and 4.13, are compared. The 1000R attenuator configuration is used, that is listed in Table 4.1 for the wafer probe version 1, and in Table 4.2 for the wafer probe version 2. The mixed-mode S-parameter measurement results of the wafer probe version 1 and version 2, biased using the isolated power supply PoF bias module, are compared in Fig. 4.17.

The value of the differential-mode transmission coefficient $S_{sd21}$ for both wafer probe design versions is similar in the frequency range up to 2 GHz. The probe version 2 has a slightly higher lower cutoff frequency. At higher frequencies, the attenuation of the probe version 1 is significantly lower compared to the probe version 2, with the difference between the two differential characteristics growing steadily up to 13 dB at 7 GHz. The differential-mode signal level remains within $\pm 3$ dB of the nominal value up to 2.4 GHz for the probe version 1, and up to 3.6 GHz for the probe version 2. This significantly greater drop in attenuation of the wafer probe version 1 is a result of using a different attenuator circuit layout, without a ground plane.

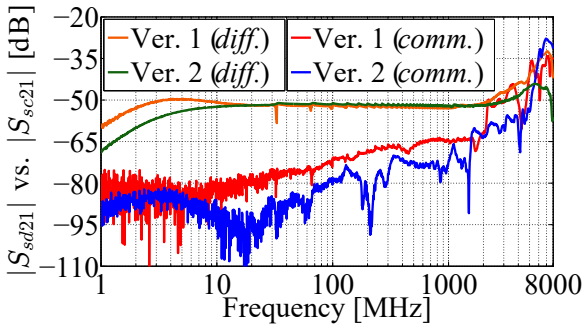
The common-mode transmission coefficient $S_{sc21}$ of the wafer probe version 2 is around 10 dB lower in the frequency range up to 1.5 GHz, compared to the probe version 1. A similar difference between the two common-mode characteristics is also observable in the frequency range between 2.2 GHz and 4.2 GHz. A sudden increase in the common-mode signal level of around 10 dB is observed at 1.5 GHz for the probe version 2, and around 2.1 GHz for the probe version 1. For frequencies above 5 GHz, the probe version 2 has a faster increase in the common-mode signal level, and an overall higher common-mode signal level above 5.6 GHz.

The similar differential-mode characteristics of the two characterized wafer probes at lower frequencies, in combination with a lower common-mode signal level of the wafer probe version 2, results in approximately 10 dB higher CMRR for the wafer probe version 2, in the frequency range up to 1.5 GHz, compared to the wafer probe version 1. At 1.5 GHz there is a 10 dB drop in the CMRR level of the probe version 2, while this drop is at 2.1 GHz for the probe version 1. The wafer probe version 2 has a more stable CMRR value between 2.1 GHz and 5.1 GHz, with a steady drop in CMRR at higher frequencies.

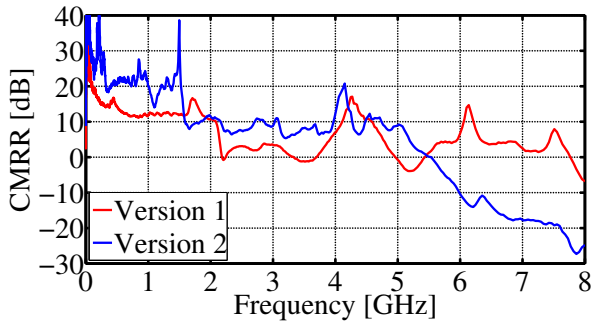
It is shown that the optimized probe circuit layout implemented on the floating-ground wafer



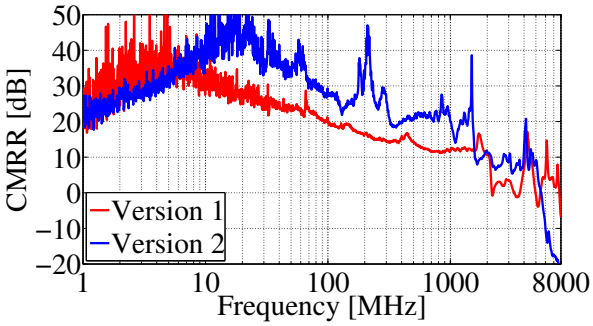

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.17:** Comparison of the measurements of the initial wafer probe design (version 1) and the optimized floating-ground wafer probe design (version 2). The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the isolated power supply (PoF bias) module.

probe version 2 has significantly better characteristics, compared to the initial probe circuit design implemented on the initial wafer probe version 1. The CMRR level is significantly higher, and the differential-mode signal level is more stable over a wide frequency range. At higher frequencies, the limitations of the probe circuit design are observable, which results in a steady drop in CMRR, that is present for all probe circuit designs.

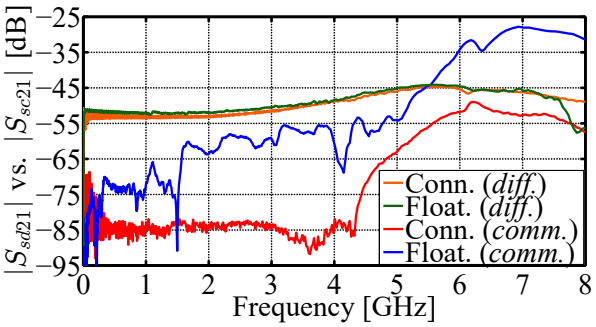
### 4.2.3 Probe comparison

The mixed-mode S-parameter measurement results of the connected-ground probe, shown in Fig. 4.7, and the floating-ground probe, shown in Figs. 4.7a and 4.13, are compared in Fig. 4.18. The probes are biased using the isolated power supply PoF bias module, shown in Fig. 3.3a. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is the same for both probes. The floating-ground probe has around 2 dB lower nominal attenuation, compared to the connected-ground probe. This can be a result of slightly different attenuation in the optical signal path, as well as small differences in the characteristics of the VCSEL and the passive components used in the attenuator circuit. However, the attenuation of the signal should apply in a similar way to both the differential and common signal level, thus not affecting the CMRR.

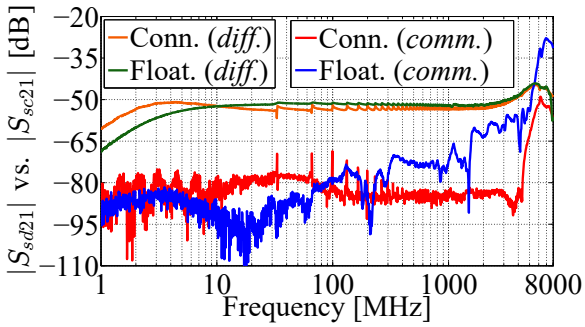
A similar trend in the differential-mode characteristics is expected because both probes use the same probe circuit design, and the impact of the noise is not significant given the high level of the differential signal. The offset between the two characteristics decreases at higher frequencies as a result of the additional attenuation introduced by the wafer probe fixture.

The level of the common-mode transmission coefficient $S_{sc21}$ is significantly lower for the connected-ground probe than for the floating-ground probe for frequencies above 300 MHz. While the common-mode signal level is relatively stable for the connected-ground probe, it increases steadily for the floating-ground probe. Due to a lack of a well-defined ground connection, the common-mode signal suppression is significantly worse for the floating-ground probe. The difference between the common-mode characteristics of the two probes above 300 MHz ranges between 10 dB and 30 dB.

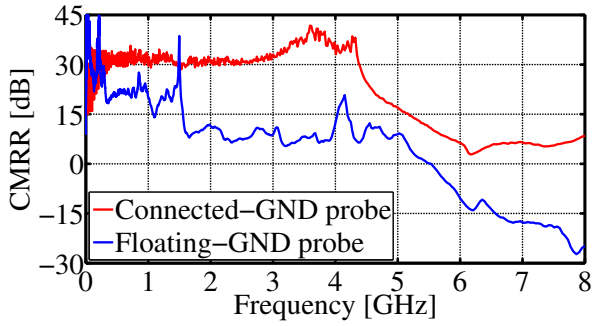
Given the similar differential-mode characteristics and the significant differences in the common-mode characteristics, the connected-ground probe has a significantly higher and more stable CMRR. While both probes are differentially driven, this analysis shows the impact of noise coupling on the fully floating probe via not well-defined parasitic coupling, and the importance of the ground connection where the parasitics are better defined and more stable. The connected-ground probe, which has a well-defined ground connection, has a much higher and



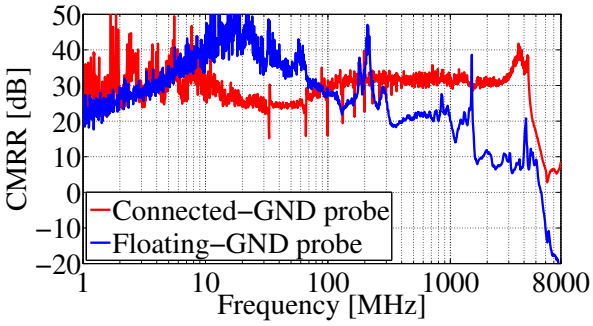

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.18:** Comparison of the measurements of the floating-ground and the connected-ground probe. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the isolated power supply (PoF bias) module.

more stable CMRR, and is more immune to noise. The importance of using an isolated power supply with the floating-ground probe is highlighted.

It is shown that the ground connection does not have an impact on the differential-mode signal propagation, while the impact on the common-mode signal suppression is very significant. A much higher CMRR is achieved when a well-defined ground reference is available. The connected-ground and the floating-ground probe both have a similar 3 dB bandwidth of around 3.5 GHz. However, the connected-ground probe has a CMRR above 30 dB up to 4.4 GHz, while the floating-ground probe has a CMRR above 20 dB up to 1 GHz. Using an isolated power supply limits the level of electromagnetic noise in the measurement system. The impact of the noise coming from a non-isolated power supply and noise coupling on the electrical wires is relatively small for the probe with a well-defined ground reference. However, power supply isolation is critical for the fully floating differential probe, as it greatly reduces the noise level in the differential-mode and especially in the common-mode signal transmission. A steady drop in CMRR at high frequencies is observed for both the connected-ground and the floating-ground probe. A similar drop in CMRR for frequencies above 4.5 GHz is also observed for the other probe circuit designs explored in this thesis, regardless of the probe circuit layout and the attenuation ratio used. It demonstrates a general limitation of the probe circuit design, as a result of the interaction between the parasitics and the mode conversion in the attenuator circuit, and the laser used to transmit the signal. The presented simple and low cost probe circuit design can be further miniaturized and realized on probes with different fixture types and applications in ESD and EMC measurement systems [85, 128].

### Wafer probe ground connection

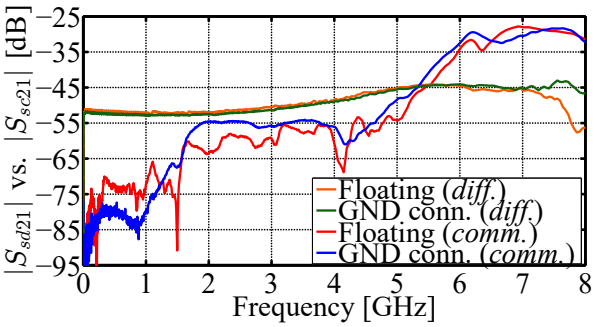
Given the demonstrated impact of the ground connection on the probe performance, particularly in terms of the CMRR, a ground connection is added to the floating-ground wafer probe. A makeshift connection between the ground plane of the wafer probe and the adapter PCB is achieved using copper strips. The goal is to evaluate the performance of the wafer probe with the added ground connection, and compare it to the fully floating wafer probe configuration.

The mixed-mode S-parameter measurement results of the wafer probe with the ground connection and the fully floating wafer probe, biased using the isolated power supply PoF bias module, are compared in Fig. 4.19. The differential-mode transmission coefficient $S_{sd21}$ is very similar for both probe ground connection configurations in the frequency range up to 7.1 GHz. At higher frequencies, there is a drop in the differential-mode characteristic of the fully floating wafer probe.

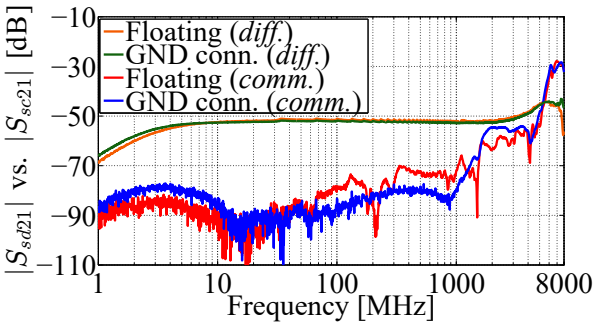
The common-mode transmission coefficient $S_{sc21}$ of the wafer probe with the ground connection is approximately 10 dB lower in the low frequency range from 70 MHz to 1.1 GHz, compared to the fully floating wafer probe. The common-mode signal level of the probe with

the ground connection increases rapidly between 900 MHz and 1.8 GHz. Between 1.6 GHz and 3.2 GHz, the common-mode level for the probe with the ground connection is higher than for the fully floating wafer probe. At higher frequencies, the general trend of the common-mode characteristic is similar for both wafer probes. In the entire measurement frequency range less resonances are observed in the characteristic of the probe with the ground connection, indicating better immunity to noise.

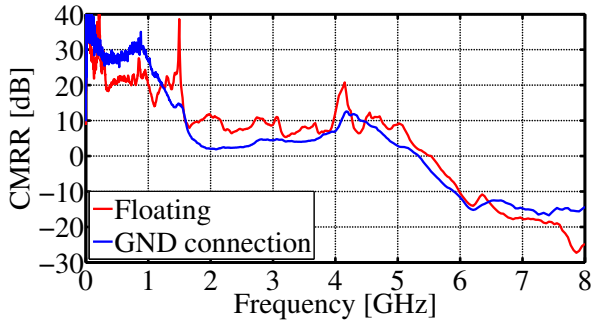
The CMRR of the wafer probe with the ground connection is approximately 10 dB higher in the frequency range between 70 MHz and 1.1 GHz, compared to the fully floating wafer probe, after which it drops rapidly. The CMRR value is lower for the probe with the ground connection in the frequency range between 1.6 GHz and 4.2 GHz, while the characteristics are similar at higher frequencies. As a result of less noise present in the common-mode characteristic, the CMRR of the probe with the ground connection is smoother in the entire measurement frequency range.



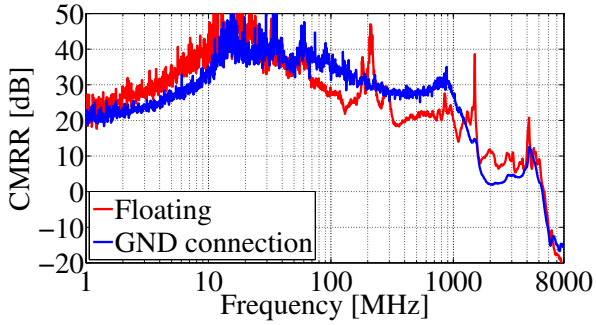

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

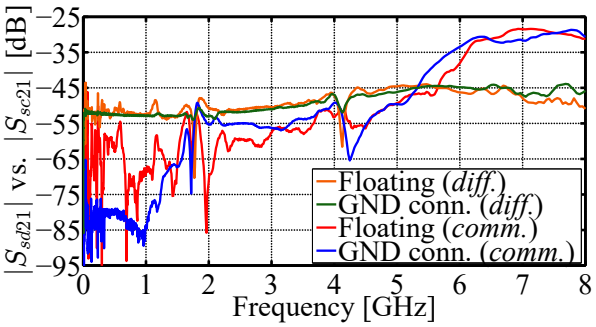
**Figure 4.19:** Comparison of the measurements of the fully floating wafer probe and the wafer probe with the ground connection. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the isolated power supply (PoF bias) module.

The mixed-mode S-parameter measurement results of the wafer probe with the ground connection and the fully floating wafer probe, biased using the non-isolated power supply DC bias module, are compared in Fig. 4.20. The general trend of the differential-mode transmission coefficient $S_{sd21}$ is similar for both wafer probes. It is notable that significantly more noise is

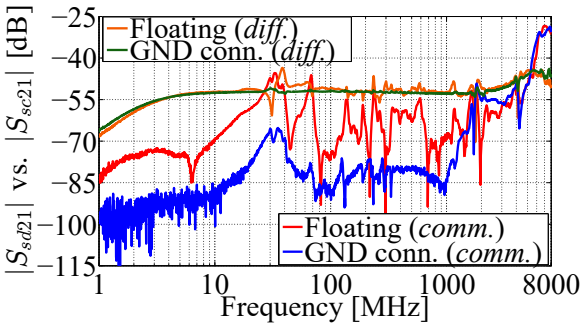
present in the differential-mode characteristic of the fully floating wafer probe, in the frequency range up to 2 GHz, compared to the wafer probe with the ground connection. Similar to when using the isolated power supply, the differential-mode signal level of the fully floating wafer probe drops at frequencies above 7 GHz, while the signal level remains more stable for the wafer probe with the ground connection.

In the characteristic of the common-mode transmission coefficient $S_{sc21}$ of the fully floating wafer probe, there is significant noise that is manifested in the form of multiple resonances and antiresonances, in the frequency range up to 2 GHz. The common-mode signal of the wafer probe with the ground connection is significantly more stable in the same frequency range, with much less noise in the characteristic. The level of the common-mode signal of the wafer probe with the ground connection is around 20 dB lower up to 1 GHz, compared to the fully floating wafer probe, after which the common-mode signal increases rapidly. For frequencies above 2.2 GHz, the general trend of the two characteristics is similar, with the common-mode characteristic of the probe with the ground connection being smoother.

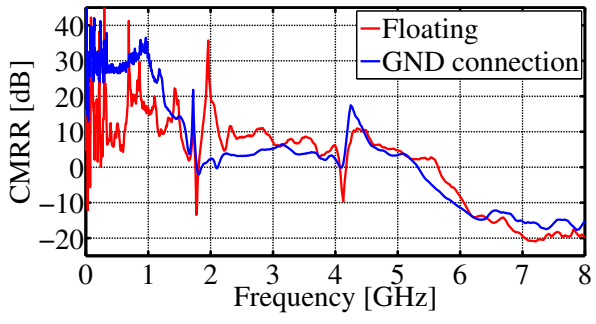
The CMRR level of the wafer probe with the ground connection is between 15–20 dB higher than for the fully floating wafer probe, in the frequency range up to 1 GHz. Above 1 GHz, the CMRR of the probe with the ground connection has a sudden drop to close to 0 dB at 1.8 GHz.



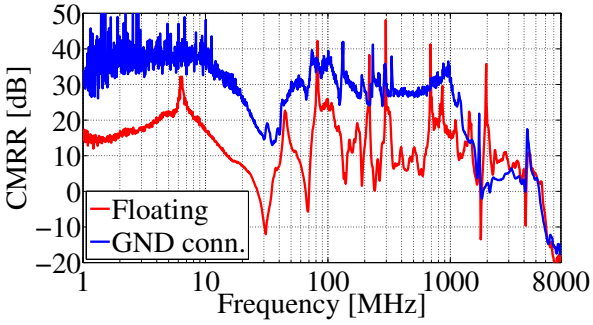

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.20:** Comparison of the measurements of the fully floating wafer probe and the wafer probe with the ground connection. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared. The probes are biased using the non-isolated power supply (DC bias) module.

In the whole measurement frequency range it is observed that the CMRR characteristic of the wafer probe with the ground connection is much smoother and more stable, with significantly less resonances and antiresonances, compared to the fully floating wafer probe.

By adding a ground connection to the wafer probe, the impact of having a ground reference on the performance of the probe is confirmed. Using a ground connection on the probe lowers the common-mode signal level, and makes both the differential-mode and common-mode signal transmission less susceptible to noise. This results in a higher CMRR level, with a more stable and smoother CMRR characteristic. The impact of the ground connection is more pronounced when using the non-isolated power supply, given that the noise suppression is more significant in that case. The makeshift ground connection used to perform the measurements has a limited bandwidth. The parasitics and the asymmetry introduced by the copper strips limit the effectiveness of the ground connection for frequencies above 1 GHz. In order to have a well-defined ground connection on the wafer probe, a different fixture configuration needs to be used. Ground pins need to be added to the existing 2-pin differential fixture configuration. A ground-signal-ground-signal-ground (GSGSG) fixture configuration would be more suitable, in order to achieve a symmetrical and well-defined ground connection on the wafer probe.

## 4.3 Probe input impedance characterization

The input impedance of the connected-ground probe and the floating-ground probe, discussed in Section 4.2, is analyzed based on the S-parameter measurements. The schematic of the connected-ground probe is shown in Fig. 4.7, while the schematic of the floating-ground probe is shown in Figs. 4.7a and 4.13. Both probes share the same probe circuit design. The connected-ground probe has a well-defined ground connection, while the floating-ground probe is fully floating, with no connection between the ground plane of the probe and the measurement setup. The probes are biased using the isolated power supply PoF bias module (Fig. 3.3a).

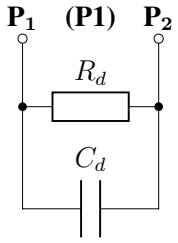
The probes are characterized in terms of the differential-mode and common-mode input impedance at the logical port (P1), shown in Figs. 4.7b and 4.13. Simplified circuit models are proposed to model the general trend of these impedances and extract the value of the parasitics. The differential-mode input impedance $Z_{d1}$ at the balanced logical port (P1) is the total impedance seen between the physical ports $P_1$ and $P_2$, as illustrated in Fig. 2.15a. The common-mode input impedance $Z_{c1}$ at the logical port (P1) is the effective shunt impedance seen from the physical ports $P_1$ and $P_2$ towards the ground, as illustrated in Fig. 2.15b. The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ are calculated using the mixed-mode S-parameter matrix at the logical port (P1) obtained using (2.54)–(2.57). Taking into account the configuration of the probes under differential-mode and common-mode drive conditions, as well as the mode conversion, the differential-mode input impedance $Z_{d1}$ is calculated using (2.70), and the common-mode input impedance $Z_{c1}$ is calculated using (2.71), as described in Section 2.1.4.

### 4.3.1 Connected-ground probe

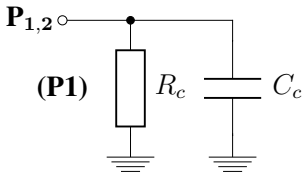
Simplified circuit models of the input impedance of the characterized probes are proposed in order to better understand the impedance characteristics and extract the parasitic values. The general trend of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the connected-ground probe is approximated by a first-order parallel RC circuit model, presented in Fig. 4.21. The model parameters are optimized and fitted to the measurement results, by fitting the phase characteristics at 45 deg. The fitted parameters of the connected-ground probe input impedance circuit models are given in Table 4.3. A comparison between the measurement results and the circuit models is shown in Fig. 4.22.

The resistances $R_d$ and $R_c$ represent the nominal differential-mode and common-mode input impedance of the probe, respectively. The parallel common-mode capacitance $C_c$ is the effective shunt capacitance seen from the physical ports $P_1$ and $P_2$ towards the ground. The parallel differential-mode capacitance $C_d$ is the effective capacitance seen between the physical ports $P_1$ and $P_2$, which is a result of the ground path and inter-port capacitance. Both capacitances are

very low, with the differential-mode capacitance being approximately four times lower. Given the combination of a higher resistance and a lower capacitance, the differential-mode input impedance is higher and more stable in the entire measurement frequency range, compared to the common-mode input impedance.




(a) Differential-mode input impedance.

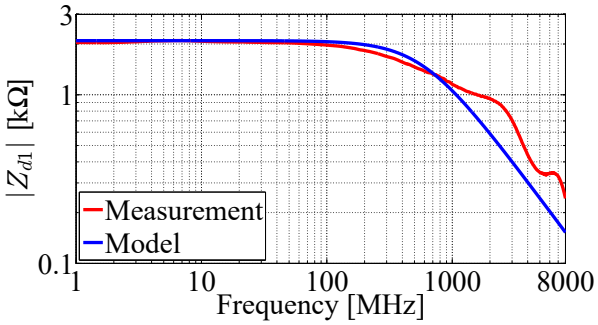



(b) Common-mode input impedance.

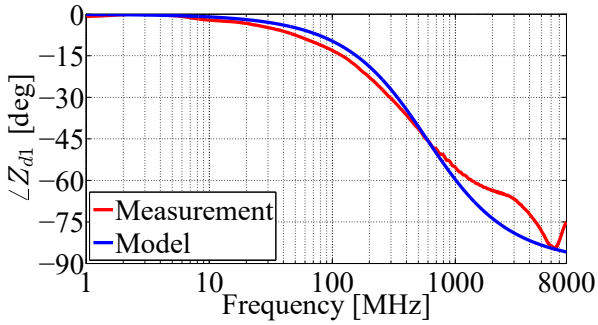
**Figure 4.21:** Connected-ground probe: simplified equivalent circuit model of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$.

**Table 4.3:** Connected-ground probe input impedance circuit model parameters.

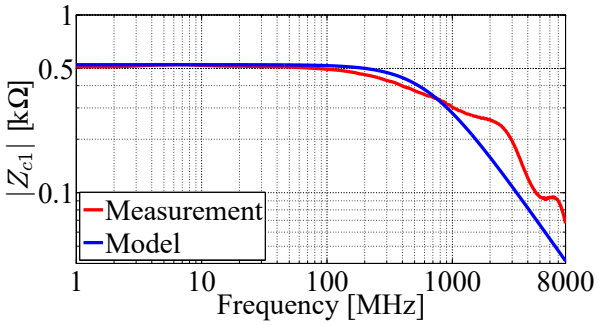
| $R_d$ | $C_d$ | $R_c$ | $C_c$ |
|---|---|---|---|
| 2095 Ω | 0.13 pF | 525 Ω | 0.48 pF |



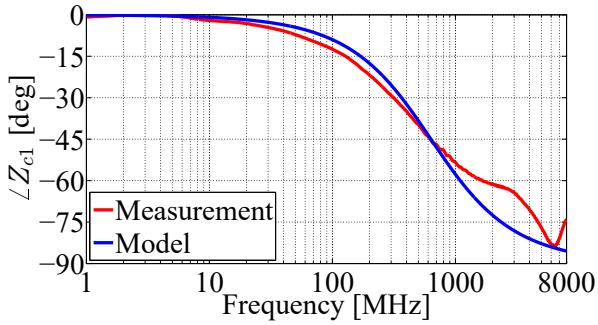

(a) Differential-mode impedance (magnitude).




(b) Differential-mode impedance (phase).




(c) Common-mode impedance (magnitude).

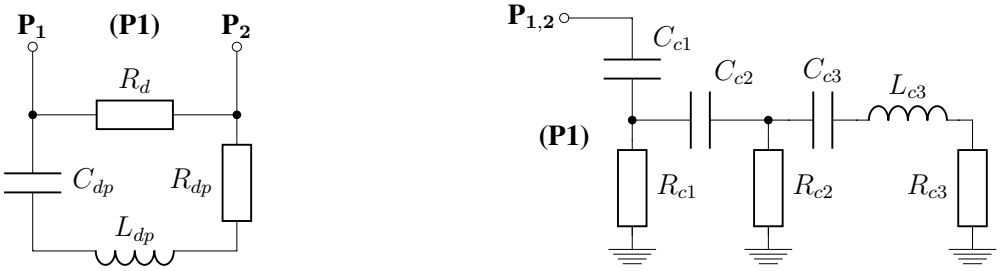



(d) Common-mode impedance (phase).

**Figure 4.22:** Connected-ground probe: magnitude and phase comparison of the measurement and the simplified circuit model of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$.

### 4.3.2 Floating-ground probe

The general trend of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the floating-ground probe is approximated with the circuit models presented in Fig. 4.23. The model parameters are optimized and fitted to the measurement results. The fitted parameters of the floating-ground probe input impedance circuit models are given in Table 4.4. A comparison between the measurement results and the circuit models is shown in Fig. 4.24.




(a) Differential-mode input impedance.

(b) Common-mode input impedance.

**Figure 4.23:** Floating-ground probe: simplified equivalent circuit model of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$.

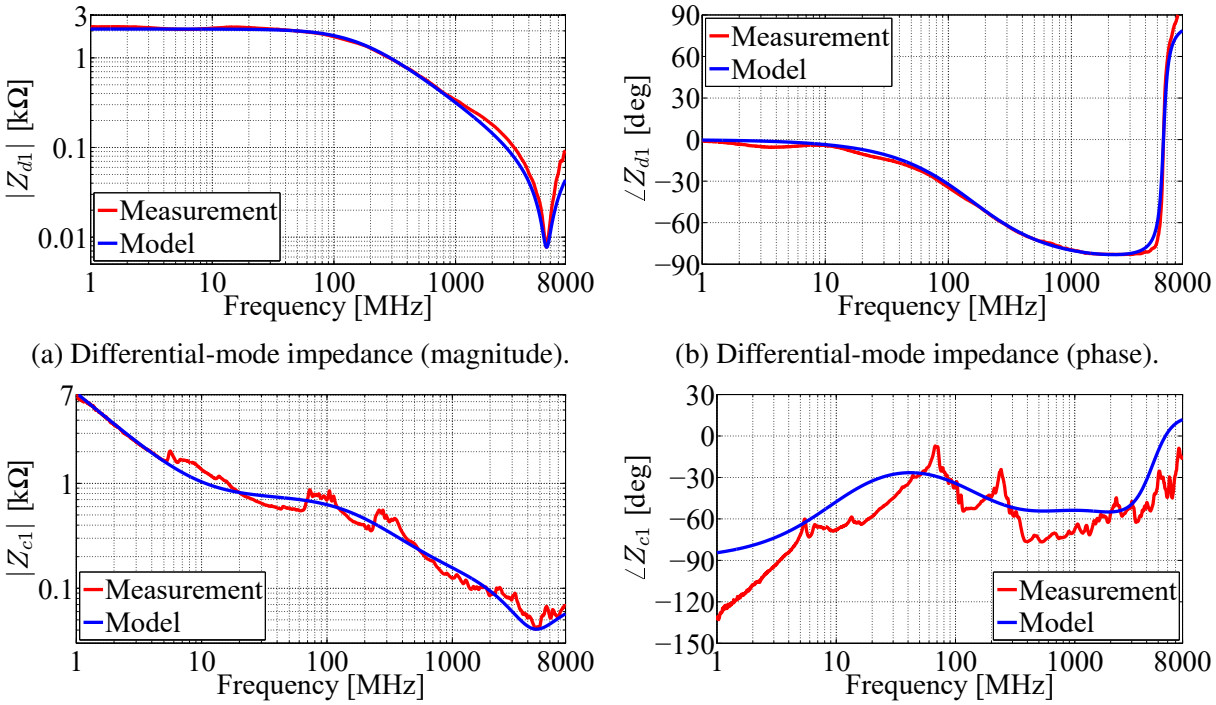
**Table 4.4:** Floating-ground probe input impedance circuit model parameters.

| $R_d$ | $C_{dp}$ | $L_{dp}$ | $R_{dp}$ |
|---|---|---|---|
| 2095 Ω | 0.48 pF | 1.68 nH | 7.73 Ω |

| $C_{c1}$ | $R_{c1}$ | $C_{c2}$ | $R_{c2}$ | $C_{c3}$ | $L_{c3}$ | $R_{c3}$ |
|---|---|---|---|---|---|---|
| 22 pF | 700 Ω | 1.3 pF | 100 Ω | 0.7 pF | 3 nH | 60 Ω |

The differential-mode input impedance of the floating-ground probe is approximated using a parallel combination of the nominal differential-mode resistance $R_d$ and a series RLC circuit. The resistance $R_d$ models the nominal input impedance of the probe at low frequencies, while the series RLC circuit elements $R_{dp}$, $L_{dp}$ and $C_{dp}$ model the resonance at 5.6 GHz. This resonance is a combination of the ground path and inter-port capacitance, as well as the inductance of the probe fixture and the ground path. The differential-mode parasitic capacitance of the floating-ground probe $C_{dp}$ is approximately four times higher than the differential capacitance $C_d$ of the connected-ground probe, resulting in a much faster decrease in impedance.

Given that there is no direct connection between the ground plane of the floating-ground probe and the ground of the measurement setup, the common-mode input impedance is very complex and is loosely defined through parasitics between the probe and the measurement setup.




(a) Differential-mode impedance (magnitude).

(b) Differential-mode impedance (phase).

(c) Common-mode impedance (magnitude).

(d) Common-mode impedance (phase).

**Figure 4.24:** Floating-ground probe: magnitude and phase comparison of the measurement and the simplified circuit model of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$.

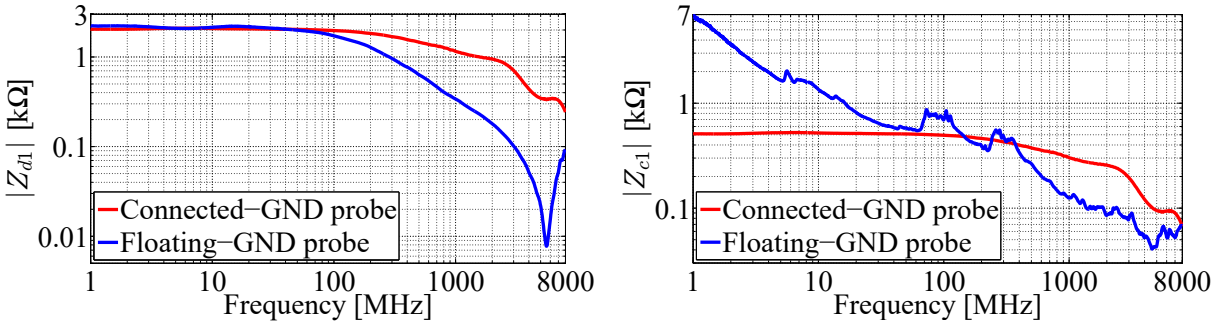
Given the measurement uncertainty of the reflection coefficient, such high parasitic impedances are difficult to measure accurately, particularly at low frequencies [68, 70]. The common-mode impedance is modelled using several stages of CR branches stacked in parallel to the resistance in the previous stage, with a series RLC circuit in the last branch, which models the resonance at 4.6 GHz. It should be noted that all parasitic capacitances in the common-mode model are higher than in the differential-mode model, resulting in a faster drop in impedance.

### 4.3.3 Probe comparison

The comparison of the magnitude of the differential-mode input impedance $Z_{d1}$ of the characterized connected-ground probe and the floating-ground probe, biased using the isolated power supply, is shown in Fig. 4.25a. At low frequencies both probes have a differential impedance close to the nominal value of 2.1 kΩ. This differential impedance is set by the resistors used in the attenuator circuit, listed in Table 4.2. A difference in the differential-mode impedance between the probes is observed at frequencies above 100 MHz. The floating-ground probe has a faster drop in impedance and a resonance is present at 5.6 GHz, while the connected-ground probe has a more stable impedance profile with a slower decrease rate. The difference in the differential input impedance between the probes is a result of a combination of different fixtures and ground connections. The wafer probe pins and microstrip traces in the floating-ground

probe fixture introduce additional parasitics. The lack of a well-defined ground connection results in a decrease in the impedance of the path to the ground with frequency.

The comparison of the magnitude of the common-mode input impedance $Z_{c1}$ of the characterized connected-ground probe and the floating-ground probe, biased using the isolated power supply, is shown in Fig. 4.25b. At low frequencies up to 100 MHz the floating-ground probe has a high common-mode impedance, given that there is no direct ground connection between the probe and the measurement setup. In the entire frequency range up to 4.6 GHz the common-mode impedance of the floating-ground probe is dropping steadily. Given that the path to the ground via parasitics is not well defined, the common-mode impedance characteristic of the floating-ground probe is relatively complex. On the other hand, the common-mode impedance of the connected-ground probe at low frequencies is close to the nominal value of 525 Ω, which is defined by the resistors used in the attenuator circuit. At frequencies above 100 MHz the common-mode impedance of the connected-ground probe is higher than the impedance of the floating-ground probe and the there is a slow drop in impedance with frequency.




(a) Differential-mode input impedance.

(b) Common-mode input impedance.

**Figure 4.25:** Comparison of the measurements of the connected-ground and the floating-ground probe. The magnitude of the differential-mode input impedance $Z_{d1}$ and the common-mode $Z_{c1}$ input impedance are compared. The probes are biased using the isolated power supply (PoF bias) module.

The connected-ground probe, which has a significantly higher and more stable CMRR over a wide frequency range, also has the higher and more stable differential-mode and common-mode input impedance at higher frequencies, with a very low parasitic capacitance. The nominal differential-mode input impedance of the connected-ground probe is 2095 Ω, with a parasitic capacitance of 0.13 pF, while the nominal common-mode input impedance is 525 Ω, with a parasitic capacitance of 0.48 pF [128].

## 4.4 Discussion of common-mode rejection ratio measurements

### 4.4.1 Common-mode rejection ratio definitions

Two definitions of the common-mode rejection ratio are typically used. The voltage definition of the CMRR is typically used when analyzing differential amplifiers [129]. The mixed-mode S-parameter definition of the CMRR is typically used when analyzing differential RF systems at high frequencies [42]. The voltage and the mixed-mode S-parameter definition of the common-mode rejection ratio are compared. A circuit with three physical ports shown in Fig. 4.26 is used an example. The physical ports $P_1$ and $P_2$ form the logical differential input port (P1), while the physical port $P_3$ forms the logical single-ended output port (P2).

#### Voltage definition of the common-mode rejection ratio

The voltage definition of the common-mode rejection ratio uses generators that are directly connected to the input of the device under test for both the differential-mode and the common-mode signal analysis. For the common-mode analysis a common signal is applied to the two input ports. This is achieved by using two in-phase generators as shown in Fig. 4.26a where

$$v_{c,g}^{+} = v_{c,g}^{-}. \tag{4.1}$$

The voltage definition of the CMRR uses generators with no internal impedance. It is assumed that the entire generator voltage is applied to the DUT. The input voltage $v_{c,i}^{+}$ at the port $P_1$ corresponds to the voltage on the positive generator $v_{c,g}^{+}$, while the input voltage $v_{c,i}^{-}$ at the port $P_2$ corresponds to the voltage on the negative generator $v_{c,g}^{-}$ as follows:

$$v_{c,i}^{+} = v_{c,g}^{+}, \tag{4.2}$$

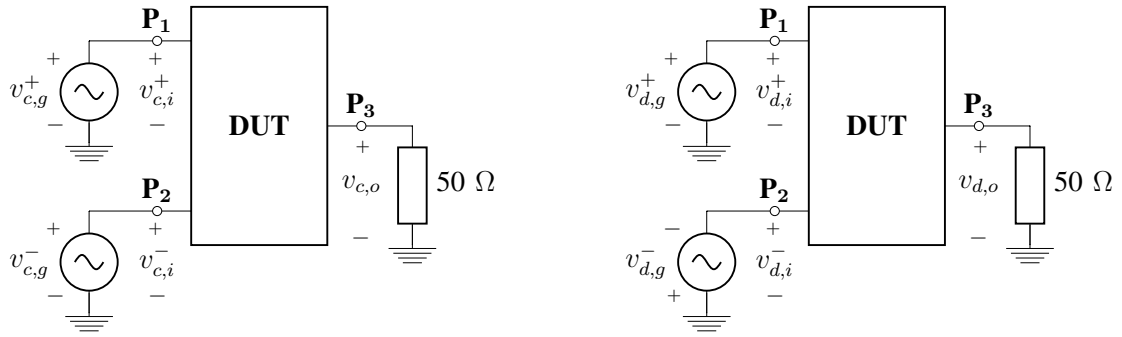
$$v_{c,i}^{-} = v_{c,g}^{-}. \tag{4.3}$$

The common-mode transfer function $A_c$ is defined as the ratio of the output voltage at the port $P_3$ and the mean of the voltages at the two input ports as follows [129]:

$$A_c = \frac{v_{c,o}}{\frac{v_{c,i}^{+} + v_{c,i}^{-}}{2}}. \tag{4.4}$$

For the differential-mode analysis a differential signal is applied between the ports $P_1$ and $P_2$. This is achieved using two counter-phase generators as shown in Fig. 4.26b where:

$$v_{d,g}^{+} = v_{d,g}^{-}. \tag{4.5}$$




(a) Common-mode characterization setup. (b) Differential-mode characterization setup.

**Figure 4.26:** Common-mode rejection ratio voltage characterization setup schematic.

The input voltage $v^+_{d,i}$ at the port $P_1$ corresponds to the voltage on the positive generator $v^+_{d,g}$, while the input voltage $v^-_{d,i}$ at the port $P_2$ corresponds to the voltage on the negative generator $v^-_{d,g}$ as follows:

$$v^+_{d,i} = v^+_{d,g}, \tag{4.6}$$

$$v^-_{d,i} = v^-_{d,g}. \tag{4.7}$$

The differential-mode transfer function $A_d$ is defined as the ratio of the output voltage and the difference of the voltages at the two input ports as follows [129]:

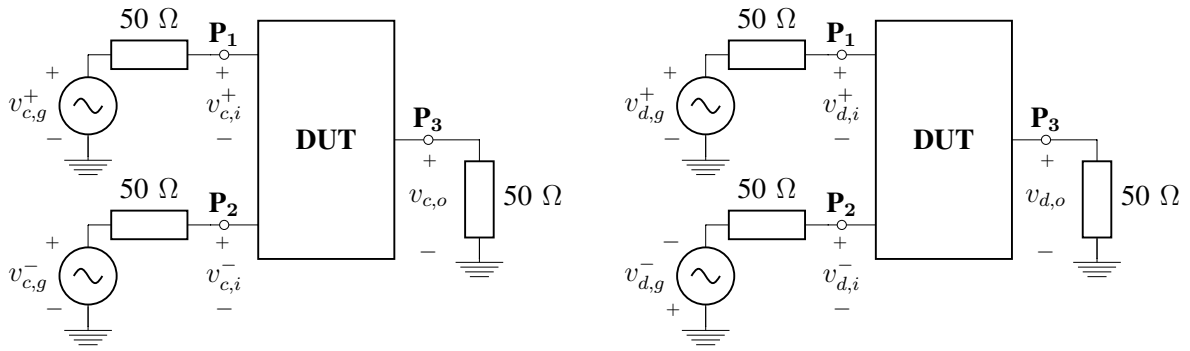
$$A_d = \frac{v_{d,o}}{v^+_{d,i} - v^-_{d,i}}. \tag{4.8}$$

The voltage definition of the common-mode rejection ratio $\mathrm{CMRR}_A$ is defined as the ratio of the magnitude of the differential-mode transfer function $A_d$ and the common-mode transfer function $A_c$ as follows [129]:

$$\mathrm{CMRR}_A = \frac{|A_d|}{|A_c|}. \tag{4.9}$$

### Mixed-mode S-parameter definition of the common-mode rejection ratio

The mixed-mode S-parameter definition of the common-mode rejection ratio uses generators with a 50 Ω internal impedance, that are connected to the input of the DUT. The common-mode transmission coefficient characterization is performed using two in-phase generators with a 50 Ω internal impedance as shown in Fig. 4.27a. For the common-mode characterization the effective internal impedance of the generator corresponds to the 25 Ω common-mode characteristic impedance. The mixed-mode S-parameter common-mode transmission coefficient $S_{sc21}$ is defined as the sum of the standard single-ended S-parameter transmission coefficient from the port $P_1$ to the port $P_3$ ($S_{31}$), and the transmission coefficient from the port $P_2$ to the port $P_3$ ($S_{32}$),




(a) Common-mode characterization setup.

(b) Differential-mode characterization setup.

**Figure 4.27:** Common-mode rejection ratio mixed-mode S-parameter characterization setup schematic.

divided by the square root of two [42]. The common-mode transmission coefficient can also be calculated using voltages, where the output voltage $v_{c,o}$, the positive generator voltage $v^+_{c,g}$, and the negative generator voltage $v^-_{c,g}$ are used as follows:

$$S_{sc21} = \frac{1}{\sqrt{2}}(S_{31} + S_{32}) = \frac{1}{\sqrt{2}}\left(\frac{v_{c,o}}{v^+_{c,g}} + \frac{v_{c,o}}{v^-_{c,g}}\right). \tag{4.10}$$

The differential-mode transmission coefficient characterization is performed using two counter-phase generators with a 50 Ω internal impedance as shown in Fig. 4.27b. For the differential-mode characterization the effective internal impedance of the generator corresponds to the 100 Ω differential-mode characteristic impedance. The mixed-mode S-parameter differential-mode transmission coefficient $S_{sd21}$ is defined as the difference of the standard single-ended S-parameter transmission coefficient from the port $P_1$ to the port $P_3$ ($S_{31}$), and the transmission coefficient from the port $P_2$ to the port $P_3$ ($S_{32}$), divided by the square root of two [42]. The differential-mode transmission coefficient can also be calculated using voltages, where the output voltage $v_{d,o}$, the positive generator voltage $v^+_{d,g}$, and the negative generator voltage $v^-_{d,g}$ are used as follows:

$$S_{sd21} = \frac{1}{\sqrt{2}}(S_{31} - S_{32}) = \frac{1}{\sqrt{2}}\left(\frac{v_{d,o}}{v^+_{d,g}} - \frac{v_{d,o}}{v^-_{d,g}}\right). \tag{4.11}$$

The mixed-mode S-parameter definition of the common-mode rejection ratio $\mathrm{CMRR}_S$ is defined as the ratio of the magnitude of the differential-mode transmission coefficient $S_{sd21}$ and the common-mode transmission coefficient $S_{sc21}$ as follows [42]:

$$\mathrm{CMRR}_S = \frac{|S_{sd21}|}{|S_{sc21}|}. \tag{4.12}$$

### Laser common-mode rejection ratio measurements

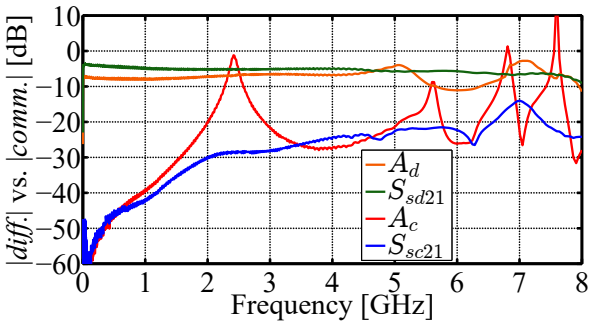
The voltage definition of the common-mode rejection ratio and the mixed-mode S-parameter definition of the common-mode rejection ratio are compared on the example of a laser diode. The VCSEL model #1 with the flexible PCB, shown in Fig. 3.1a, biased using the isolated power supply PoF bias module (Fig. 3.3a), is used as the example. The three-port standard single-ended S-parameters of the laser measured using the characterization setup shown in Fig. 3.23, which are discussed in Section 3.3, are used to compare the CMRR definitions.

The differential-mode voltage transfer function $A_d$, the common-mode voltage transfer function $A_c$, and the voltage common-mode rejection ratio $\mathrm{CMRR}_A$ are extracted from the measured three-port single-ended S-parameters of the laser, using the characterization setup shown in Fig. 4.26. The differential-mode mixed-mode S-parameter transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the mixed-mode S-parameter common-mode rejection ratio $\mathrm{CMRR}_S$ are extracted from the measured three-port single-ended S-parameters of the laser, using the characterization setup shown in Fig. 4.27. The generator voltages in both the voltage and the mixed-mode S-parameter characterization setup are set as follows:

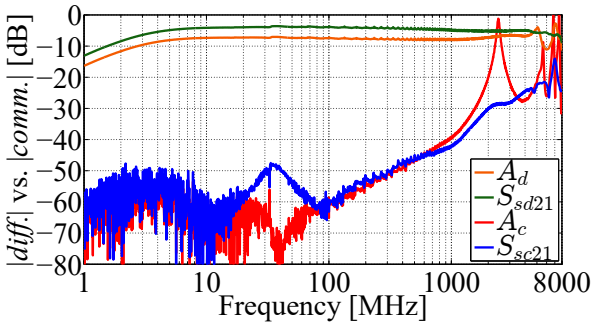
$$v_{c,g}^{+} = v_{c,g}^{-} = v_{d,g}^{+} = v_{d,g}^{-} = 1\ \mathrm{V}. \tag{4.13}$$

The magnitude of the differential-mode voltage transfer function $A_d$, the common-mode voltage transfer function $A_c$, and the voltage definition of the common-mode rejection ratio $\mathrm{CMRR}_A$ is compared to the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the mixed-mode S-parameter definition of the common-mode rejection ratio $\mathrm{CMRR}_S$ in Fig. 4.28. In the low frequency range up to 500 MHz there is good matching between the two differential-mode characteristics, taking into account the 3 dB difference between the differential voltage definitions in (4.8) and (4.11). In the frequency range above 5 GHz, there are multiple peaks and dips in the differential-mode voltage transfer function $A_d$, which are not present in the differential-mode transmission coefficient $S_{sd21}$. While the common-mode characteristic extracted using the mixed-mode S-parameters $S_{sc21}$ is relatively smooth, there are multiple resonances and antiresonances in the common-mode voltage transfer function $A_c$. The resonances and antiresonances in the common-mode voltage transfer function translate into the resonances and antiresonances in the voltage definition of the common-mode rejection ratio $\mathrm{CMRR}_A$, which are not present in the relatively smooth mixed-mode S-parameter common-mode rejection ratio $\mathrm{CMRR}_S$ characteristic.

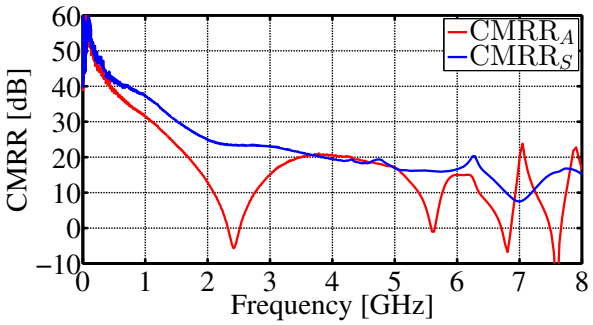
The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the laser at the balanced logical port (P1) are calculated using (2.70) and (2.71), respectively, as described in Section 2.1.4. The magnitude of the differential-mode and the common-mode input impedance of the laser is shown in Figs. 4.29a and 4.29b. The common-mode voltage at



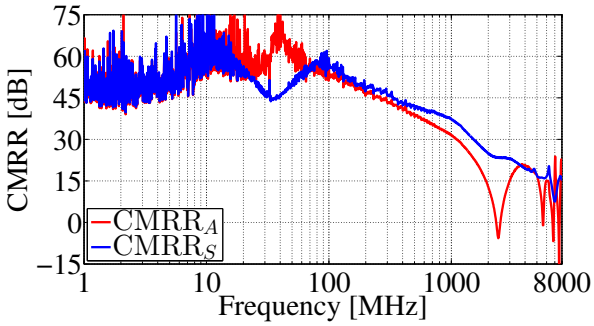

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.28:** Characteristics of the VCSEL model #1 in the package with the flexible PCB. The magnitude of the differential-mode voltage transfer function $A_d$, the common-mode voltage transfer function $A_c$, and the voltage definition of the common-mode rejection ratio $\mathrm{CMRR}_A$ is compared to the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the mixed-mode S-parameter definition of the common-mode rejection ratio $\mathrm{CMRR}_S$.

the generator $v_{c,g}$ and the differential-mode voltage at the generator $v_{d,g}$ in the characterization setup shown in Fig. 4.27 are defined as follows:

$$v_{c,g} = v_{c,g}^{+} + v_{c,g}^{-}, \tag{4.14}$$

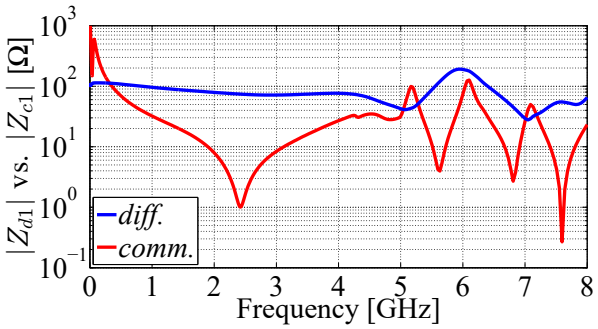
$$v_{d,g} = v_{d,g}^{+} - v_{d,g}^{-}. \tag{4.15}$$

The common-mode signal at the input of the laser $v_{c,i}$ and the differential-mode signal at the input of the laser $v_{d,i}$ in the characterization setup shown in Fig. 4.27 are defined as follows:

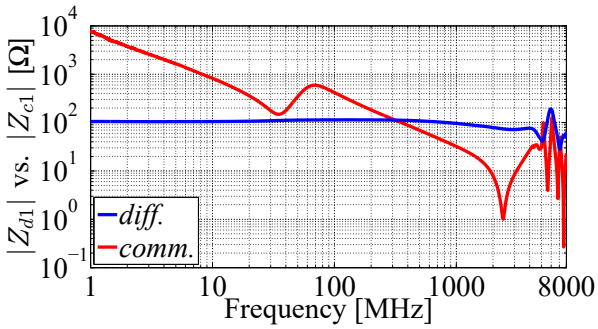
$$v_{c,i} = v_{c,i}^{+} + v_{c,i}^{-}, \tag{4.16}$$

$$v_{d,i} = v_{d,i}^{+} - v_{d,i}^{-}. \tag{4.17}$$

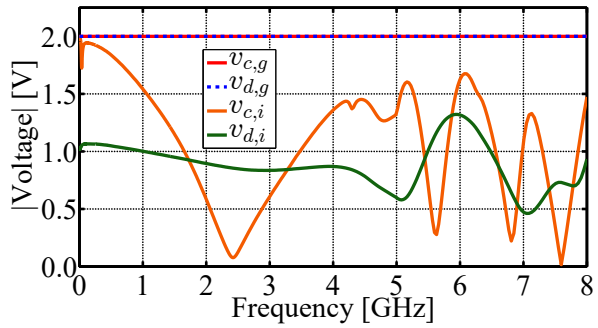
The common-mode and differential-mode voltages at the generator and at the input of the laser are compared in Figs. 4.29c and 4.29d. Given that the voltages of the individual generators are set to 1 V using (4.13), both the differential-mode voltage at the generator $v_{d,g}$ and the common-mode voltage at the generator $v_{c,g}$ is fixed to 2 V. The differential-mode input voltage $v_{d,i}$



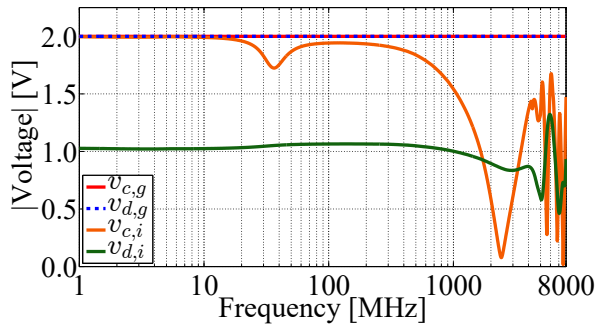

(a) Differential-mode and common-mode input impedance (linear frequency scale).




(b) Differential-mode and common-mode input impedance (logarithmic frequency scale).




(c) Generator and input voltage (linear frequency).




(d) Generator and input voltage (log. frequency).

**Figure 4.29:** Characteristics of the VCSEL model #1 in the package with the flexible PCB. The magnitude of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ are compared (top). The magnitude of the common-mode generator voltage $v_{c,g}$, the differential-mode generator voltage $v_{d,g}$, the common-mode input voltage $v_{c,i}$, and the differential-mode input voltage $v_{d,i}$ are compared (bottom).

is around 1 V. This is a result of the differential-mode input impedance $Z_{d1}$ of the laser that is matched to the 100 Ω generator differential-mode internal impedance. The dips and peaks in the differential-mode input impedance result in dips and peaks in the differential-mode input voltage. This is a result of the impedance matching between the generator and the laser, where the voltage is divided between the generator internal impedance and the input impedance of the laser. The changes in the differential-mode input voltage translate into changes in the differential-mode voltage transfer function $A_d$. On the other hand, these changes do not translate into the differential-mode transmission coefficient $S_{sd21}$, given that it is calculated relative to the generator voltages $v_{d,g}^{+}$ and $v_{d,g}^{-}$, which remain constant.

The same applies to the common-mode characterization. At low frequencies where the common-mode input impedance $Z_{c1}$ is significantly higher than the 25 Ω generator common-mode internal impedance, almost the entire generator voltage $v_{c,g}$ is applied at the input of the laser. At higher frequencies, where the common-mode input impedance drops, the common-mode input voltage $v_{c,i}$ drops as well. The resonances and antiresonances in the common-mode input impedance result in the resonances and antiresonances in the common-mode input voltage. The resonances and antiresonances in the common-mode input voltage translate into resonances

and antiresonances in the common-mode voltage transfer function $A_c$. On the other hand, these changes do not translate into the common-mode transmission coefficient $S_{sc21}$, which is relatively smooth, given that it is calculated relative to the generator voltages $v_{c,g}^{+}$ and $v_{c,g}^{-}$, which remain constant.

When performing the common-mode mixed-mode S-parameter analysis using the characterization setup shown in Fig. 4.27a, the common-mode component of the input voltage $v_{c,i,c}$ and the differential-mode component of the input voltage $v_{c,i,d}$ are defined as follows:

$$v_{c,i,c} = v_{c,i}^{+} + v_{c,i}^{-}, \tag{4.18}$$

$$v_{c,i,d} = v_{c,i}^{+} - v_{c,i}^{-}. \tag{4.19}$$

When performing the differential-mode mixed-mode S-parameter analysis using the characterization setup shown in Fig. 4.27b, the differential-mode component of the input voltage $v_{d,i,d}$ and the common-mode component of the input voltage $v_{d,i,c}$ are defined as follows:

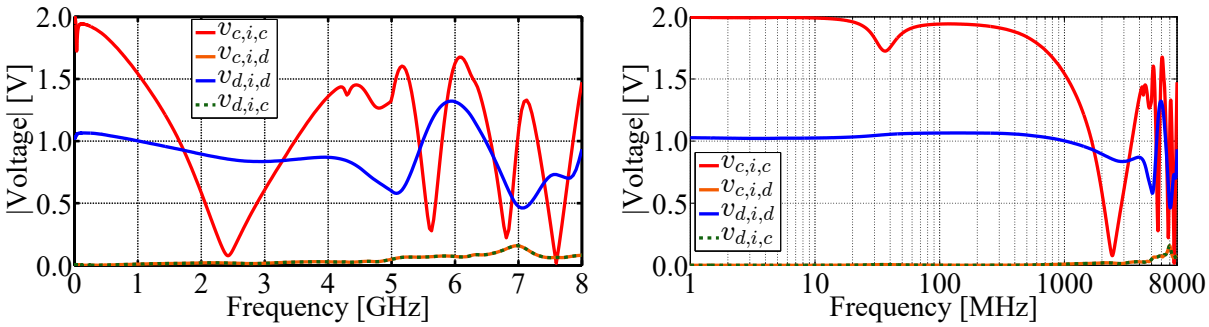
$$v_{d,i,d} = v_{d,i}^{+} - v_{d,i}^{-}, \tag{4.20}$$

$$v_{d,i,c} = v_{d,i}^{+} + v_{d,i}^{-}. \tag{4.21}$$

The input voltage components for the differential-mode and the common-mode characterization are displayed in Fig. 4.30. For the common-mode characterization, the common-mode signal component $v_{c,i,c}$ at low frequencies is around 2 V, because of the much higher input impedance of the laser compared to the generator internal impedance. At higher frequencies the common-mode voltage component decreases as a result of the changes in the common-mode input impedance $Z_{c1}$. For the common-mode characterization, a differential-mode input voltage component $v_{c,i,d}$ is present, which increases with frequency. At frequencies where there are sharp resonances in the common-mode voltage component, the differential-mode voltage component is comparable or even higher than the common-mode component.

For the differential-mode characterization, the differential-mode signal component $v_{d,i,d}$ at lower frequencies is around 1 V, because the differential impedance of the laser is matched to the generator internal impedance. At higher frequencies the differential-mode voltage component changes with the differential-mode input impedance $Z_{d1}$ frequency profile. For the differential-mode characterization, a common-mode input voltage component $v_{d,i,c}$ is present, which increases with frequency. At 7 GHz the common-mode component is approximately three times lower than the differential-mode component.

The differential-mode voltage component present in the common-mode characterization, and the common-mode voltage component present in the differential-mode characterization, are a result of the asymmetry of the device under test. Because of the different input impedance seen at the physical ports $P_1$ and $P_2$ of the laser, the voltage magnitude and phase are different




(a) Linear frequency scale.

(b) Logarithmic frequency scale.

**Figure 4.30:** Characteristics of the VCSEL model #1 in the package with the flexible PCB. The magnitude of the common-mode voltage component $v_{c,i,c}$ and the differential-mode voltage component $v_{c,i,d}$ in the common-mode characterization setup shown in Fig. 4.27a, and the differential-mode voltage component $v_{d,i,d}$ and the common-mode voltage component $v_{d,i,c}$ in the differential-mode characterization setup shown in Fig. 4.27b are compared.

between the two ports. For the characterized laser model, the differential-mode voltage component present in the common-mode characterization, and the common-mode voltage component present in the differential-mode characterization are equivalent.

The common-mode rejection ratio is a metric used to quantify the suppression of the common-mode signal relative to the differential-mode signal. The voltage definition of the CMRR assumes that the differential-mode and the common-mode generator voltage is applied directly at the input of the DUT, and does not take the impedance matching between the generator and the DUT into account. The same level of the differential-mode voltage and common-mode voltage at the input of the DUT is assumed, which does not change with frequency, as well as the same voltage magnitude and phase at both input ports.

The mixed-mode S-parameter definition of the CMRR assumes that the differential-mode and the common-mode voltage is applied using generators with a 50 Ω internal impedance, that is, the generators are matched to the 100 Ω differential-mode characteristic impedance, and the 25 Ω common-mode characteristic impedance, respectively. The generator voltage is divided between the generator internal impedance and the input impedance of the DUT. The lower the input impedance, the lower the input voltage. The different impedance matching for the differential-mode and the common-mode input signal affects the CMRR characteristic. The voltage levels at the two input ports are typically different, because of the asymmetry of the DUT.

For circuits with a high differential-mode and common-mode input impedance, the mixed-mode S-parameter CMRR definition matches the voltage CMRR definition. The voltage definition of the CMRR assumes a pure differential-mode and a pure common-mode stimulus at the input of the DUT. When performing the mixed-mode S-parameter CMRR characterization pure differential-mode and a pure common-mode stimulus are typically not applied at the input of the DUT. The voltage levels at the input of the DUT can be different for the differential-mode and

the common-mode measurement, because of the different common-mode and differential-mode input impedance matching. The differential-mode stimulus can contain a common-mode component alongside the differential-mode component, and the common-mode stimulus can contain a differential-mode component alongside the common-mode component. The mixed-mode S-parameter definition of the common-mode rejection ratio presents a practical usage scenario for the broadband circuits characterized in this thesis, where the realistic internal impedance of the RF generators is taken into account. For that reason, this is the CMRR definition which is consistently used.

### 4.4.2 Probe circuit impedance matching

The schematic of the probe circuit characterization structure is shown in Fig. 4.1. In the probe circuit, the attenuator and the laser are connected in cascade, as shown in Fig. 4.31. The attenuator circuit and the laser are characterized separately in Sections 2.3 and 3.3, respectively. The goal is to simulate the performance of the probe circuit by combining the characteristics of the attenuator and the laser, that are characterized separately.

#### Probe circuit simulation

A probe circuit structure that uses the attenuator #3 circuit design (Fig. 2.25c) and the VCSEL model #1 in the through-hole package (Fig. 3.1b) biased using the bias circuit #4 design, realized using ferrite beads (Fig. 3.21), is used as an example. The isolated power supply PoF bias module, shown in Fig. 3.3a, is used for biasing. Three-port S-parameters of the probe circuit characterization structure are measured. The measurements are performed using a two-port VNA [68], in the frequency range from 1 MHz to 8 GHz. The three-port standard single-ended S-parameters are converted to mixed-mode S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58). The performance of the probe circuit is simulated by using the char-

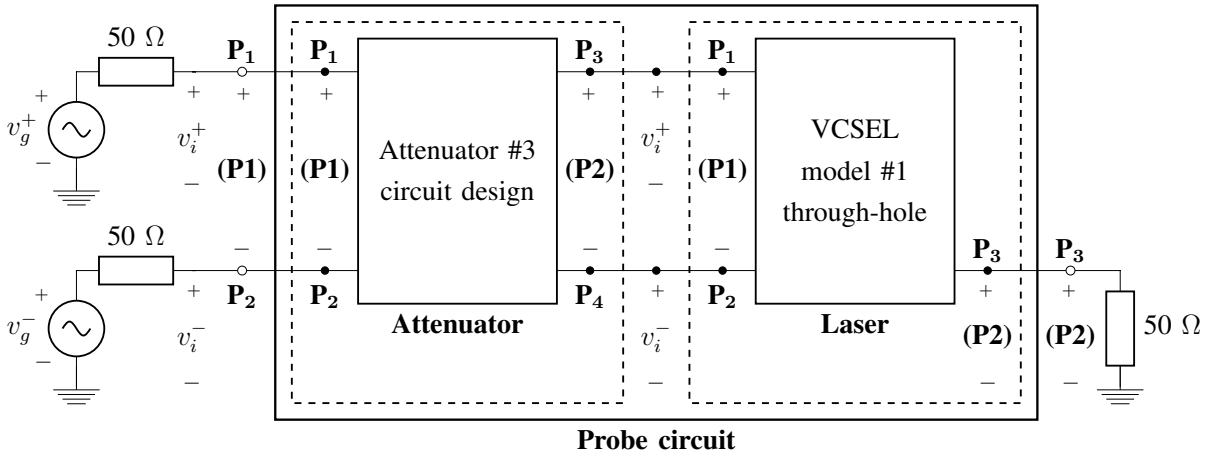
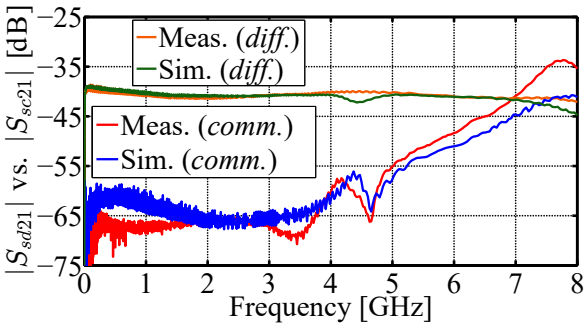


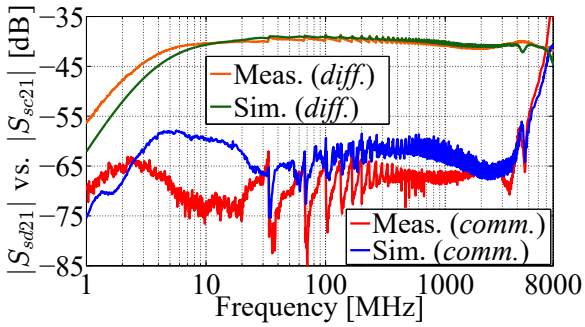

**Figure 4.31:** Probe circuit represented as a cascade connection of the attenuator circuit and the laser.

acteristics of the attenuator and the laser which are characterized separately. Four-port S-parameter electromagnetic simulation results of the attenuator circuit are used in the probe circuit simulation. The 500R attenuator configuration listed in Table 4.2 is used in both the attenuator structure and the probe circuit. Three-port S-parameter measurement results of the laser are used in the probe circuit simulation. By combining the characteristics of the probe circuit elements connected in cascade, a simulation of the probe circuit is performed.

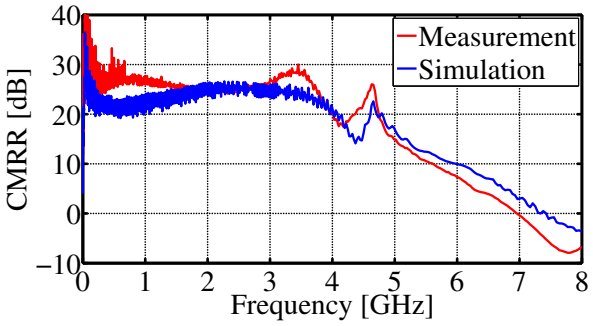
The probe circuit measurement and simulation results are compared in Fig. 4.32. The simulation results of the differential-mode transmission coefficient $S_{sd21}$ show good matching to the measurement results. There are dips in the simulation results around 4.5 GHz and above 7 GHz, which are not present in the measurement results. The simulation results match the general trend of the common-mode transmission coefficient $S_{sc21}$ measurements. There is a difference between the simulation and the measurement results of the common-mode signal transmission which varies between 3–10 dB. Taking into account the matching of the differential-mode and the common-mode signal transmission, the simulation results match the general trend of the common-mode rejection ratio measurements. The difference between the simulation and the measurement results varies between 3–5 dB. The simulated CMRR of the probe circuit remains above 20 dB up to 4.1 GHz. The fast drop in the CMRR at frequencies above



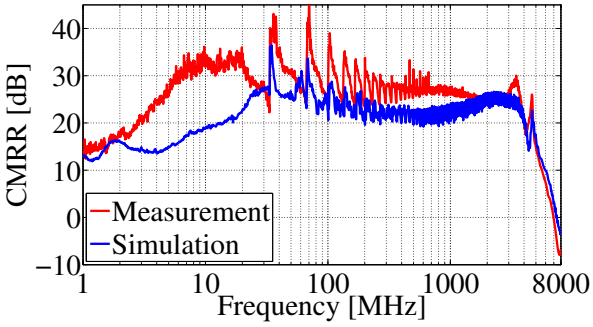

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).




(d) Common-mode rejection ratio (log. frequency).

**Figure 4.32:** Comparison of the measurement and the simulation of probe circuit shown in Fig. 4.31. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

4.5 GHz, that is observed for all probe circuit designs characterized in Sections 4.1 and 4.2, is replicated by the simulation results of the probe circuit shown in Fig. 4.31.

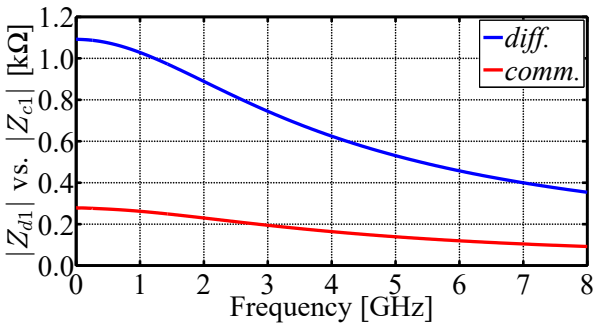
Some differences are expected between the simulation and the measurement results, because of the differences between the laser samples used, the components used in the attenuator circuit, the limitations of the attenuator EM simulations, as well as the coupling between the components of the probe circuit structure, which is not present when characterizing the parts individually. The differences between the simulation and the measurement results are mostly within the repeatability of the characteristics between the probe structures with the same design, which has been shown in Section 4.1.2.

**Probe circuit input voltage**

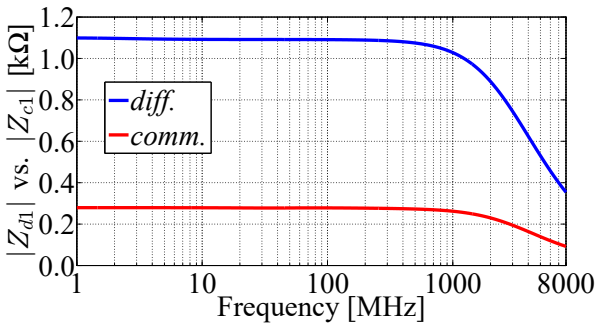
The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the simulated probe circuit at the balanced logical port (P1) are calculated using (2.70) and (2.71), respectively, as described in Section 2.1.4. The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the simulated probe circuit are shown in Figs. 4.33a and 4.33b. Both the differential-mode input impedance and the common-mode input impedance decrease with frequency, from the nominal value of 1092 Ω and 275 Ω, respectively. The impedances decrease to approximately 1/3 of the nominal value at 8 GHz, while the relative ratio between the two impedances remains around 4:1 in the entire frequency range. The input impedance of the probe circuit matches the input impedance of the attenuator structure very similarly, given that the input impedance of the laser, that is connected to the output of the attenuator, is matched to the 100 Ω differential-mode characteristic impedance.

The mixed-mode S-parameter probe circuit simulation setup shown in Fig. 4.31 is represented using the voltage sources $v_g^+$ and $v_g^-$ with a 50 Ω internal impedance, and the 50 Ω termination load. In-phase generators $v_{c,g}^+$ and $v_{c,g}^-$ are used for the common-mode simulation, as shown in Fig. 4.27a. Counter-phase generators $v_{d,g}^+$ and $v_{d,g}^-$ are used for the differential-mode simulation as shown in Fig. 4.27b. All generator voltages are set to 1 V using (4.13). The common-mode voltage at the generator $v_{c,g}$ and the differential-mode voltage at the generator $v_{d,g}$ in the probe circuit simulation setup are defined using (4.14) and (4.15), respectively. The common-mode voltage at the input balanced port (P1) of the probe circuit $v_{c,i}$ and the differential-mode voltage at the input of the probe circuit $v_{d,i}$ in the probe circuit simulation setup are defined using (4.16) and (4.17), respectively.

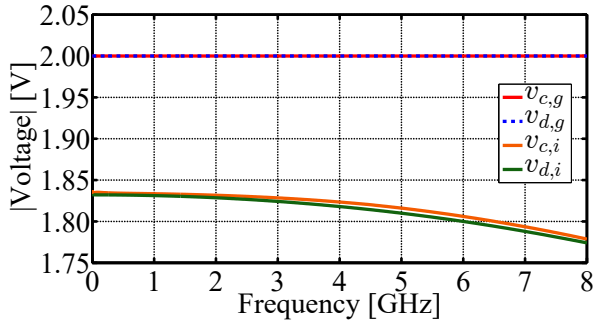
The common-mode and differential-mode voltages at the generator and at the input of the simulated probe circuit are compared in Figs. 4.33c and 4.33d. Given that the voltages of the individual generators are set to 1 V, both the differential-mode voltage at the generator $v_{d,g}$ and the common-mode voltage at the generator $v_{c,g}$ is fixed to 2 V. Both the differential-mode input voltage $v_{d,i}$ and the common-mode input voltage $v_{c,i}$ are close to the generator voltage of



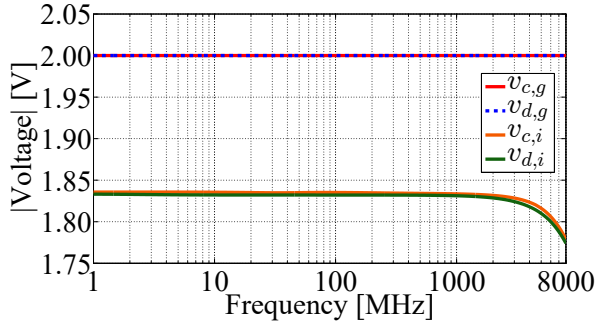

(a) Differential-mode and common-mode input impedance (linear frequency scale).




(b) Differential-mode and common-mode input impedance (logarithmic frequency scale).




(c) Generator and input voltage (linear frequency).




(d) Generator and input voltage (log. frequency).

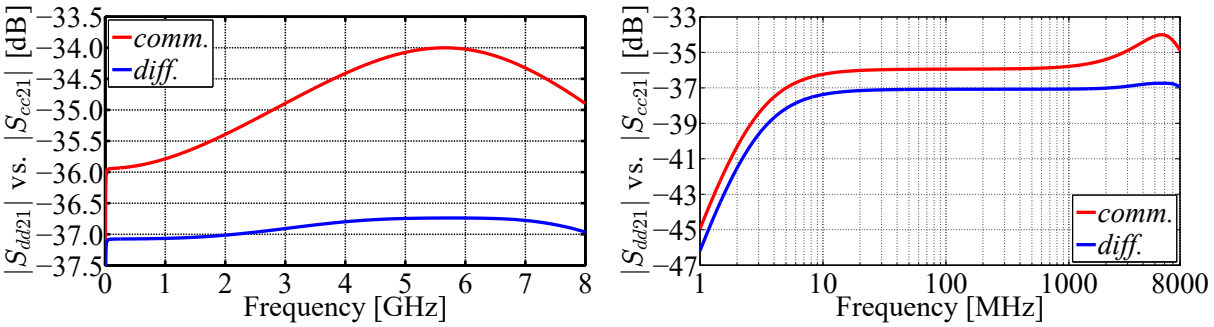
**Figure 4.33:** Probe circuit simulation results. The magnitude of the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ are compared (top). The magnitude of the common-mode generator voltage $v_{c,g}$, the differential-mode generator voltage $v_{d,g}$, the common-mode input voltage $v_{c,i}$, and the differential-mode input voltage $v_{d,i}$ are compared (bottom).

2 V, given that both the differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the probe circuit are significantly higher than the generator differential-mode internal impedance of 100 Ω, and the generator common-mode internal impedance of 25 Ω. Both input voltages slightly decrease with frequency given that both the differential-mode and the common-mode input impedance decrease with frequency, while the internal impedance of the generator remains constant. Despite the common-mode input impedance being lower, the common-mode input voltage is slightly higher than the differential-mode input voltage, because the common-mode input impedance is higher relative to the 25 Ω generator common-mode internal impedance, than the differential-mode input impedance is relative to the 100 Ω generator differential-mode internal impedance.

### Attenuator signal transmission

EM simulations of the attenuator #3 circuit design (Fig. 2.25c) are used in the probe circuit simulation setup shown in Fig. 4.31. The mixed-mode S-parameters of the attenuator are calculated from the four-port standard single-ended S-parameter EM simulation results using (2.31)–(2.46), and are shown in Fig. 4.34. Both the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ are very stable over

the entire frequency range. The common-mode transmission coefficient is slightly higher than the differential-mode transmission coefficient, meaning that the common-mode signal is less attenuated that the differential-mode signal. The lower cutoff frequency is a result of the DC block capacitors in the attenuator circuit. As discussed in Section 2.3.1, the mode conversion in the attenuator circuit EM simulations is limited. The mode conversion transmission coefficients $S_{dc21}$ and $S_{cd21}$ extracted from the simulation are significantly lower than it would be expected in practice. For this reason, the mode conversion in the attenuator circuit is not taken into account in this analysis.




(a) Linear frequency scale.

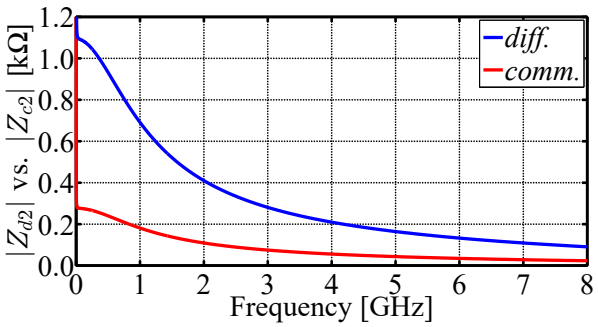
(b) Logarithmic frequency scale.

**Figure 4.34:** EM simulations of the attenuator #3 circuit design used in the probe circuit simulation. The magnitude of the differential-to-differential transmission coefficient $S_{dd21}$ and the common-to-common transmission coefficient $S_{cc21}$ are compared.

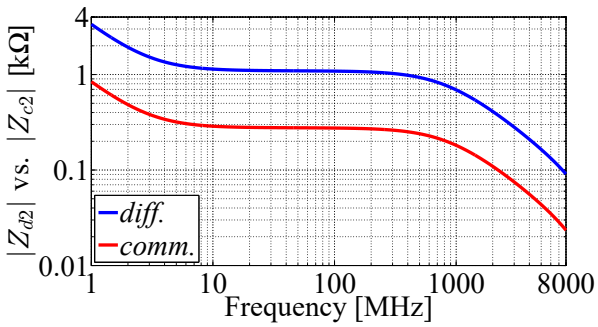
### Impedance matching between the attenuator and the laser

The differential-mode output impedance $Z_{d2}$ and the common-mode output impedance $Z_{c2}$ of the attenuator (Fig. 2.25c) at the balanced logical port (P2) are calculated using (2.70) and (2.71), respectively, adjusted for the port (P2). The differential-mode output impedance $Z_{d2}$ and the common-mode output impedance $Z_{c2}$ of the attenuator circuit are shown in Figs. 4.35a and 4.35b. Both the differential-mode output impedance and the common-mode output impedance decrease with frequency, from the nominal value of 1092 Ω and 275 Ω, respectively. The impedances decrease to about 1/12 of the nominal value at 8 GHz, while the relative ratio between the two impedances remains around 4:1 in the entire frequency range. The output impedance of the attenuator circuit is lower than the input impedance in most of the frequency range. The high output impedance at low frequencies is a result of the DC block capacitors in the attenuator circuit.

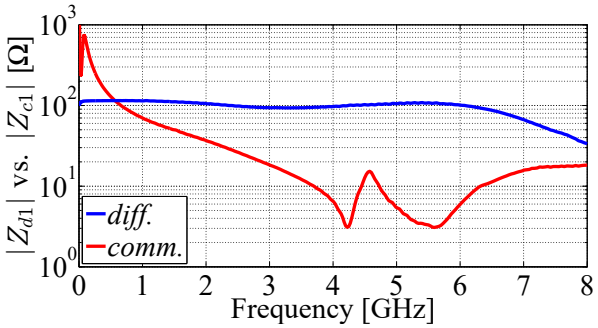
The S-parameters of the VCSEL model #1 in the through-hole package (Fig. 3.1b) biased using the bias circuit #4 design, realized using ferrite beads (Fig. 3.21), are measured using the characterization setup shown in Fig. 3.23. The measurements are performed in the frequency range from 1 MHz to 8 GHz, using a two-port VNA [68]. The three-port S-parameter measurement results of the laser are used in the probe circuit simulation setup shown in Fig. 4.31.



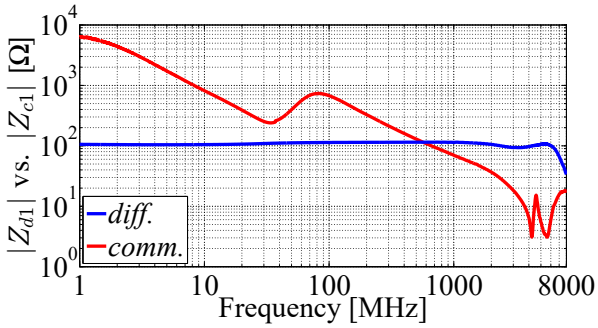

(a) Attenuator differential-mode and common-mode output impedance (linear frequency).




(b) Attenuator differential-mode and common-mode output impedance (log. frequency).




(c) Laser differential-mode and common-mode input impedance (linear frequency scale).




(d) Laser differential-mode and common-mode input impedance (logarithmic frequency scale).

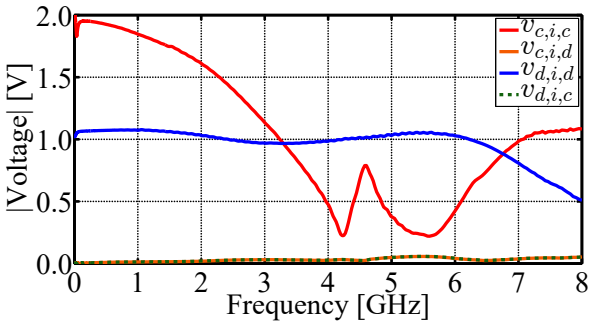
**Figure 4.35:** Comparison of the EM simulations of the attenuator #3 circuit design and the measurements of the VCSEL model #1 in the through-hole package used in the probe circuit simulation. The magnitude of the attenuator differential-mode output impedance $Z_{d2}$ and the common-mode output impedance $Z_{c2}$ are compared (top). The magnitude of the laser differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ are compared (bottom).

The mixed-mode S-parameters of the laser are calculated from the measured three-port standard single-ended S-parameters using (2.49)–(2.57), and the CMRR is calculated using (2.58). The differential-mode input impedance $Z_{d1}$ and the common-mode input impedance $Z_{c1}$ of the laser at the balanced logical port (P1) are calculated using (2.70) and (2.71), respectively, as described in Section 2.1.4. The magnitude of the differential-mode and the common-mode input impedance of the laser is shown in Figs. 4.35c and 4.35d. The differential-mode input impedance of the laser is matched to the 100 Ω differential-mode internal impedance of the generator. At frequencies above 6.1 GHz, the differential-mode input impedance drops off a bit. The common-mode input impedance of the laser is very high at lower frequencies and drops gradually, with the minimum around 4.2 GHz, followed by a resonance and an antiresonance. The common-mode input impedance increases for frequencies above 5.6 GHz, but remains lower than the differential-mode input impedance.

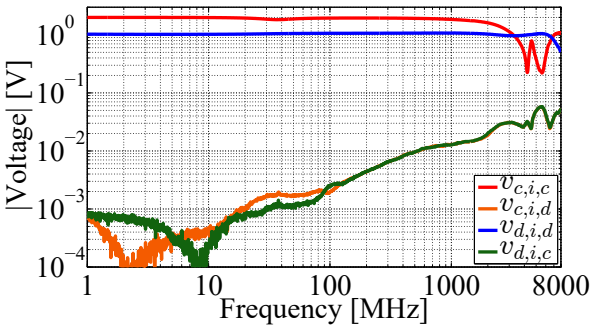
### Laser input voltage

The voltage components at the input balanced logical port (P1) of the laser, for the differential-mode and common-mode characterization of the laser by itself are displayed in Figs. 4.36a and 4.36b. The voltage components at the input of the laser extracted from the probe circuit simulation (Fig. 4.31), where the laser is connected in cascade with the attenuator circuit, for the differential-mode and common-mode characterization are shown in Figs. 4.36c and 4.36d. The common-mode input voltage component $v_{c,i,c}$ and the differential-mode input voltage component $v_{c,i,d}$ for the common-mode characterization are defined using (4.18) and (4.19), respectively. The differential-mode input voltage component $v_{d,i,d}$ and the common-mode input voltage component $v_{d,i,c}$ for the differential-mode characterization are defined using (4.20) and (4.21), respectively.

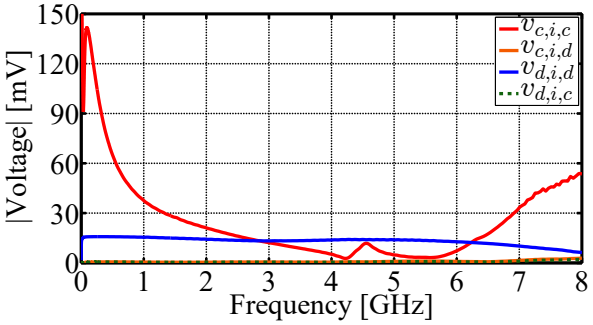
When the laser is characterized by itself, the differential-mode input voltage $v_{d,i,d}$ follows the trend of the differential-mode input impedance $Z_{d1}$, while the common-mode input volt-



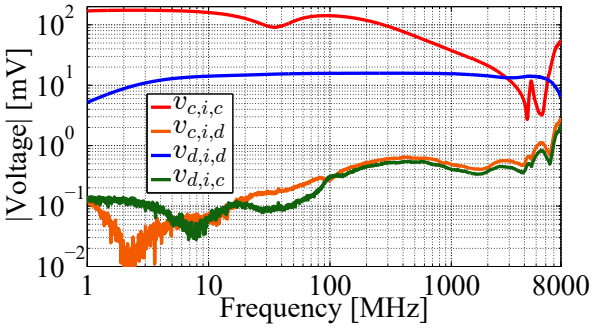

(a) Input voltage of the laser characterized by itself (linear frequency scale).




(b) Input voltage of the laser characterized by itself (logarithmic frequency scale).




(c) Input voltage of the laser used in the cascade connection with the attenuator in the probe circuit simulation (linear frequency scale).




(d) Input voltage of the laser used in the cascade connection with the attenuator in the probe circuit simulation (logarithmic frequency scale).

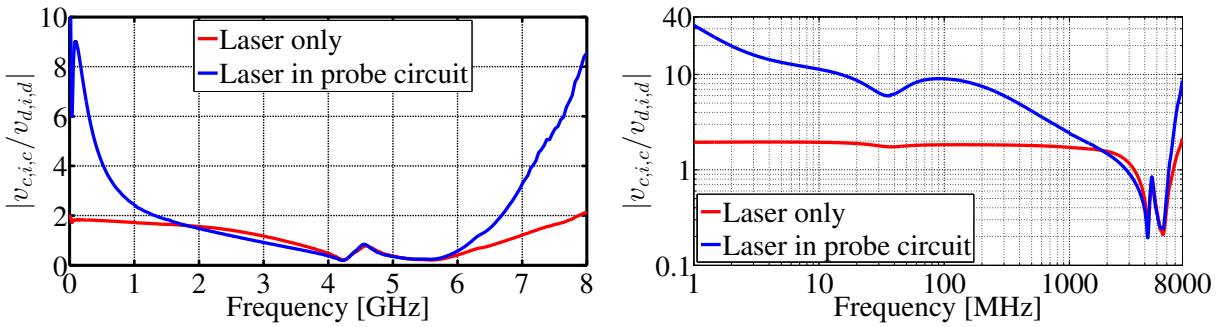
**Figure 4.36:** Comparison of the voltage at the input of the VCSEL model #1 in the through-hole package extracted from the measurements of the laser by itself (top), and extracted from the probe circuit simulation using the cascade connection of the attenuator and the laser (bottom). The magnitude of the common-mode voltage component $v_{c,i,c}$ and the differential-mode voltage component $v_{c,i,d}$ in the common-mode characterization, and the differential-mode voltage component $v_{d,i,d}$ and the common-mode voltage component $v_{d,i,c}$ in the differential-mode characterization are compared.

age $v_{c,i,c}$ follows the trend of the common-mode input impedance $Z_{c1}$ of the laser shown in Figs. 4.35c and 4.35d. For the differential-mode characterization, the differential-mode signal component $v_{d,i,d}$ is around 1 V, because the differential-mode input impedance of the laser is matched to the 100 Ω generator differential-mode internal impedance. At frequencies above 6.1 GHz, the differential-mode voltage component drops with the differential-mode input impedance. For the common-mode characterization, the common-mode voltage component $v_{c,i,c}$ at low frequencies is around 2 V, because of the much higher common-mode input impedance of the laser compared to the 25 Ω generator common-mode internal impedance. At higher frequencies the common-mode voltage component decreases as a result of the changes in the common-mode input impedance. Due to the asymmetry of the laser, a differential-mode voltage component $v_{c,i,d}$ is present in the common-mode characterization, and a common-mode voltage component $v_{d,i,c}$ is present in the differential-mode characterization. These components slowly increase with frequency.

When the laser is used as a part of the probe circuit simulation in the characterization setup shown in Fig. 4.31, the laser is connected in cascade with the attenuator circuit. The differential-mode and the common-mode voltage at the input of the laser are dependent on the attenuation of the differential-mode and the common-mode signal in the attenuator shown in Fig. 4.34, and the impedance matching between the output impedance of the attenuator and the input impedance of the laser shown in Fig. 4.35. More common-mode signal passes through the attenuator than the differential-mode signal. The differential-mode voltage $v_{d,i}$ and the common-mode voltage $v_{c,i}$ at the input of the probe circuit, shown in Figs. 4.33c and 4.33d, are very similar and decrease very slightly with frequency, so this does not have a significant impact on the laser input voltage.

The common-mode output impedance $Z_{c2}$ of the attenuator drops gradually with frequency, while the common-mode input impedance $Z_{c1}$ of the laser drops quickly up to 4.2 GHz, but starts increasing again after 5.6 GHz. For the common-mode characterization the common-mode input voltage component $v_{c,i,c}$ roughly follows the trend of the common-mode input impedance of the laser. However, compared to the nominal case when the laser is characterized by itself, the common-mode input voltage $v_{c,i,c}$ is higher relative to the differential-mode input voltage $v_{d,i,d}$ in the lower frequency range up to 1.8 GHz and in the high frequency range above 5.5 GHz, while it is lower in the frequency range between 1.8 GHz and 4.2 GHz, as shown in Fig. 4.37.

The differential-mode output impedance $Z_{d2}$ of the attenuator drops gradually with frequency, while the differential-mode input impedance $Z_{d1}$ of the laser remains almost constant up to 6.1 GHz. This means that more differential-mode voltage $v_{d,i,d}$ is applied at the input of the laser at lower frequencies, compared to the nominal case when the laser is characterized by itself. Although the mode conversion extracted from the attenuator EM simulation is limited compared to a realistic circuit, the differential-mode voltage component introduced by the




(a) Linear frequency scale.

(b) Logarithmic frequency scale.

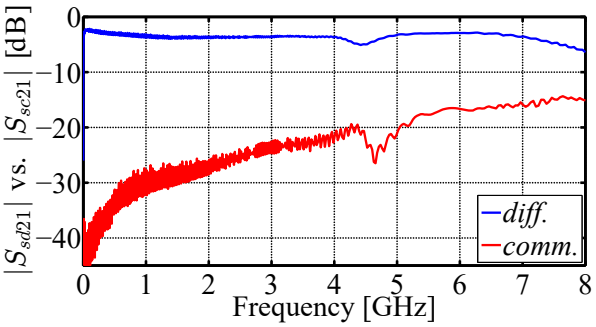
**Figure 4.37:** Comparison of the voltage at the input of the VCSEL model #1 in the through-hole package extracted from the measurements of the laser by itself, and extracted from the probe circuit simulation using the cascade connection of the attenuator and the laser. The magnitude of the ratio of the common-mode voltage component in the common-mode characterization $v_{c,i,c}$ and the differential-mode voltage component in the differential-mode characterization $v_{d,i,d}$ is compared.

common-mode characterization $v_{c,i,d}$ is higher relative to the common-mode voltage component introduced by the differential-mode characterization $v_{d,i,c}$, compared to the case when the laser is characterized by itself, as shown in Fig. 4.36.

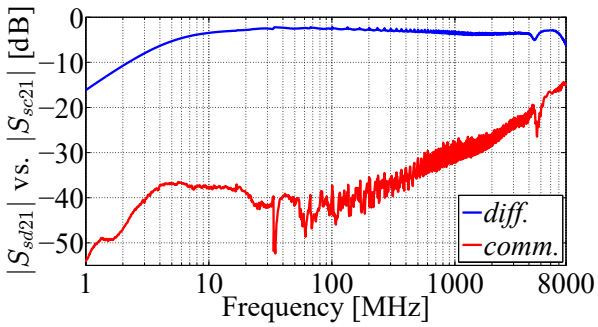
### Laser signal transmission

The mixed-mode S-parameter measurements of the laser used in the probe circuit simulation are shown in Fig. 4.38. The differential-mode transmission coefficient $S_{sd21}$ is relatively stable over the entire frequency range. At frequencies above 6.6 GHz, there is a slight drop in the differential-mode signal level. The drop in the differential-mode signal transmission at low frequencies is a result of the lower cutoff frequency of the photodetector model used to perform the measurements [69]. The common-mode transmission coefficient $S_{sc21}$ increases gradually with frequency over the measurement frequency range. The common-mode rejection ratio of the laser drops gradually with frequency. It is above 30 dB up to 600 MHz and above 20 dB up to 3.1 GHz. It should be noted that the sudden drop in the CMRR above 4.5 GHz that is observed in all probe circuit designs characterized in Sections 4.1 and 4.2 is not present in the CMRR characteristic of the laser, nor the differential-mode and the common-mode characteristic. The same is true for the attenuator mixed-mode S-parameter characteristics shown in Fig. 4.34.

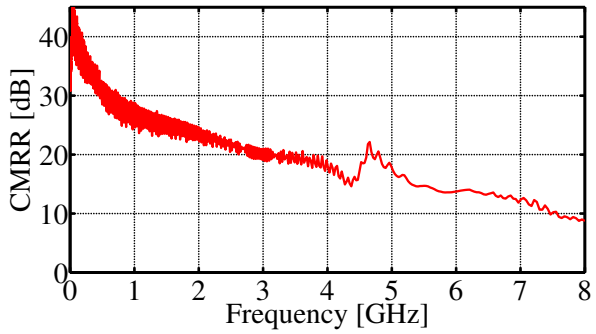
The high frequency drop in the CMRR that is observed in the probe circuit measurement and simulation results, shown in Fig. 4.32, is a result of the interaction between the attenuator circuit and the laser. Taking into account the differential-mode and common-mode signal propagation through the attenuator circuit, due to the impedance matching between the attenuator circuit and the laser, the common-mode voltage at the input of the laser increases significantly in the frequency range up to 1.8 GHz and above 4.2 GHz, relative to the differential-mode voltage, as shown in Fig. 4.37. Because of the higher common-mode signal relative to the differential-mode



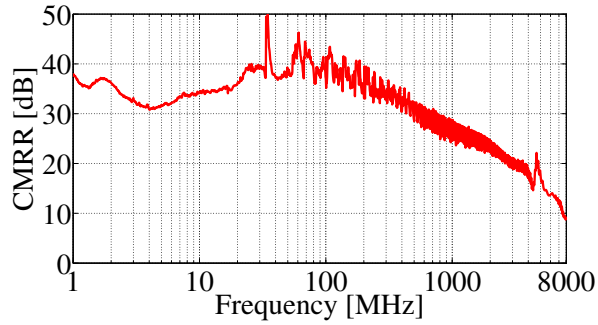

(a) Differential-mode and common-mode signal transmission (linear frequency scale).




(b) Differential-mode and common-mode signal transmission (logarithmic frequency scale).




(c) Common-mode rejection ratio (lin. frequency).

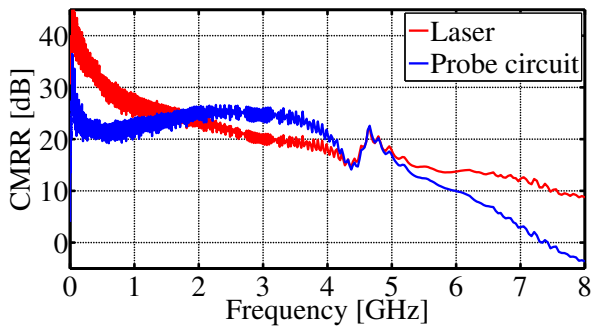



(d) Common-mode rejection ratio (log. frequency).

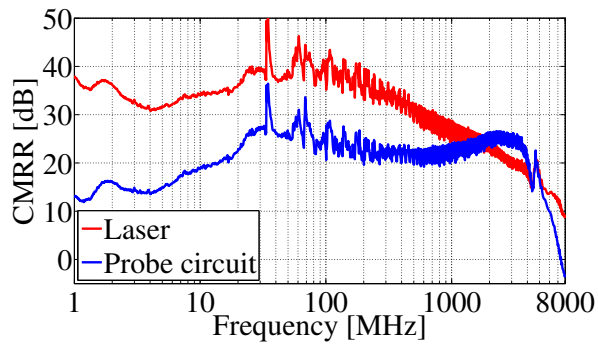
**Figure 4.38:** Measurements of the VCSEL model #1 in the through-hole package used in the probe circuit simulation. The magnitude of the differential-mode transmission coefficient $S_{sd21}$, the common-mode transmission coefficient $S_{sc21}$, and the common-mode rejection ratio (CMRR) are compared.

signal at the input of the laser, compared to the nominal case when the laser is characterized by itself, the CMRR of the probe circuit is degraded. The probe circuit CMRR is decreased in the frequency range up to 1.7 GHz and above 4.9 GHz. In turn, in the frequency range between 1.9 GHz and 4.3 GHz, where the common-mode signal is more attenuated than the differential-mode signal relative to the nominal case, the simulated probe circuit has a higher CMRR than the laser characterized by itself, as shown in Fig. 4.39.

The impedance matching between the attenuator circuit and the laser is the cause of the




(a) Linear frequency scale.




(b) Logarithmic frequency scale.

**Figure 4.39:** Comparison of the common-mode rejection ratio of the probe circuit simulation and the measurement of the VCSEL model #1 in the through-hole package used in the probe circuit simulation.

typical characteristics shared by all probe circuit designs explored in Sections 4.1 and 4.2. In particular, the higher common-mode laser input voltage at lower frequencies, relative to the differential-mode input voltage, when compared to the characterization of the laser by itself, results in a relatively stable CMRR up to around 4 GHz. The typically higher CMRR of the laser at lower frequencies is flattened out by the higher common-mode voltage at the input of the laser, that is connected in cascade with the attenuator. Using the same mechanism, the increasing common-mode input voltage at high frequencies, relative to the differential-mode input voltage, when compared to the characterization of the laser by itself, accelerates the rate at which the CMRR drops at frequencies above 4.5 GHz, resulting in a steep slope.

This demonstrates an important mechanism of the common-mode signal propagation through the probe circuit, where not only the suppression of the common-mode signal and the mode conversion in each part of the probe circuit is important, but also the transmission of the differential-mode and the common-mode signal between the attenuator and the laser. While the CMRR of the probe circuit is primarily dependent on the CMRR of the laser used for the electro-optical conversion of the signal, the CMRR of the system can be increased above the CMRR of the laser, by optimizing the attenuator circuit design. The CMRR of the system can be improved by controlling the output impedance of the attenuator and the input impedance of the laser, where the portion of the common-mode signal that is transmitted to the laser should be minimized, while achieving a high transmission of the differential-mode signal.

### 4.4.3 Impact of circuit asymmetry on the common-mode rejection ratio

The symmetry of a differential circuit has an impact on the common-mode rejection ratio, as shown in Section 3.4. In particular, the greater the asymmetry between the two port-to-ground paths, the higher the unwanted common-mode signal and the lower the CMRR. In addition to asymmetry of the two ground paths, the impedance magnitude also has an impact on the CMRR that can be achieved. The impact of the ground path impedance on the CMRR in terms of the impedance magnitude, phase, and asymmetry between the two ground paths is explored. A differential signal transmission path shown in Fig. 4.40 is used as the test case. The physical ports $P_1$ and $P_2$ form the input balanced logical port (P1), while the physical ports $P_3$ and $P_4$ form the output balanced logical port (P2). The impedance $Z_1$ is the impedance of the path from the port $P_1$ towards the ground, while the impedance $Z_2$ is the impedance of the path from the port $P_2$ towards the ground. The characteristic impedance of the system is 50 Ω, and the termination loads connected to the ports $P_3$ and $P_4$ form a matched 100 Ω load for the differential-mode signal analysis.

A circuit simulation of the differential signal transmission path characterization setup is performed. The mixed-mode S-parameters are calculated from the four-port standard single-ended S-parameter simulation results using (2.31)–(2.46). The differential-to-differential transmis-

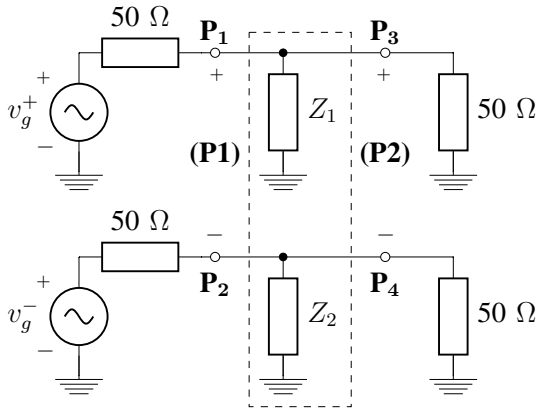



**Figure 4.40:** Schematic of the differential signal transmission path characterization setup used to evaluate the impact of the port-to-ground path impedance asymmetry on the common-mode rejection ratio.

sion coefficient $S_{dd21}$ and the common-to-differential transmission coefficient $S_{dc21}$ are used to evaluate the impact of the ground path impedance asymmetry on the transmission of the differential-mode signal to the differential load, and the conversion of the common-mode signal to a differential-mode signal, respectively. The common-mode rejection ratio is defined as the ratio between the differential-to-differential transmission coefficient and the common-to-differential transmission coefficient using (2.47).

The port-to-ground impedances $Z_1$ and $Z_2$ are defined as follows:

$$Z_1 = |Z_1| \angle \varphi_1 = Z \angle 0^\circ, \tag{4.22}$$

$$Z_2 = |Z_2| \angle \varphi_2 = k \cdot Z \angle \varphi, \tag{4.23}$$

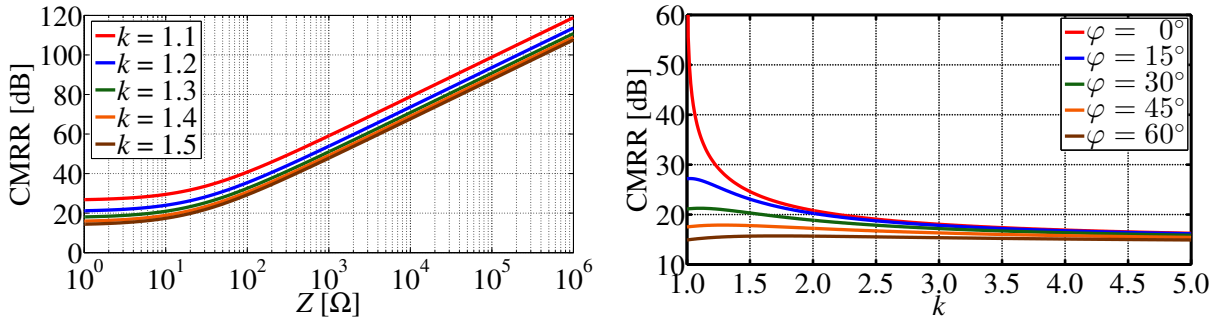
where $Z$ is the nominal impedance magnitude of the ground path, $k$ is the impedance magnitude imbalance between the two ground paths:

$$k = \frac{|Z_2|}{|Z_1|}, \tag{4.24}$$

and $\varphi$ is the impedance phase imbalance between the two ground paths:

$$\varphi = \varphi_2 - \varphi_1. \tag{4.25}$$

The impact of the port-to-ground path impedance magnitude $Z$ on the CMRR, depending on the impedance magnitude imbalance $k$, is shown in Fig. 4.41a. The greater the impedance asymmetry, the lower the CMRR that is achieved. The higher the impedance magnitude, the higher the CMRR that is achieved. For the nominal impedance magnitude of $Z = 50\ \Omega$ and the phase imbalance $\varphi = 0^\circ$, the CMRR levels listed in Table 4.5 are achieved. While the absolute increase in the CMRR is similar regardless of the impedance magnitude, for low impedance magnitudes the relative increase in CMRR is much more significant. This demonstrates that if




(a) Impedance magnitude $Z$ and impedance magnitude imbalance $k$ ($\varphi = 0°$).

(b) Impedance magnitude imbalance $k$ and impedance phase imbalance $\varphi$ ($Z = 50\ \Omega$).

**Figure 4.41:** Simulation results of the impact of the ground path impedance asymmetry on the CMRR of the differential signal transmission path characterization setup shown in Fig. 4.40.

the ground path impedance is significantly large, a high CMRR can be achieved regardless of the ground path asymmetry. For lower impedances, significant improvements can be made to the CMRR by reducing the ground path asymmetry.

**Table 4.5:** Impact of the impedance magnitude imbalance $k$ on the CMRR simulation results of the differential signal transmission path characterization setup shown in Fig. 4.40 ($Z = 50\ \Omega$, $\varphi = 0°$).

| $k$ | 1.1 | 1.2 | 1.3 | 1.4 | 1.5 |
|---|---|---|---|---|---|
| CMRR | 36.2 dB | 30.8 dB | 27.9 dB | 26.0 dB | 24.6 dB |

The impact of the port-to-ground path impedance magnitude imbalance $k$ on the CMRR, depending on the impedance phase imbalance $\varphi$, is shown in Fig. 4.41b. By increasing either the magnitude or the phase imbalance, the CMRR drops quickly. For higher magnitude and phase imbalance levels, the CMRR stabilizes and additional increases in the magnitude and phase imbalance have a relatively small impact on the further drop in the CMRR.

As it is shown, the common-mode rejection ratio of a differential circuit is primarily limited by the impedance magnitude of the two port-to-ground signal paths. The higher the ground path impedance relative to the differential impedance of the circuit, the higher the CMRR that can be achieved. The CMRR is also very sensitive to any magnitude and phase imbalance between the two ground paths. The impact of the ground path impedance asymmetry is very significant if the impedance magnitude of the ground path is relatively low.

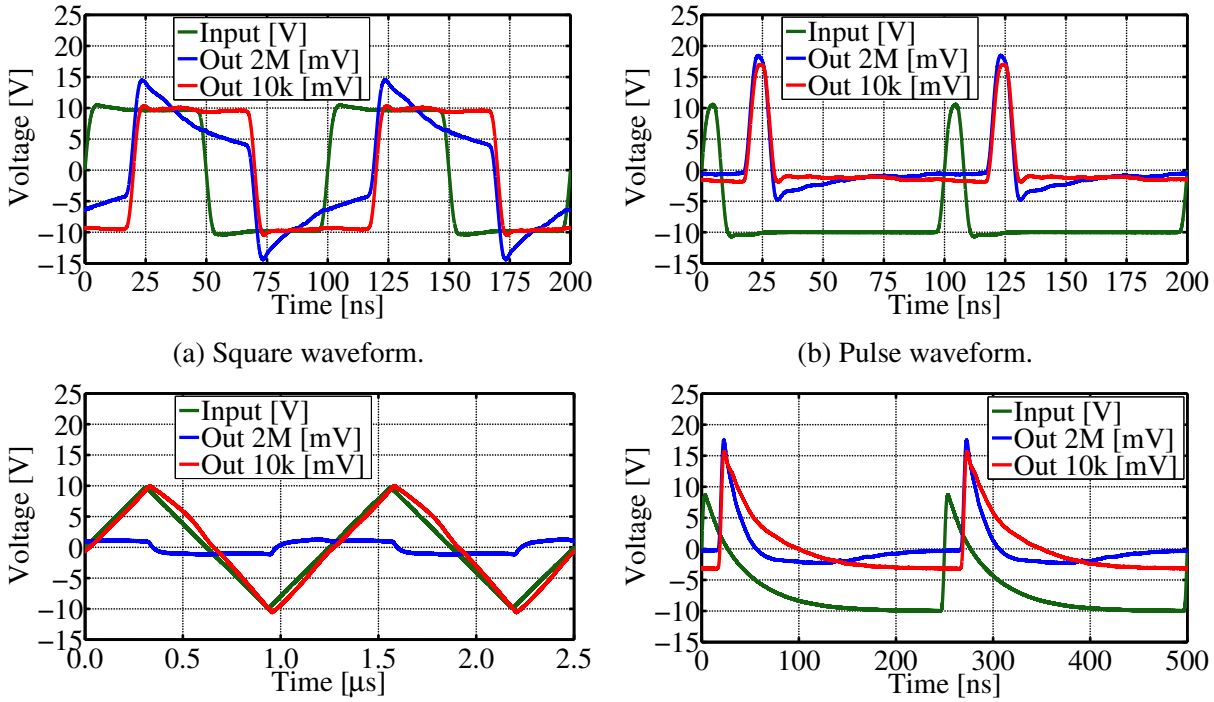
## 4.5 Probe time domain measurements

The developed probe circuit is evaluated by performing time domain measurements. The connected-ground probe shown in Fig. 4.7 is used. The probe is biased using the isolated power supply PoF bias module, shown in Fig. 3.3a. Several characteristic waveforms are measured. The waveforms are generated using an arbitrary waveform generator [130]. For the reference measurement, the waveform generator is connected directly to a high frequency oscilloscope [131]. The oscilloscope port is terminated with a 1 MΩ impedance. In this way, the input signal of the probe is measured. For the probe measurement, the waveform generator is connected to the input of the connected-ground probe. The photodetector output is connected to an oscilloscope port terminated with a 50 Ω impedance. The waveforms measured using the electro-optical probe are compared to the waveforms generated by the arbitrary waveform generator.

Measurements are performed using two photodetector models with a different lower cutoff frequency. The first photodetector model has a 2 MHz lower cutoff frequency [69], and is used for all the electro-optical measurements presented in the previous chapters of this thesis. The second photodetector model has a 10 kHz lower cutoff frequency [132]. The impact of the photodetector lower cutoff frequency on the time domain waveform measurements is explored.

Four time domain waveforms are measured. The first waveform is a square waveform with a 10 MHz frequency and a 50% duty cycle. The second waveform is a pulse waveform with a rise time and fall time of 3.3 ns, a pulse width of 8.0 ns, and a frequency of 10 MHz. The third waveform is a triangle waveform with a frequency of 800 kHz. The fourth waveform is an exponential fall function with a frequency of 4 MHz. All four generated waveforms have an amplitude of 10 V (20 $V_{PP}$), when connected to a high impedance load. Due to the relatively low signal amplitude of 10 V, compared to the maximum input signal amplitude of the probe of 100 V, the signal-to-noise ratio of the measurements is limited. Measurement averaging is used in order to reduce the effective noise level and extract the measured waveforms more clearly, with 500 samples being averaged.

The time domain measurement results are shown in Fig. 4.42. Due to the relatively high lower cutoff frequency of the 2 MHz photodetector, all the measured voltage waveforms are distorted. These distortions are particularly noticeable in the lower frequency components, which are below the lower cutoff frequency of the photodetector, and are significantly more attenuated than the higher frequency signal components. The triangle signal is almost completely attenuated, because the low frequency components present in the signal are below the lower cutoff frequency of the photodetector and are thus filtered. In the square waveform, the steady high and low signal state are not properly reproduced, because these low frequency components are missing from the output signal. On the other hand, the fast signal level changes are reproduced accurately. In the pulse and the exponential fall waveforms, the lack of low frequency




(a) Square waveform.

(b) Pulse waveform.

(c) Triangle waveform.

(d) Exponential fall waveform.

**Figure 4.42:** Comparison of the time domain measurements of different voltage waveforms measured using the connected-ground probe. The input voltage waveform, the output of the photodetector with a 2 MHz lower cutoff frequency and the output of the photodetector with a 10 kHz lower cutoff frequency are compared.

components is manifested in the form of dips in the waveform as the signal levels off.

Compared to the measurements performed using the photodetector with a lower cutoff frequency of 2 MHz, in the time domain measurements performed using the photodetector with a lower cutoff frequency of 10 kHz [132], no significant signal distortions are observable. The measured waveforms closely match the input waveforms. They are attenuated by the voltage attenuation ratio of the connected-ground probe with the 1000R attenuator configuration listed in Table 4.2. Additionally, the probe output port is terminated with a 50 Ω impedance, while the input reference signal port is terminated with a 1 MΩ impedance, effectively doubling the voltage amplitude. The SNR of the output signal is also lower compared to the input signal, due to the attenuation of the signal and the noise introduced by the photodetector.

It is shown that the characteristics of the photodetector model used have a significant impact on the performance of the electro-optical measurement system, both in terms of the lower cutoff frequency and the SNR. In order to accurately reproduce the measured voltage waveforms, using a photodetector with a sufficiently low lower cutoff frequency is required.

## 4.6 Summary

The probe circuit of the electro-optical differential voltage measurement system consists of three main parts: the attenuator, the laser and the bias circuit. The initial version of the probe circuit design is implemented on a floating wafer probe. Different probe circuit designs are explored, and the changes made to the design of the attenuator circuit, the laser diode layout, and the bias circuit in the previous chapters, are implemented in the probe circuit. Probe circuits with different attenuation ratios are characterized. In general, the lower the attenuation ratio, the higher the CMRR that can be achieved. This is a result of the higher attenuation of the differential-mode signal, compared to the common-mode signal. In addition to a higher CMRR, probe circuits with a lower attenuation ratio typically have a more stable frequency profile of the differential-mode signal and a wider 3 dB bandwidth. For the characterized test probe circuit samples, the repeatability of the CMRR is within 5 dB, while the repeatability is better for the professionally assembled wafer probes. This shows the impact of the soldering and assembly process on the repeatability of the probe circuit characteristics.

The probe circuit layout is optimized in order to improve the CMRR. The optimized probe circuit layout is implemented on a differential connectorized probe with a well-defined ground connection, and a fully floating differential wafer probe. The CMRR of the the wafer probe with the optimized probe circuit design is 10 dB higher than for the initial probe circuit design. The ground connection does not have an impact on the differential-mode signal propagation, while the impact on the common-mode signal suppression is very significant. A much higher CMRR is achieved when a well-defined ground reference is available. The connected-ground and floating-ground probe both have a similar 3 dB bandwidth of around 3.5 GHz. However, the connected-ground probe has a CMRR above 30 dB up to 4.4 GHz, while the floating-ground probe has a CMRR above 20 dB up to 1 GHz.

The impact of using an isolated power-over-fiber power supply on the performance of the probes is examined in terms of noise in the differential-mode and common-mode signal transmission. The impact of the noise coming from a non-isolated power supply and noise coupling on the electrical wires is relatively small for the probe with a well-defined ground reference. However, power supply isolation is critical for the fully floating differential probe, as it greatly reduces the noise level in the differential-mode and especially in the common-mode signal transmission. In addition to a significantly higher CMRR over a wide frequency range, the connected-ground probe also has the higher and more stable differential-mode and common-mode input impedance at higher frequencies, with a very low parasitic capacitance. The presented simple and low cost probe circuit design can be further miniaturized and realized on probes with different fixture types and applications in ESD and EMC measurement systems.

# Chapter 5

# Conclusion

A broadband differential electro-optical voltage measurement system is designed and characterized. The electro-optical probe circuit consists of three main parts: the attenuator, the laser and the bias circuit. Each part of the electro-optical system is characterized separately and its design is optimized in order to increase the common-mode rejection ratio of the differential measurement system. An iterative research approach is used, by combining the results of measurements, electromagnetic and circuit simulations, in order to improve the performance of each part of the probe circuit design over multiple design iterations. Frequency domain characterization of the differential circuits is performed by measuring the mixed-mode S-parameters, and evaluating the response to differential-mode and common-mode input signals.

The improvements made to the attenuator circuit design, the laser layout and the bias circuit design are incorporated in the probe circuit design. The optimized probe circuit layout is implemented on a differential connectorized probe with a well-defined ground connection, and a fully floating differential wafer probe. Despite the difference in the fixture and ground connection, both probes are realized in a differential configuration and the laser is driven differentially. The probes are designed for differential measurement of ESD voltage waveforms with amplitudes up to 100 V (200 $V_{PP}$). Although no significant power dissipation is expected when working with ESD pulses, the maximum allowed input differential RMS voltage is 14.1 V.

The probe ground connection does not have an impact on the differential-mode signal propagation, while the impact on the common-mode signal suppression is very significant. A much higher CMRR is achieved when a well-defined ground reference is available. The connected-ground and the floating-ground probe both have a similar 3 dB bandwidth of around 3.5 GHz. However, the connected-ground probe has a CMRR above 30 dB up to 4.4 GHz, while the floating-ground probe has a CMRR above 20 dB up to 1 GHz.

The impact of the noise coming from a non-isolated power supply and noise coupling on the electrical wires is relatively small for the probe with a well-defined ground reference. However, power supply isolation is critical for the fully floating differential probe, as it greatly reduces the noise level in the differential-mode and especially in the common-mode signal transmission. The nominal differential-mode input impedance of the connected-ground probe is 2095 Ω with a parasitic capacitance of 0.13 pF, while the nominal common-mode input impedance is 525 Ω with a parasitic capacitance of 0.48 pF.

A higher CMRR is typically achieved for probes with a lower attenuation ratio. This is because the common-mode signal cannot be attenuated by the same amount as the differential-mode signal, given that there is a contribution to the common-mode signal that is independent of the probe attenuation ratio. Using resistors with a lower nominal resistance also results in a more stable differential-mode signal transmission over a wide frequency range for probes with a lower attenuation ratio. Differences in the CMRR between probe circuit samples with identical layouts of up to 5 dB are observed. This is a result of the tolerances of the passive

components used in the probe circuit, the laser samples, and the parasitics introduced by the soldering process. Better repeatability between probe samples can be achieved when using a professional soldering and assembly process.

A steady drop in the CMRR at frequencies above 4.5 GHz is observed for all characterized probe circuits, regardless of the probe circuit topology and the attenuation ratio. This shows a fundamental limitation of the proposed probe circuit design. Such a high frequency drop in the CMRR is not observed when characterizing the attenuator circuit and the laser diode separately. The high frequency drop in the CMRR is a result of the interaction of the differential-mode and common-mode signal propagation through the attenuator and the laser, in combination with the differential-mode and common-mode impedance matching between the two circuits. The CMRR of the electro-optical probe circuit can be improved by optimizing the attenuator output impedance and the laser input impedance. By controlling the impedances the common-mode signal level at the input of the laser can be reduced, relative to the differential-mode signal level, thus increasing the CMRR of the system.

A differential electro-optical voltage measurement system that works well up to several gigahertz has been developed. A simple and low-cost probe circuit design is used. Optical links are used for both the RF signal and the bias signal, to galvanically isolate the system, allowing it to operate in an electromagnetically polluted environment. The limitations of the system in terms of stability of the differential-mode signal transmission and the high frequency drop in the CMRR are shown. Suggestions for further improvements of each part of the probe circuit design are proposed. Instead of heavily focusing on the lower frequencies at the expense of high frequency performance, a more stable CMRR frequency profile is achieved. This is accomplished by simplifying the circuit design and using only the essential components, which reduces its physical size, improves the performance, and also keeps the cost down. Along with ESD waveform characterization, the developed probe circuit design can be modified to perform measurements for EMC applications. The proposed design allows for experimentation with different fixture types, in order to reduce the size of the probe, and incorporate it into an integrated circuit test environment.

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# List of Abbreviations

| | |
|---|---|
| **CBCPW** | Conductor-backed coplanar waveguide |
| **CMRR** | Common-mode rejection ratio |
| **DC** | Direct current |
| **DUT** | Device under test |
| **EM** | Electromagnetic |
| **EMC** | Electromagnetic compatibility |
| **ESD** | Electrostatic discharge |
| **ESL** | Equivalent series inductance |
| **ESR** | Equivalent series resistance |
| **FEM** | Finite element method |
| **GSGSG** | Ground-signal-ground-signal-ground |
| **MAE** | Mean absolute error |
| **MLCC** | Multi-layer ceramic capacitor |
| **MoM** | Method of moments |
| **NRMSE** | Normalized root-mean-square error |
| **PCB** | Printed circuit board |
| **PMVNA** | Pure-mode vector network analyzer |
| **PoF** | Power-over-fiber |
| **Q-factor** | Quality factor |
| **RBW** | Resolution bandwidth |
| **RF** | Radio frequency |
| **RMS** | Root-mean-square |
| **SMA** | Subminiature version A |
| **SMT** | Surface-mount technology |
| **SNR** | Signal-to-noise ratio |

| | |
|---|---|
| **SRF** | Self resonant frequency |
| **S-parameters** | Scattering parameters |
| **TDMM** | True differential measurement mode |
| **TO** | Transistor outline |
| **TOSA** | Transmitter optical subassembly |
| **TOSM** | Through-open-short-match |
| **VCSEL** | Vertical-cavity surface-emitting laser |
| **VNA** | Vector network analyzer |
| **Y-parameters** | Admittance parameters |
| **Z-parameters** | Impedance parameters |

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# Biography

Hrvoje Štimac was born in 1988 in Zagreb, Croatia. He received the M.S. degree from the University of Zagreb Faculty of Electrical Engineering and Computing, Zagreb, Croatia, in 2013. He started working at the Faculty of Electrical Engineering and Computing in 2014, first as a research associate and then as a research and teaching assistant since 2016. He has enrolled in the Ph.D. program in electrical engineering at the University of Zagreb Faculty of Electrical Engineering and Computing in 2015. As a teaching assistant he has thought five undergraduate and graduate courses at the University of Zagreb. He participated in several national and international research projects. He has authored multiple papers published in peer-reviewed international journals and presented papers at international conferences. His research interests include the design and characterization of broadband differential probes for voltage and current sensing, radio frequency design, and modelling of microwave structures and components.

## List of published papers

### Journal papers

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# Životopis

Hrvoje Štimac rođen je 1988. godine u Zagrebu. Završio je diplomski studij na Fakultetu elektrotehnike i računarstva Sveučilišta u Zagrebu 2013. godine. Zaposlen je na Fakultetu elektrotehnike i računarstva od 2014. godine, prvo kao zavodski suradnik, a zatim kao asistent od 2016. Doktorski studij iz elektrotehnike upisao je 2015. godine na Fakultetu elektrotehnike i računarstva Sveučilišta u Zagrebu. Kao asistent sudjelovao je u nastavi pet predmeta na preddiplomskom i diplomskom studiju na Sveučilištu u Zagrebu. Sudjelovao je u nekoliko nacionalnih i međunarodnih istraživačkih projekata. Autor je više radova objavljenih u međunarodno recenziranim znanstvenim časopisima te je prezentirao radove na međunarodnim konferencijama. Njegovi istraživački interesi uključuju projektiranje i karakterizaciju širokopojasnih diferencijskih sondi za mjerenje napona i struje, radiofrekvencijski dizajn te modeliranje mikrovalnih struktura i komponenata.